TI Developer Conference
Birmingham Nov 11 • Paris Nov 13 • Munich Nov 14

TI Developer Conference
European Series

Birmingham November 11
Paris November 13
Munich November 14

www.ti.com/europe/devcon

Conference details

Contents

VENUES & FEES

Locations

Nov. 11th, 2002
UK: Birmingham – Hilton Hotel
Hilton Birmingham Metropole
National Exhibition Centre,
Birmingham, GB B40 1PP
Tel: +44-121-7804242
Fax: +44-121-7803923

Nov. 13th, 2002
France: Paris – Coeur Défense Conference Center
110, Esplanade du Général de Gaulle,
92032 Paris La Défense cedex
France
Tel: +33 1 46 92 21 21

Nov. 14th, 2002
Germany: Munich – Hilton Park Hotel
Am Tucherpark 7
80538 Munich
Germany
Tel: +49-89-38450
Fax: +49-89-38452588

Conference fee

There is a 100 euro*package fee (excl VAT) to cover the full conference, lunch, breaks and workbook.

Registration and detailed agenda:

Please see: www.ti.com/europe/devcon

Email Contact: devcon@list.ti.com

CONFERENCE AGENDA

	Track	Video / Imaging	Embedded Communication	Industrial & Digital Control	Audio	Hardware	Software	DSP Fundamentals Workshop*
8.00-8.30	Welcome coffee and registration							
8.30-9.30	Introduction							
9.30-11.00	**Module 1**	Technology trends, challenges & solutions	Speed-up telephony application design	Flexible embedded control development tools	Technology trends, challenges and solutions	Basics of understanding DSP hardware	Introduction Software Reference Framework	Workshop
11.00-11.30	Break							
11.30-13.00	**Module 2**	Video security, entertainment & portable applications	Considerations for your modem design	Sensorless vector control solution	Professional and high-end audio	Advanced design rules to design board	DSP application debug, analysis & tuning	Workshop (continued)
13.00-14.30	Lunch							
14.30-16.00	**Module 3**	Multiprocessor video system considerations	How to integrate a TCP/IP stack	Porting floating point algorithms to fixed-point DSPs	Compressed audio and related applications	Complex hardware board debugging	Analyze an embedded application using RTDX™	Workshop (continued)
16.00-16.15	Break							
16.15-17.30	Guide to TI design and support							Workshop (continued)
17.30	Conference ends							

VIDEO & IMAGING

Video/Imaging Module 1

Length: 90 minutes
Time: 9.30-11.00

Module title:

Digital Video and Imaging Systems – The Challenges and The Pieces of the Puzzle

Target audience:
Focused on Engineering detail, anyone interested to get a good overview of digital video systems and the underlying technology.

Speaker: Jean-Marc CHARPENTIER, Roger MONK, Arnaud LASSERRE, Texas Instruments

Abstract
As the World of Digital Multimedia Content continues to expand and become universally accepted into markets such as Broadcasting (DVB, Set-Top-Box), Communication and Security markets, the 'Video and Imaging Systems Designer' is faced with a new and challenging set of system design goals. Partitioning system resources between hardware and software is now further 'blurred' by the challenge of finding the optimum balance of cost / integration and product flexibility. As the designer strives to build their new 'state of the art' equipment, some of the more challenging design aspects are due to the explosion of new video standards as MPEG4, HDTV, H26L, MWM9,... requiring constantly changing algorithm requirements. The disruptive technology brought by the Multimedia Broadband Infrastructure capabilities, the heterogeneous network connections implying trans-coding or trans-rating functionality and the increasing complexity and rapid evolution of algorithms to implement do not lower this challenge.

This track should help you to go successfully through this whole challenge. After reviewing the market trends in video and imaging systems, we shall overview most of the basics about analog / digital video formats (color space, RGB/YUV, BT.601/656, ...) and codecs both hardware (TVPxxx) and software (JPEG, MPEG-x, H.26x). At the end, you will learn about video system architecture including interfacing and network applications.

Module agenda:
– General market trends in video imaging systems
– Overview of digital video systems
  - Video Formats (Analog / Digital)
  - Video Codecs (Hardware / Software)
– Digital Video Applications
  - Application areas
  - Decisions / Trade-offs
  - System architecture and challenges
– Wrap-up / Q&A

Speaker information:
Jean-Marc CHARPENTIER, Roger MONK, Arnaud LASSERRE
European Business Development Manager, Video and Imaging DSP Field Applications Engineers
Texas Instruments

After completing a Masters Engineering Degree at Nottingham University in England, Roger Monk joined TI as part of the Texas Instruments European Graduate Program, where he worked on Digital Motor Control applications, High Performance DSP applications and DSP Embedded Operating System software. Over the last 2.5 yrs Roger has worked as part of the North European Technical Applications team, with a key focus on Video/Imaging and Networking Applications, using TIs TMS320c6000 family of DSP processors, working with European customers to develop their programmable DSP-based video solutions.

Video/Imaging Module 2

Length: 90 minutes
Time: 11.30-13.00

Module title:
Imaging applications; Client side and Portable applications

Target audience:
Project management, decision makers

Speaker: Marc GUILLAUMET, ATEME

Abstract
What does DSP technology bring to video appliances? Why use this technology now? What critical features drive the adoption of this technology?

What does it take to build a product with a DSP inside, what are the benefits of programmability?

Improving features and flexibility while cutting down time to market and total cost of ownership are the critical points of this presentation.

We will try to answer these questions by taking a look at some generic applications:
Video security: with different applications such as video-security networks, battery powered home surveillance, video recording,…
Video entertainment and Digital Video Recorder: with transport and hotel equipments, for instance
Portable video applications, battery powered.
What are the typical hardware and software architectures for each typical application? What about programmable logic? Which DSP is the most appropriate?

In even more concrete terms, we are going to show ways to get started in new imaging design on DSP: available hardware platforms, software tools, and support possibilities. Tools, standards, frameworks and solutions are the keys to shortening time to market.

Module agenda:
– Track introduction
– Ateme background
– Subject introduction
– Video security
– Video Entertainment
– Portable video
– Developments steps
– Ateme and TI tools and support

Speaker information:
Marc GUILLAUMET
Marketing Director
Ateme

Marc GUILLAUMET has been with Ateme since 1992, when he joined as employee number 10. After 7 years spent in the management of technical staff and development projects, he created and developed Ateme's products business unit. He holds now the position of Marketing Director. He has a leading role in defining the product development roadmap, and heads the products business both from a technical and marketing point of view. Marc obtained a Masters Degree in Aeronautics Engineering from SUP'AERO (France) (E.N.S.A.E.) in 1991.

Video/Imaging Module 3

Length: 90 minutes
Time: 14.30-16.00

Module title:
Building High-End Video & Imaging Solutions for Real-World Applications

Target audience:
Video & Imaging product designers & developers, high-end application users & integrators

Speaker: Joel Rotem, Mango DSP Ltd

Abstract
The increasing demand for higher performance Hardware & Software applications in the fields of Digital Video and Imaging is constantly growing. Companies now need to provide full Hardware & Software solutions while keeping cost and time to market to a minimum. This session will demonstrate the methods used to build high-end applications in a short time and also aims to highlight some of the additional considerations involved with designing and using multiple image processing engines for very high end 'infrastructure style' applications. It will cover product definition, prototyping, hardware and software development up to production. The benefits of programmability, flexibility and upgradability will also be covered.

Real products examples will be discussed to explain how TI's Hardware and Software can be used for :
– Building/Choosing a development platform
– Building a Video broadcast/communication server
– Building Digital Video Surveillance Systems
– Building Optical Inspection Systems

Module agenda:
– Intro: High-end Video Applications (Communication, Broadcast, Surveillance) / Imaging (Optical Inspection)
– The challenges of the field
– An overview of current solution technologies
– The advantages of the TI resource environment (CCS, DSP Village, Third party software)
– Sample development platform
– Video Server Example & Demo
– Video Surveillance example & demo
– Optical Inspection example & demo
– Q&A

Speaker information:
Joel Rotem
Application engineer
Mango DSP Ltd

Graduated EE Tel Aviv University 1995, Majoring in DSP, Computer and Communication Systems. 1995-1999 DSP developer at Waves Inc. Specializing in high end Audio Signal Processors, Psychoacoustics and DSP optimisation. 2000-2001 Co Founder & VP. R&D DVDemand Inc. Specializing in DVD/DVB, MPEG-2. Filed two patents in the field of DVD & MPEG-2. 2002+ Application Engineer at Mango DSP, Specializing in Digital Video.

EMBEDDED COMMUNICATION

Embedded Communication
Module 1

Length: 90 minutes
Time: 9.30-11.00

Module title:
Speed up the design of your telephony application.

Target audience:
System engineers, DSP software developers, project managers, technical marketing, sales managers.

Speaker: Alexey Frunze, SPIRIT Corp.

Abstract
The workshop will teach how to quickly develop any user-specific telephony application based on C54CST chip with its flexible Telephony Framework and several most popular algorithms (modems/voice processing/PSTN signalling).

It will explain the concept of multi-layer telephony Framework which can significantly reduce the development time and help engineers concentrate on high-level design. Examples will be given on how to build a simple voice-processing application.

The workshop will address how to create voice/modem-processing applications (such as VoIP, Remote data collection, smart phones) using the integrated telephony solution (C54CST chip), how to add user-specific drivers for external devices, how to create a complete software/hardware solution, and other development issues.

Furthermore, it will be shown how SPIRIT's Telephony Framework, working on DSP/BIOS™ and TI Reference Framework, will speed-up the design of your application.

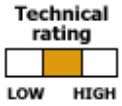
Module agenda:
– Why Are You Here?
– C54CST Chip Overview
– Telephony Framework Overview
– Flex Application Design Quick Start: 3 Steps!
– Lab 1: Hello, Ring!
– Lab 2: Voice Toy
– Call to Action & References
– Q & A

Speaker information:
Alexey Frunze
CST Senior Engineer
SPIRIT Corp.

Mr. Frunze graduated with M.S. degree in Physics from Moscow State Pedagogical University, Moscow, Russia, and then finished his graduate studies in Electrical and Computer Engineering at the University of Rochester, NY, USA. Mr. Frunze has over 5 years of software engineering experience (including embedded systems software and DSP software)

Embedded Communication
Module 2

Length: 90 minutes
Time: 11.30-13.00



Module title:

Considerations for your modem design: From Schematics to Homologation

Target audience:
System engineers, DSP software developers, project managers, technical marketing, sales managers.

Speaker: Terry Engel. TITAN Technology Alliance, LLC.

Abstract

The workshop will teach how to design an embedded modem. What are the consideration to take into account, problems you could encounter and how to solve them? It will explain how to define the schematics and the layout and how to place the oscillator vs the DSP vs the DAA vs power supply.
By defining a good layout, we will teach you how to:
- Get the best modem performance.
- Address the country regulations (TBR21, FCC, JATE).
- Implement a safe design answering the High voltage isolation regulations.
- Be compliant with the Electro-Magnetic interferences rules.

Country certifications are the ultimate goal and we will teach you how to meet them and the different tests you will have to pass.

Module agenda:

A) Modem Overview
- Terminology (e.g. V.xx data rates; what is V.42/42bis, etc.)
- Basic Modem Architecture (e.g. controller-based, contoller-less, soft)
- Embedded Modem overview -- what is it / how different from PC

B) Typical Process of a Modem Design (from customer view)
- Evaluate potential solutions (what are key criteria: cost, power, space, reliability, etc.)
- System considerations (e.g. Use UART or HPI)
- More of a listing of steps a customer would go through: module vs. chipset tradeoff;
- Schematics and layout considerations

C) Software View of Modem
- Overview of AT commands (w/ common examples)
- Other items like country code explanations, sampling rates (digital PBX vs. analog line); drivers?

D) Modem Performance
- What type of testing is / should be expected from a V.90 modem?
- NMC coverage (other test

E) Homologation / Certification procedures
- What is homologation?
- Why do modems need to be certified and how is this done?

F) Questions & Answers

Speaker information:

Terry Engel
TITAN Technology Alliance, LLC

Terry Engel

Mr Engel has worked the last 17+ years in the area of high-speed modem design. His work in this area began with the design of custom LSI's for modem applications at General DataComm, an early pioneer in high-speed modem design. For the last 13 years, he has shifted to the software side, writing digital signal processing algorithms and control code for modem applications.

Embedded Communication
Module 3

Length: 90 minutes
Time: 14.30-16.00

Module title:
Integration of a TCP/IP stack

Target audience:
DSP engineers interested in the development of embedded Internet applications based on TMS320 DSP.

Speaker: Rutger van Dalen, Windmill Innovations

Abstract
The presentation provides insight into the development of DSP applications which require Internet connectivity. Starting with an introduction to TCP/IP communication, the presentation will cover the entire development process of an Internet-enabled DSP application, including configuration, integration and debugging.
The process is illustrated with live demonstrations using Windmill Innovations' bf3Net TCP/IP Protocol Stack. Both Ethernet and Point-to-Point Protocol (PPP) connections will be discussed.

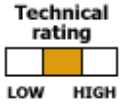
Module agenda:
– TCP/IP Communication Basics
– Embedded Internet for DSP Applications
– bf3Net and eXpressDSP™Configuration of the TCP/IP Protocol StackIntegration of the TCP/IP Stack with the DSP Application
– Integration of Physical Layer Drivers and Application Protocols
– How to Debug Embedded Internet Applications
– Monitoring the Run-time Behavior of the TCP/IP Communication
– Optimizing the TCP/IP Stack Configuration
– Conclusion/Summary
– Questions and Answers

Speaker information:
Rutger van Dalen
Vice President Engineering
Windmill Innovations

Mr. Rutger van Dalen is the vice president of engineering at Windmill Innovations. He has eight years experience in DSP and embedded application design, and was actively involved in the architectural definition and design of bf3Net.
Previously, he worked as design engineer in the Bell Labs organization of Lucent Technologies. Mr. Van Dalen graduated from the Technical University in Darmstadt (Germany) as telecommunications engineer.

INDUSTRIAL & DIGITAL CONTROL

Industrial &
Digital Control
Module 1
Length: 90 minutes
Time: 9.30-11.00



Module title:
Visual Embedded Controls Development for TI LF2407/F2812 with VisSim

Target audience:
Software designers, Project managers

Speaker: Peter Darnell, Visual Solutions

Abstract
Learn how to speed designs to market with VisSim/Embedded Controls Developer. By abstracting chip peripherals, and hand coded assembler routines into a high-level block set, VisSim/ECD lets you rapidly test, verify, and generate embedded targets for industrial control applications. Current applications include high voltage, 2 stage H-Bridge power supply control, multi-unit Gas Turbine power generator control, Brushless DC control for Robotics, AC Induction motor control.

Module agenda:
– Quick intro to visual programming with VisSim
– Design of fixed point filters
– Discussion of scaled fixed-point block set for efficient floating point calculations
– Review of block set for C2000 peripheral support (Analog In, Digital I/O, CAN, PWM, Encoder, Event Capture, SCI, SPI, I/O Space read/write)
– Review of Digital Motor Control block set: 2nd harmonic 3 phase wave form generation, Park & Clarke transformations, fixed point PID, etc.
– Demonstration of virtual prototyping
– Demonstration of live feedback control with Visual Interface using PWM and Encoder blocks
– Demonstration of embedded target creation using C-Code generator, fixed-point block set, and Code Composer

Speaker information:
Peter Darnell
President
Visual Solutions

Peter Darnell
President and founder of Visual Solutions, Inc. (1989-present)
Associate Professor UMass, Lowell
Member of ANSI X3J11 Committee to Standardize the C language
Compiler engineer at Data General, Masscomp, Stellar (1976-1989)
Graduate work in compiler design at MIT 1977-1980
Author of VisSim - simulation software. Author of "C, A Software Engineering Approach", Springer Verlag
US Patent #4829422 "CONTROL OF MULTIPLE PROCESSORS EXECUTING IN PARALLEL REGIONS"
Graduate work in compiler design at MIT 1977-1980
BA Physics, University of Connecticut, 1976

Industrial & Digital Control Module 2

Length: 90 minutes
Time: 11.30-13.00

Module title:

Sensorless vector control solution for AC Induction Motor using NFO algorithm

Target audience:
Hardware designers, Software designers, Project managers

Speaker: Fredrik Jeppsson, NFO Control AB

Abstract
Natural-Field-Orientation enables a cheap, reliable AC induction motor to be controlled as easily as a DC motor, achieving servo performance. Natural-Field-Orientation is a new method of field-oriented control, which works without sensors on the motor. Measurement of the current and voltage supplied to the motor provides information for control.
The name "Natural Field Orientation" was chosen since the control system adapts in a natural and simple manner to the native properties of the motor. In effect, the control system is a mirror image of the motor.
NFO describes how the control signals for the motor should be generated. In practice, this is done on a Texas Instruments DSP.
The main advantages of NFO are: Sensorless, Constant speed (Slip compensation), Full torque at all speeds, Fast torque and speed response, Wide speed range, Simplicity (no boost settings).
The presentation explains how NFO works and its applications, including a live elevator speed-servo demonstration.

Module agenda:
– Introduction
– How Natural-Field-Orientation works
  - Necessary signals
  - How to calculate motor parameters
– Implementation on a TI DSP
  - Software structure
  - MIPS load
  - Hardware considerations
– Applications
– Demonstration
– Q & A

Speaker information:
Fredrik Jeppsson
Engineering Manager
NFO Control AB

Fredrik is the Engineering Manager of NFO Control AB since 2000. He has over 20 years experience in development and application support of analog circuits, power electronics and embedded sy stems. Previous position include Hardware/Software design consulting, Application engineering in automotive and motor control for Siemens Semiconductors (now Infineon), ICE and compiler support for embedded tools manufacturer Nohau and Solution Team Leader for "DSP and high-end uC" at TI Distributor Hatteland (now Arrow Nordic).

NFO®

Industrial & Digital Control Module 3

Length: 90 minutes
Time: 14.30-16.00

Module title:

Floating point capabilities on fixed point devices : IQ math.

Target audience:
Software designers and project managers

Speaker: Alex Tessarolo, Texas Instruments

Abstract
A new approach to fixed point algorithm development on the C28x DSP, which greatly simplifies the designer's development task. This IQ math approach can be termed "virtual floating point" in that it looks like floating point math, but it'simplemented using fixed point techniques. An example of an ACI vector controlled motor is used to illustrate the concept and make performance comparisons against a floating-point implementation.

Module agenda:
– The Fixed-Point DSP Development Dilemma & Approach
– The IQmath Approach And How It Addresses The Problem
– AC Induction Motor Example
– The IQmath Library
– IQmath On C28x versus Floating-Point On C3x/C67x
– Applicability & Road-Map

Speaker information:
Alex Tessarolo
Chief architect
Texas Instruments

Alexander Tessarolo, Senior Member Technical Staff at Texas Instruments, joined 1989. Main responsibilities; Cheif Architect of the C28 32-bit DSP core and Chief Systems Architect for all C28 DSP based products in the Digital Control Systems (DCS) group. Over 20 years experience in DSP algorithms, software, architecture, custom designs and in the application of DSP in the fields of digital control and hard disk drives. B.E.E University Of Technology, Sydney, 1st Class Honours.

AUDIO

Audio Module 1

Length: 90 minutes
Time: 9.30-11.00

Module title:

Digital audio: Users and Uses, Challenges and Heroes

Target audience:
Consumer product development managers; audio architecture specialists; hardware design engineers

Speaker: Kendall Castor-Perry, Texas Instruments

Abstract
Audio touches all our lives, and increasingly today it's digital technology which is responsible for the creation, transmission and reproduction of our musical 'fix'. TI's broad competences in all areas of signal processing and communication are proving more valuable than ever, as audio systems converge with computation and communications infrastructure, at work and at home. After a quick look at the path that music can take from the performer's lips to the listeners' ears, we'll look at how the gradual adoption of new audio technologies in the market is affected by the nature of different kinds of customers. We'll review the challenges that you face in designing good audio equipment, and then look in greater detail at seven selected new TI audio devices, all of which represent some significant advance in the state of the art. These parts include the highest performance audio DSPs around, latest generation single chip 1394 devices for AV applications, TI's groundbreaking True Digital Audio Amplifier products, and some analogue audio components with innovative features and world-record performance. Combining some important market observations with a focus on technical analysis and discussions about key audio devices, this presentation will give you a real insight into how TI is combining its product design, systems knowledge and market understanding into a set of powerful solutions for Audio in the 21st Century. Interaction from the audience will be strongly encouraged!

Module agenda:

- How music moves from the creator to the consumer
- Why you need to understand how your customers adopt technology
- The challenges you're facing in the marketplace

Solutions: High performance digital audio signal processing on both programmable and fixed function audio DSPs; audio interfacing and conversion, and high efficiency audio amplifiers. Technical review.

Speaker information:

Kendall Castor-Perry
Audio & Consumer Specialist
Texas Instruments

Kendall has worked in the electronics industry since 1977 and has held a wide variety of roles in engineering, design, marketing and management. He has specialised in precision signal processing, particularly filtering, and has a career-long interest in the fundamentals of quality audio reproduction in both analogue and digital domains. He joined Burr-Brown in 1998 to manage the Audio product space in Europe, applying his broad technical and commercial knowledge to growing BB's audio business. He holds a BA in Physics from Oxford University and an MBA from London Business School, and is currently on the UK Committee of the AES.

Audio Module 2

Length: 90 minutes
Time: 11.30-13.00

Module title:

Developing Audio Systems for Professional and High-End Audio Segments

Target audience:
Professional audio and high-end consumer audio systems developers

Speaker: Mr. Jean-François OUELLET, LYRTech Signal Processing

Abstract
The audio industry has so far been dominated by fixed-point processors and ASICs, mainly for cost and B.O.M. concerns. However, the advent of powerful yet low-cost floating-point DSP processors is opening a myriad of opportunities for high-end & professional audio systems developers. Extended dynamic range, ease of programming and development, availability of development frameworks and system-level design tools make it possible for engineers to develop more demanding audio applications while making them available sooner to customers. This session will introduce the benefits of using floating-point DSP processors for audio applications, examine related design methodologies (with a special emphasis on system-level design approaches), and present developers' and other technical testimonials of how such an approach has proven beneficial in the recent past, and how. As a conclusion, currently available solutions as well as practical "Where to Start?" suggestions will be provided.

Module agenda:
– Introduction
– Benefits of floating-point over fixed-point for leading-edge audio applications development
– New design methodologies for audio
– Testimonials
– Where to start?

Speaker information:
Mr. Jean-François OUELLET
Director, European Technical Marketing & Sales Engineer
LYRtech Signal Processing (LSP)

Mr. Jean-François OUELLET has been LYRtech Signal Processing (LSP)'s Director of Technical Marketing since 1997, and has recently been appointed Director of the company's new European office, based in Grenoble, France. After attending Laval University's Computer Engineering program, he went on to pursue an MBA in Marketing in Québec City, Canada. Mr. Ouellet is co-author of a number of articles relating to the use of FPGAs and DSP processors in the fields of telecommunications, embedded control and audio/video processing, and has been presenting many of those papers in conferences, mainly in Asia and the United States.

Audio Module 3

Length: 90 minutes
Time: 9.30-11.00

Module title:

Review of digital compressed audio standard/trends & related applications

Target audience:
Consumer product development managers; audio architecture specialists; hardware design engineers

Speaker: Elie Belmand / Gerardo Murillo, Texas Instruments

Abstract
The market for Digital Compressed Audio products has shown constant growth over the past three years and is expected to keep on gaining momentum. The proliferation of various Compressed Audio format is shaping the utility function of users in terms of the versatility required, that is ensuring seamless multi-format coding/decoding on their portable, Home and Car equipment. The increasing demand for smart Audio devices is also changing the way engineers design the architecture for Compressed Audio products and select the best DSP platform to get their design on time to market.
The presentation reviews the different Audio standards and looks at the cost effective ways to reduce the silicon count, but increase the functionality of the product by selecting the appropriate DSP platform. The presentation goes through the Software and Hardware requirements for various audio products specifications and explains how TI DSPs can match the requirements for diverse audio applications.

Module agenda:
Marketing perspective
- Products categories
- Market forecast

Digital Audio technologies
- Audio Compression principle
- MP3, MP3 pro, AAC, etc.
- Digital Rights Management

TI value proposition
- Platforms C54x, C55X
- Software
- System Solution

Speaker information:
Elie Belmand, European Business Development Manager
Gerardo Murillo, Field Application Engineer
Texas Instruments

Elias Belmand is the European Business Development Manager for the Internet Audio Group at Texas Instruments France. Prior to joining TI, Elias worked in the consumer electronics industry and held various R&D roles in the Digital TV and Set Top Box businesses. Elias holds two patents on Digital Nyquist Filtering for Intermediate Frequency processing and Video / Graphics data compression. Elias holds a MSEE from the ENSPS, diplome dIngenieur and DEA, and a MBA from the Australian Graduate School of Management.

Gerardo Murillo is a Member of the Technical Staff and supports European applications for the Imaging and Audio group within TI. He hold a PH.D degree in signal processing and has worked as a researcher with CNRS French national research labs before joining Texas Instruments DSP labs in Nice. He is currently working at a system level on programs involving multimedia processing, such as digital audio portable players, cellular media coprocessors and car audio, implementing solutions in which the DSP handles the complete application from the software , hardware and system point of view.

HARDWARE

Hardware Module 1

Length: 90 minutes
Time: 9.30-11.00

Module title:
Basics of understanding DSP hardware

Target audience:
Project managers, Decision Makers, Purchasers and DSP Beginners

Speaker: Neville Bulsara, Texas Instruments

Abstract
The goal of this module is to provide a basic understanding of the signal chain of a Digital Signal Processor based design and is targeted at people having little or no DSP experience. The session helps the attendee to determine the different possible options for a new hardware architecture, covering aspects like the definition of a suitable power supply, the understanding of different types of memories, the main features of fixed and floating point Digital Signal Processors etc...

For each of these items, key criteria are given to determine the most appropriate choice depending on system constraints. The complex theme of managing the data flow in a design is used to address specific issues like the use of DMA and the control of external communication links. The chip support libraries available in the TI DSP development tools are also demonstrated to show how they can help to reduce the DSP code development time and complexity.

Module agenda:
– General overview of a DSP board
– Description of the main hardware blocs : power supply, memory, ADC, DAC, communication links (SPI, SCI, McBSP, CAN), buses.
– Fixed point versus Floating point architectures
– Data flow management at system level : external vs internal accesses, DMA pros and cons, high and low speed communication links.
– C5000 Chip support library demonstration.

Speaker information:
Neville Bulsara
Field Application Manager
Texas Instruments

Neville has worked in the electronics industry since 1983 and has held a variety of roles in engineering, hardware and software design, technical marketing and management. After a varied career in the telecom industry he joined Texas Instruments in 1997 as a DSP Field Applications Engineer in the UK, and has a strong commitment to the proliferation of DSP technology into new and emerging markets, where Neville is currently active in the fields of DAB, V.90 modem, and related technologies. He holds a First Class Honours Degree in Combined Engineering Studies and is currently manager of the North region catalog DSP team

Hardware Module 2

Length: 90 minutes
Time: 11.30-13.00

Module title:
Advanced design rules to design board

Target audience:
Hardware designers

Speaker: Peter Forstner, Texas Instruments

Abstract
This session is targeted at design engineers who will be working on systems which will include high speed DSP devices. It will cover basic and advanced design rules and also offer solutions to solve the main hardware design headaches. This module provides practical (and useful !) tips for the design of clocking circuits, recalls the theoretical background of transmission line theory to address key phenomena like data reflection and crosstalk as well as addressing PCB layout rules for both digital and analog systems (including reference to supply voltages and analog signal lines). Finally critical information regarding Bus design such as open collectors, floating lines and bus termination is covered.

Module agenda:
– Clock circuits (crystal oscillators types and design tips)
– Transmission (transmission line theory, reflection, crosstalk)
– Lay-out rules (supply voltage, digital signal lines, unused inputs, clocks, analog rules)
– Bus systems (bus termination, clamp circuits, open collectors' systems, floating lines, design rules)

Speaker information:
Peter Forstner
Technical Support Engineer, Member Group Technical Staff
Texas Instruments

Dipl. Ing. **Peter Forstner**, born in Nürnberg, Germany, studied electrical engineering at the Technical University in Berlin. 1984 he started to work for Texas Instruments in Freising as Product Engineer. In 1991 he became a Field Application Engineer with European wide responsibility for backplane bus systems and signal integrity problems. Peter presented about 80 Digital Design Seminars and Digital Design Workshops all over Europe with more than 2000 participants. Later his focus was on PCI bus systems. His actual assignment is MSP430 specialist in the Technical Support Team of the EPIC. He is "Member Group Technical Staff".

Hardware Module 3

Length: 90 minutes
Time: 14.30-16.00

Module title:
Debugging a DSP based system

Target audience:
Hardware Designers, Software designers, Hardware decision makers

Speaker: Sigolene Pangaud, Texas Instruments

Abstract
This module will discuss how TIs use of JTAG technology will ease and speed up the debug phase of the most complex hardware boards. It targets designers who want to understand how the implementation of a JTAG scan chain in their system - including Boundary Scan - dramatically improves the hardware debug phase. We will also show how the use of sophisticated design tools such as Code Composer Studio can help during these critical debug stages.

We will cover the power of Real Time Data Exchange (RTDX™) and DSP-BIOS™ diagnostics to provide a true real time debugging capability on a DSP based system without disturbing its real time processing capability (this is key in many high data throughput applications today) and speeding up the debug phase.

This session also explains some other, more sophisticated advanced tools packages from TI's 3rd Party Network which provide a key link between software simulation and hardware implementation during the conception phase.

Module agenda:
– TI's JTAG implementation across all the DSP platforms
– JTAG design and layout with single and multiple devices in the scan chain
– Benefits of Real Time Data Exchanger (RTDX) when debugging the hardware
– Interaction between RTDX and DSP-BIOS, hardware features of DSP-BIOS
– Smooth bridge between software simulation and hardware implementation thanks to Mathworks and Visual Solutions.

Speaker information:
Sigolene Pangaud
TMS320C6000 DSP Field Application Engineer
European Sales & Applications
Texas Instruments

Sigolene Pangaud is today a TMS320C6000 DSP Field Application Engineer for South Europe. She has joined TI-France 2 years ago as TMS320C6000 DSP product specialist. She has been in the semi-conductor industry since 10 years, working on telecom equipments (SDH, SONET, ATM), ASICs for such equipments, then ASIC libraries, memories for Sea-Of-Gate and standard cells solutions, then System On Chip (SOC), MCUs (8-bit, 16-bit, 32-bit Microcontrollers) and since 4 years, on DSP applications.

SOFTWARE

Software Module 1

Length: 90 minutes
Time: 9.30-11.00

Module title:

Introduction to Software Reference Frameworks

Target audience:
Software engineers

Speaker: Elisabete De Freitas, Texas Instruments

Abstract
Software Reference Frameworks are source code that customers can adapt and populate with various TMS320 DSP Algorithm Standard compliant algorithms to jumpstart application development. Some of the common features as well as technical details of the two available Software Reference Frameworks will be described. The different key characteristics and capabilities of each of the frameworks make them more suitable for one or the other type of application. TI offers selection criteria that aid the selection of the right one.
One of the elements of the Software Reference Frameworks are DSP/BIOS™ Device Drivers, which are implemented via the new DSP/BIOS Low-Level I/O Device Driver model. This layered model can be used to very easily build custom device drivers to interface to application specific external hardware.

Module agenda:

– Introduction to Reference Frameworks
– The eXpressDSP™ SolutionReference Frameworks using DSP/BIOS Device Drivers
– DSP/BIOS Device Driver Objectives
– Device Driver Software Architecture
– Reference Frameworks Availability

Speaker information:
Elisabete De Freitas
DSP Software Field Applications Engineer
Texas Instruments

Elisabete De Freitas completed an Engineering Degree at the University of the Algarve in Portugal and then developed a thesis project with a TMS320C24x DSP processor in the University of Zwickau in Germany. She joined Texas Instruments to work on Digital Motor Control Applications and was a Technical Support Engineer in DSP Applications in the Texas Instruments Graduate Program. Over the past two years she has been working as a Software Field Applications Engineer with the TI network of Third-Party developers and European customers to develop their Software Components and Application Frameworks.

Software Module 2

Length: 90 minutes
Time: 11.30-13.00

Module title:
DSP Application Debug, Analysis, and Tuning

Target audience:
Software engineers

Speaker: Rich Scales, Texas Instruments

Abstract

Tooling support for debug and efficiency analysis can provide deep insight into an applications' operation and performance. This lab provides an introduction to TI's express DSP™ tooling aimed at debug, analysis, and tuning. Cache analysis over time, multi-event profiling, code coverage, and pipeline analysis tooling will be used to detect potential problem areas and provide resolutions and improvements.

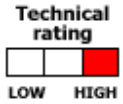
Module agenda:
– Application Development on the Simulation Platform
– Support for Debug & Analysis
– Demo: Simulation of a full Reference Framework application

Speaker information:
Rich Scales
Compiler technology product manager in SDS
Texas Instruments

Rich began his career at TI in 1990 in TI's memory business working on Flash EEPROMs. In 1993, he moved into the DSP group to work on the C6000 architecture development team. From 1993 – 1998 he worked on architecture evaluation, benchmarking, compiler evaluation, development tools directions, and the C62x/C67x floating point instruction sets.
In 1998, he managed the Catalog Products C6000 Software Applications team. In 2000, he joined the DSP Software Development Systems group as Compiler Technology Product Manager.
Currently, Rich is now responsible for Wireless infrastructure systems team in Europe. This system team focuses on 3G UMTS system design and advanced features.
Rich has a BSEE from North Carolina State University and an MEE from Rice University.

Software Module 3

Length: 90 minutes
Time: 14.30-16.00



Module title:

Analyzing an Embedded Application Using Real-Time Data Exchange (RTDX™)

Target audience:
Software engineers

Speaker: André Schnarrenberger, Texas Instruments

Abstract
TI's RTDX™ technology allows streaming of data between the DSP and the host PC in real time, i.e. not intruding on the DSP's real time constraints. Understanding the basic principles and building blocks of RTDX will help maximize data throughput. A focus is put on the features of the newly announced XDS560 technology which offers communication speeds of up to 2MB/s with High Speed RTDX. Step by step code examples introduce the RTDX APIs and show how to establish an RTDX connection between the DSP and the host. Windows applications can inject and extract data from the running DSP, e.g. to display real time data graphically.

Module agenda:
– Learn the fundamentals of the RTDX™ architecture for the XDS560™
– Understand the difference between Standard RTDX and High-Speed RTDX (HS-RTDX)
– Learn how to instrument a target audio application with RTDX
– Demonstrate the use of HS-RTDX

Speaker information:
André Schnarrenberger
Field Applications Engineer
DSP Applications Central Europe
Texas Instruments

DSP FUNDAMENTALS WORKSHOP

Please note this is an all-day workshop.
Participants selecting this option will only be able to attend the workshop during the day.

DSP Fundamentals

Full-day workshop
Length: 5 hours 45 minutes
Time: 9.30-17.30

Module title:
DSP: Theory, Algorithms and Applications

Target audience:
For anyone new to DSP or not familiar with the technology.

Speaker: Drs. Bob Stewart S& Stephan Weiss, University of Southampton

Abstract
In the last ten years DSP has emerged as an enabling technology for a wide range of applications such as modem communication, adaptive beamforming, digital telephony, multimedia, high fidelity audio, video compression, mobile telephony and so on. DSP is now a technology with a vast array of current applications; it is therefore a technology that should be fundamentally understood and appreciated by a very wide and diverse audience of engineers, scientists, computer programmers, technologists, project managers and so on.

The aim of this course is to educate participants in the theory, algorithms and applications of modern digital signal processing techniques and technology. Participants will be presented with the core theory and algorithms of DSP and be given demonstrations of real time TI based digital signal processing strategies.

Module agenda:
Signal Processing Review
- – Signals, Systems and Applications
- – Amplification, distortion, and noise
- – The 90s DSP Revolution to Software Radio in 2000

The Generic DSP System (Review)
- – ADCs and DACs / Signal Conditioning
- – Anti-alias and Reconstructions Filters
- – Distortion, Quantisation Error and Noise
- – The Nyquist Sampling Rate
- – z-domain representation and transforms

Frequency Domain Analysis
- – Periodic, aperiodic and random signals
- – The DFT, FFT and Power Spectra
- – Spectral Leakage and Data Windowing
- – Modern spectral analysis
- – Time/Frequency Representation

Digital Filtering Introduction
- – FIR Digital Filter Design Parameters and methods
- – Poles and zeroes
- – IIR Digital Filters
- – All-pass, CIC, MA, ARMA, comb filters etc…Bit true simulations

Adaptive DSP Algorithms
- – Least squares (LS) minimization

– Least mean squares (LMS)
– Channel equalisation / Inverse system identification
– Echo Control for feedback suppression
– Acoustic echo control / noise control

DSP Software/Hardware

– Processor architecture overview
– DSP vs ASICs/FPGAs
– Pipelined execution and MAC operations
– Assembly instructions
– C compiler
– Simulation based design / compilation
– FIR filter design example
– Adaptive filter design example

Speaker information:

Dr. Bob Stewart
University of Strathclyde

Dr Bob Stewart is currently faculty in the Department of Electronic and Electrical Engineering at the University of Strathclyde, UK. Prior to joining University of Strathclyde, Dr Stewart was a visiting Professor in Department of Electrical Engineering at the University of Minnesota in 1990, and a visiting scholar at the University of Southern California in 1986/7. More recently in 1997/98 he was appointed a part-time Visiting Professor at the University of California, Los Angeles. In 1999 Bob worked on a Royal Academy of Engineering Industrial Secondment scheme with Entegra Ltd, and its customers.

Bob Stewart's general research interests are in the areas of adaptive signal processing and digital communications, particularly 3G DSP strategies. Current research projects in Dr Stewart's research group include work on adaptive channel equalisation, adaptive receiver techniques for multi-user communications (CDMA), oversampling strategies for sigma delta ASICs, sub-band strategies for acoustic echo control, multimedia integration of DSP educational tools and LPC strategies for speech coding. Dr Stewart's current work is funded by a number of companies and agencies including the Engineering and Physical Sciences Research Council and Motorola. Dr Stewart has consulted on digital signal processing to companies including British Telecom, Motorola, Ericsson, GEC-Plessey Telecommunications, Lucent, Marconi Instruments, Racal, the BBC, Robert Bosch and a number of DSP technology start-up companies.

Bob Stewart is also the presenter of the European DSP Foundation Course which, since its inception in 1994, has been presented to more than 900 attendees in Europe and the USA. Over the last 10 years Dr Stewart has published more than 130 technical papers, one textbook and is the author and designer of the DSPedia CDROM, and of the CompanionCD for the textbook Digital Communications by Bernard Sklar (Prentice Hall, 2001). Dr Stewart is a Chartered Engineer, and a member of the IEEE and the IEE. He is also a member of the EURASIP ADCOM committee.

Dr. Stephan Weiss
University of Southampton

Dr Stephan Weiss (Dipl.-Ing. 1995, University of Erlangen-Nuernberg, Germany, PhD 1998, University of Strathclyde, Glasgow, Scotland) is a lecturer in the Communications Group, Department of Electronics and Computer Science, University of Southampton, since 1999 and a part-time visiting faculty at the University of California, Los Angeles (UCLA) extension school since 1998. Prior to his appointment at ECS, he was a visiting lecturer at the University of Strathclyde in 1998/99, and a visiting scholar at the University of Southern California in 1996/97. His research interests are mainly in adaptive and multirate signal processing and find applications in communications, audio, and biomedical areas. Funded by EPSRC, QuinetiQ Ltd, Samsung (UK), and the University of Southampton, Stephan Weiss manages a research group working on fast converging and numerically efficient techniques for adaptive equalization and beamforming, as well as on various aspects of software defined radios. He has 60 technical publications, including a book, received the 2001 research award of the German hearing aid society, and is a member of the IEEE and the VDE.