Application Report
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Latch-Up, ESD, and Other Phenomena

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ABSTRACT

The engineer designing an electronic system often needs to know the behavior of its components under operating conditions that are outside those usually described in the data sheets. Thus, although the latch-up effect is no longer a problem with modern CMOS circuits, a closer look at this phenomenon makes it easier for the engineer to assess realistically the risks that may arise under specific – perhaps extreme – operating conditions. The electromagnetic compatibility of integrated circuits, as well as their sensitivity and immunity to these effects, plays a significant role. Under particular operating conditions, parasitic transistors in integrated circuits can jeopardize the correct function of a component. This application report discusses latch-up, electrostatic discharge (ESD), and other phenomena, and their relationships, thereby providing designers information needed to assure the functional security of the system, even under extreme operating and environmental conditions.

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1 Introduction

When a customer buys an integrated circuit – a gate or an operational amplifier – from a semiconductor manufacturer, it contains considerably more transistors and diodes than are necessary for the basic function. The additional components, such as the clamping diodes on the inputs and outputs of logic circuits, are required to ensure reliable operation under particular conditions. These components limit the overshoots and undershoots resulting from line reflections and, thus, reduce signal distortion. Also, protection circuits, which are intended to protect the component from destruction as a result of electrostatic discharge, are provided.

In addition to these intentionally integrated additional components, an integrated circuit also contains a number of transistors and diodes that inevitably result from the construction and manufacture of the semiconductor circuit. These components are called parasitic transistors and diodes. Under normal operating conditions, as specified in the data sheets, such parasitic components have no influence on the function of the circuit. However, in particular situations, these parts of the circuit suddenly and unexpectedly can become active, and threaten the correct operation of the complete system. Therefore, the development engineer who uses integrated circuits also must be acquainted with the behavior of parasitic components. Only then can a circuit be designed with the necessary protective precautions that ensure reliable operation under required environmental conditions. Parasitic effects are discussed in the following sections to help design engineers understand these phenomena and, if necessary, take suitable precautions to prevent undesirable behavior by the integrated circuit.

2 Latch-Up

2.1 Parasitic Thyristors

Isolation of the individual diodes, transistors, and capacitors from each other in an integrated circuit is achieved by reverse-biased P-N junctions. During the development of the circuit, precautions are taken to ensure that these junctions always are reliably blocking under the conditions that can be expected in the application. However, these P-N junctions form N-P-N and P-N-P structures with other adjacent junctions. The result of this is parasitic npn or pnp transistors, which can be undesirably activated. The current gain of these transistors is usually very small (ß < 1). As a result, considerable input current is usually necessary to activate these transistors. With sensitive analog circuits, interference and other undesirable effects can occur. Also, the transit frequency of these transistors is comparatively low ($f_T \approx 1$ MHz), which means that very short pulses are not able to turn on such transistors.

A typical example for the undesirable interaction between various P-N junctions is the well-known phenomenon of latch-up, which can occur with CMOS circuits and with BiCMOS circuits that have similar structures: a thyristor formed from parasitic transistors is triggered and generates a short-circuit in the circuit. Figure 1 shows the arrangement of the P- and N-doped regions in a CMOS circuit. For clarity, one structure is shown with incorrect proportions. This circuit represents a simple inverting amplifier.

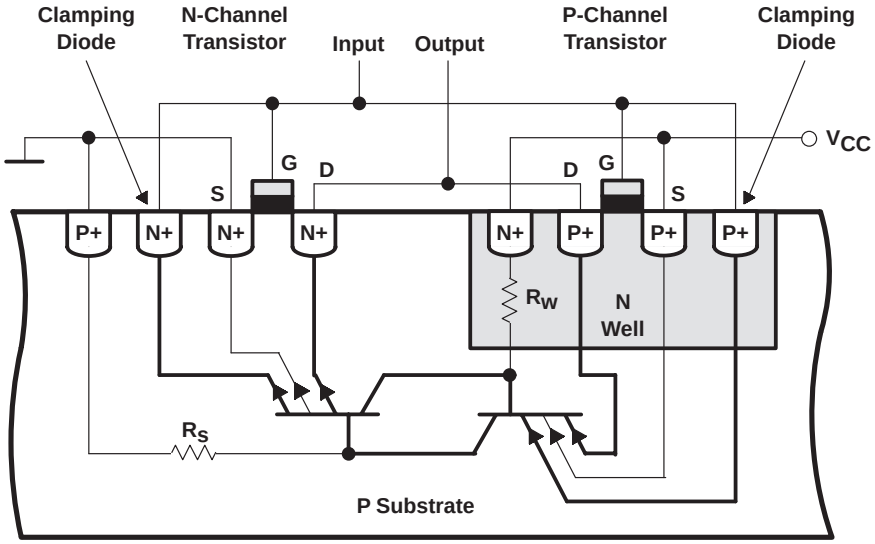

Figure 1. Parasitic Transistors in a CMOS Circuit

In this example, the N-doped regions for source and drain of the N-channel transistor and the cathodes of the clamping diodes have been diffused into a P-doped substrate. The substrate is connected to the most negative point in the circuit, usually the ground connection (GND). In normal operation, the N-doped regions have a voltage that is more positive than the ground connection. In this way, these P-N junctions are blocking. The substrate now forms the base of a parasitic npn transistor, while all N-doped regions – that is, the drain and source of the N-channel transistor and cathode of the clamping diodes – function as emitters. The collector belonging to this transistor forms the well in which the complementary P-channel transistor is located. The latter, with its connections, forms a parasitic pnp transistor. The npn and pnp transistors form a thyristor, as shown in Figure 2. The anode and cathode of this thyristor are connected to the supply voltage of the integrated circuit, while all other points – inputs and outputs – function as the gate of the thyristor. As long as the voltages on the latter connections stay more positive than the ground connection and more negative than V_{CC}, correct operation occurs. The base-emitter diodes are blocking.

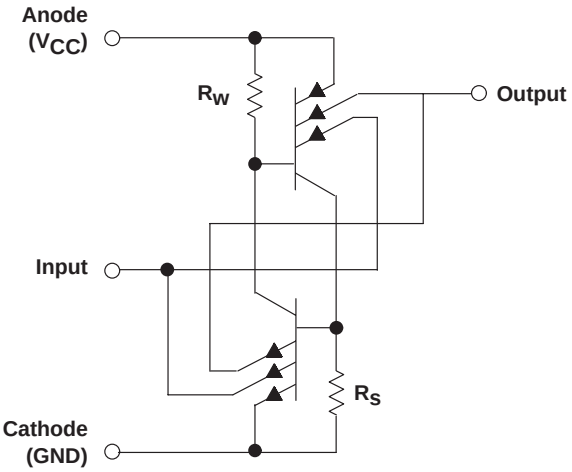

Figure 2. Parasitic Thyristor in a CMOS Circuit

A parasitic thyristor of this kind in an integrated circuit can be triggered in various ways:

- If there is a voltage at the input or output of a circuit that is more positive than the supply voltage, or more negative than the ground connection (or, to be precise, more negative than the connection to the substrate), current flows into the gate of the thyristor. If the amplitude and duration of the current are sufficient, the thyristor is triggered. The transit frequency of the parasitic transistors is only about 1 MHz. For this reason, overvoltages and undervoltages with durations of only a few nanoseconds, such as result from line reflections along the connections on circuit boards, usually are not able to trigger the thyristor. With lines of several meters in length and overshoots of correspondingly longer duration, the probability that the thyristor might be triggered must be taken into account. This applies also at the interfaces between a circuit and the outside world; unacceptable overvoltages also often occur at this point.

- An electrostatic discharge can trigger the parasitic thyristor. Even if the electrostatic discharges have a duration of only a few tens of nanoseconds, when this happens, the complete chip may be flooded with charge carriers, which then flow away slowly, resulting in the triggering of the thyristor.

- The parasitic thyristor can be triggered by a rapid rise of the supply voltage. This effect often was observed in earlier generations of CMOS circuits.
- Additionally, the thyristor might be triggered by a high supply voltage – far higher than the value given in data sheets. In this case, the supply voltage must be increased up to the breakdown voltage of the transistors. When in breakdown, the current in the parasitic transistors, which should be blocking, increases in an avalanche process, so that activation of the thyristor must be anticipated.
- Also, latch-up can be initiated by ionizing radiation. This is important with components that operate close to a source of high-energy radiation.

After the triggering of the thyristor, various reactions can be observed:

- The parasitic thyristor triggers very rapidly and enters a very low-resistance state. The source of the supply voltage is short circuited as a result of the circuit that has been affected. A very high current flows, which, in a very short time, leads to destruction of the component. The thyristor can be switched off again only by switching off the supply voltage. Therefore, the recommendation in the literature is that a resistor should be placed in series with the supply voltage connection to the integrated circuit. If the thyristor does trigger, this resistor limits the current to a value that no longer poses any danger to the device. If possible, the resistor should limit the current to a value below the holding current of the thyristor such that, after the end of the conditions that led to its being triggered, the thyristor automatically switches off.
- The thyristor triggers in the manner previously described, but, in this case, the thyristor has a comparatively high forward resistance. The result is that only the supply current increases, but this increase usually is quite large. Because of the high power dissipation in the circuit, the component can be damaged. The thyristor usually switches off only after the supply voltage has been switched off.
- In some cases, the thyristor has a very high resistance. The high forward resistance limits the current to values below the holding current of this thyristor. In this case, the supply current increases. The supply current sinks to normal values when the trigger current at the gate of the thyristor (as a result of an overvoltage at the input or output of the integrated circuit) is switched off.

2.2 Precautions to Be Taken Against Latch-Up

Semiconductor manufacturers have worked to avoid latch-up of CMOS circuits, and various precautions can be implemented. First, the conflicting components can be located as far as possible from each other. This reduces the current gain of the parasitic transistors, and the triggering sensitivity of the thyristors is reduced. However, these precautions achieve only limited success because, for reasons of space and cost, the distance between the conflicting components can be increased only to a certain limit. On the other hand, the continuous process of reduction in the geometries of semiconductor circuits works in the opposite direction. Therefore, other remedies that combat latch-up are necessary, including surrounding the critical parts of the circuit with guard rings (see Figure 3).

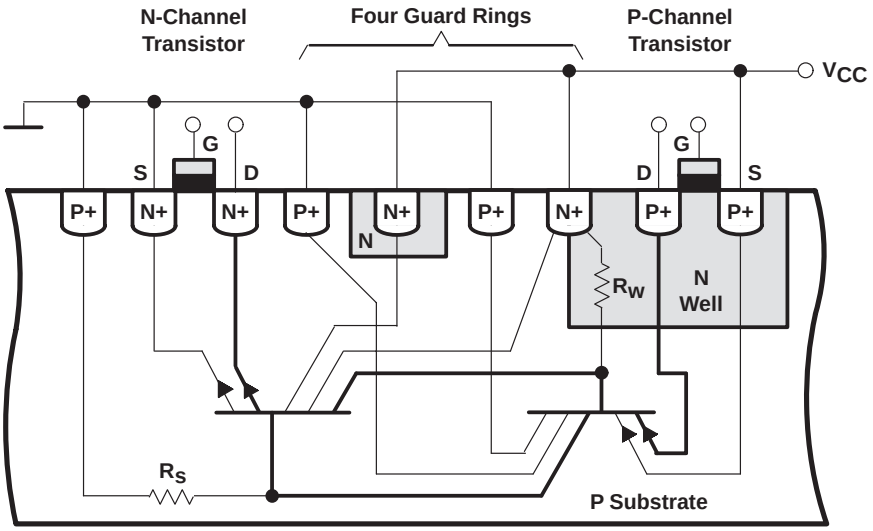

Figure 3. Guard Rings in a CMOS Circuit

These guard rings form additional collectors for the parasitic transistors. Such collectors are connected either to the positive or negative supply-voltage connection of the integrated circuit. These additional collectors are placed considerably closer to the base-emitter region of the transistor in question than the corresponding connections of the complementary transistor. As a result, the charge carriers injected into one of the two transistors is diverted largely via these auxiliary collectors to the positive or negative supply-voltage connection. These precautions do not completely eliminate the questionable thyristor. However, the thyristor's sensitivity is reduced to such an extent that, under normal operating conditions, there should be little risk of triggering the thyristor.

2.3 Latch-Up Test

After designing an integrated circuit, the first samples of the new device are subjected to intensive testing. All relevant parameters are measured – many more than those included in the data sheets. The latch-up sensitivity of CMOS and BiCMOS circuits also is examined, using the test circuit shown in Figure 4. The maximum permissible supply voltage is applied to the circuit, then current is injected for a certain duration into each input and output. During this test, the supply current of the device under test must not rise.

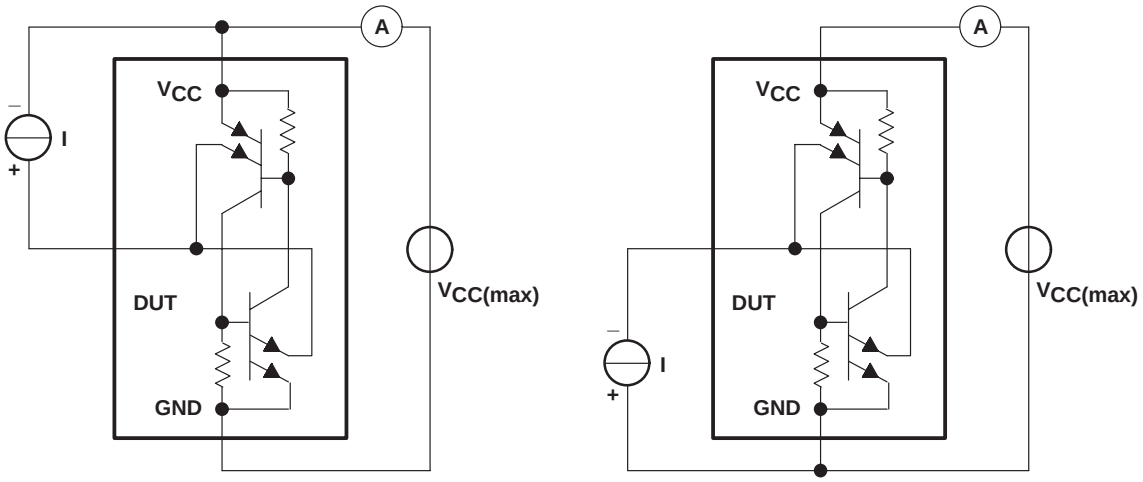

Figure 4. Latch-Up Test Circuit

Measurement conditions are different for various types of circuits. For example, logic circuits of the SN54/74 families are subjected to a current of 300 mA to 500 mA for 10 μs at an ambient temperature of 125°C. These test conditions should comprehend the worst-case operating conditions. The parasitic transistors in the integrated circuit are bipolar components. The current gain of such devices increases with temperature and, thus, also the sensitivity of the thyristor that is to be tested. A test pulse duration of 10 μs should ensure that the questionable thyristor is triggered, if this is possible. As previously mentioned, the transit frequency of the parasitic transistors is very low. Thus, significantly shorter pulses cannot provoke a reaction from the circuit. The amplitude of the current is used to assess the worst-case conditions under which the circuit can be operated. Overshoots and undershoots caused by line reflections can – in theory – give rise to currents of up to 100 mA in the clamping diodes (see Section 4.3). At the interfaces to the outside world, under certain circumstances, even higher currents can occur. Additional investigations have shown that, at room temperature, currents of 1 A to 2 A typically are needed to cause latch-up. The test conditions described are potentially destructive, meaning that devices tested in this way must not be delivered to customers. The high current density during this test might permanently damage the device.

At final test, LinCMOS devices are tested individually for latch-up sensitivity. To avoid damage to the components, a current of only 100 mA is injected into the device under test. Because analog components, such as operational amplifiers, usually operate in a considerably higher-resistance environment compared to digital circuits, these test conditions are sufficient to cover conditions likely to occur in practice.

The characteristics of modern CMOS and BiCMOS circuits described here meet practically all the requirements, with respect to insensitivity to latch-up, that are likely to occur in practice. Only in a very few cases would the development engineer need to take additional precautions.

2.4 Pseudolatch-Up

In addition to the essential meaning of latch-up, as described previously, this term also is used commonly for a number of other phenomena, even though, in such cases, latch-up in its classical sense is not involved. Because, in certain applications, effects of the other phenomena also can cause serious problems, they are discussed in more detail in the following sections.

2.4.1 Pseudolatch-Up With Analog Circuits

If a voltage that is applied to the inputs of an operational amplifier or comparator lies outside the range given in the data sheet for common-mode operation, the input stage of the circuit may be put into a state that results in unpredictable behavior. See Figure 5 and the following paragraph for a discussion of this behavior.

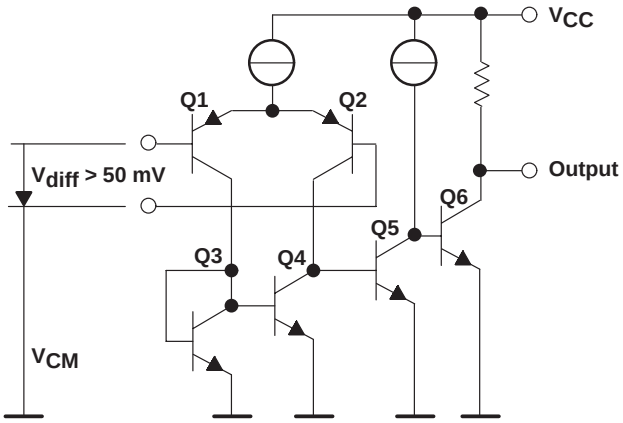

Figure 5. Simplified Circuit of a Differential Amplifier

The initial assumption is that the difference in voltage between the two inputs is V_{diff} = 50 mV, whereby the voltage on the base of transistor Q1 is more positive than that on the base of transistor Q2. It also is assumed that the two voltages are within the permissible common-mode range (0.3 V ≤ V_{CM} ≤ V_{CC} – 1 V). Under these conditions, transistors Q1, Q3, and Q4 are blocking, Q2 and Q5 are conducting, and output transistor Q6 is blocking. Consequently, a voltage level at the output is reached that corresponds to the supply voltage, V_{CC}. If the common-mode voltage, V_{CM}, is raised by more than approximately V_{CC} – 1 V, the base-emitter voltage available to transistor Q2 is no longer sufficient to cause a base current to flow. Because the current flow in transistor Q2 is interrupted, Q5 also switches off. Output transistor Q6 becomes conducting, and a voltage level at its collector is reached that no longer conforms to the required potential difference at the input of the amplifier. This sudden and unexpected behavior of the circuit sometimes is called latch-up, even when this effect has nothing to do with the phenomenon described in Section 2.1. A defined state of the circuit again is reached at the instant when the voltage at the inputs returns to a value within the recommended range of input voltage. However, with certain complex operational amplifiers, the internal circuitry might become latched under the input conditions described in this paragraph. In this case, a reduction of the input voltage no longer results in the correct operation of the circuit; on the contrary, the supply voltage first must be switched off to reactivate the amplifier. However, this is not the basic phenomenon of latch-up.

2.4.2 Pseudolatch-Up With Bipolar Transistors

Another phenomenon, also called latch-up, occurs with bipolar transistors, particularly with output transistors carrying high currents. Figure 6 shows the output characteristics of a bipolar transistor in which the load resistor also is represented. The data sheet for the transistor includes, among other characteristics, the maximum collector current $I_{C(max)}$ and the breakdown voltage V_{CEO} of the transistor. These two figures can be assumed to define the limits of the permissible safe operating area of the transistor.

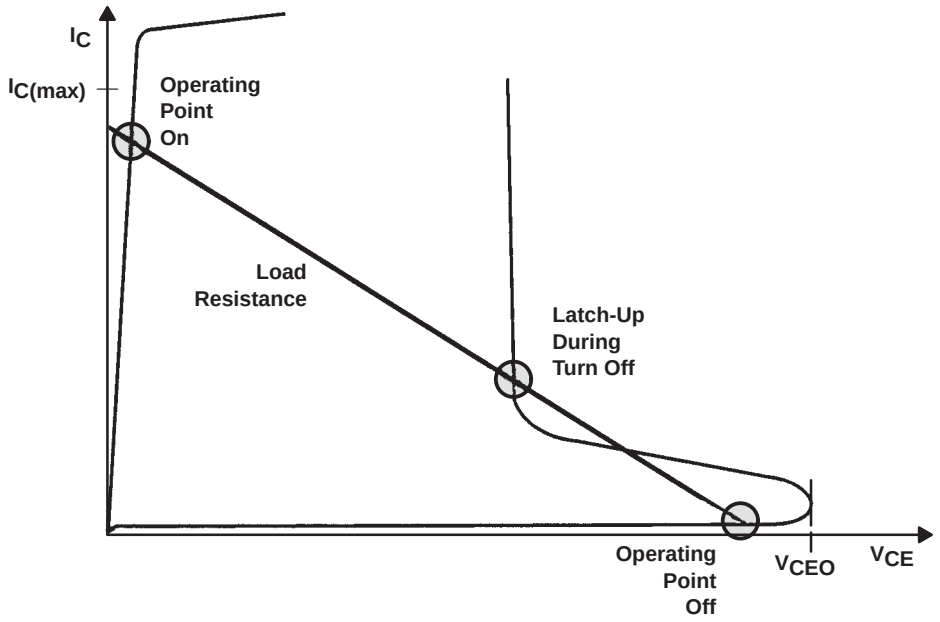

Figure 6. Output Characteristics With Load Resistor

A detailed analysis of the breakdown characteristics of the transistor reveals that, when the transistor is in breakdown, the breakdown voltage decreases with increasing collector current. If a low resistance is drawn in on the diagram, this intersects the corresponding output characteristics, not only at the desired on and off points, but also at a third intersection of the breakdown characteristics with the load resistance. This is not critical when the transistor is switched on fast, although, in this case, the breakdown characteristics are exceeded briefly. During this transition, the transistor acquires an increasingly low resistance; therefore, the working on point is defined reliably. The behavior is very different when the transistor is switched off because it travels along the load resistance line in the direction of off. During this journey, the transistor intersects the breakdown characteristics as it becomes increasingly resistive. At this point, the transistor hangs up: the term commonly used is, again, latch-up. A considerable collector current flows while there is a high collector-emitter voltage. The result is high power dissipation which, in turn, causes a high chip temperature and results in accelerated aging (and even destruction) of the component.

It often is difficult to detect this situation with commonly used measurement techniques. If contact is made to a point connected to the collector using the test probe of a voltmeter, or with the probe of an oscilloscope, which usually has a much lower capacitance, the effect mentioned above no longer can be observed. When there is capacitive loading, the switch-off curve no longer is a straight-line resistance characteristic but, instead, is a hyperbola. The capacitance at the output first prevents a rise of the collector voltage, while the collector current already is falling. As a result, the critical point is avoided.

This kind of latch-up can be avoided effectively only by choosing transistors that have sufficient reserve in the breakdown region. Texas Instruments frequently specifies in data sheets of interface circuits a latch-up-free region in which the output transistor can be operated without danger to the device. For example, with the power drivers in the SN75471 family, the data sheet gives a maximum collector voltage in a blocking state (off-state output voltage) of V_O = 70 V. This value corresponds approximately to the voltage V_{CEO} in Figure 6. Because of the behavior in breakdown of the transistor described above, latch-up-free operation is specified only with an output voltage of $V_{CE(max)}$ = 55 V and a collector current of $I_{C(max)}$ = 300 mA.

3 Electrostatic Discharges

Electrostatic discharges constitute a danger for integrated circuits that never should be underestimated[1]. Electrostatic charging can occur as a result of friction, as well as for other reasons. When two nonconducting materials rub together, then are separated, opposite electrostatic charges remain on both. These charges attempt to equalize each other. A common example of the generation of such charges is when one walks with well-insulated shoes on a carpet that is electrically nonconducting, causing the body to become charged. If a conducting object is touched, for example, a water pipe or a piece of equipment connected to a ground line, the body is discharged. The energy stored in the human body is injected into the object that is touched, and is converted primarily into heat. The power dissipation that arises in such cases can destroy sensitive electronic circuits.

Even though the semiconductor industry has increased efforts to protect components against destruction as a result of electrostatic discharges, usually it is not possible to provide adequate protection in every conceivable situation. Test circuits have been developed to test sensitivity to electrostatic discharges by simulating various scenarios. These test circuits are analyzed in more detail in the following paragraphs. These should provide the design engineer with insight into the reliability of these tests and the effectiveness of the individual protection circuits, providing the criteria to decide, in individual cases, whether additional precautions are necessary.

3.1 Human-Body Model

The human-body model is described in MIL-STD-883B. The test is a simulation, in which the energy stored in a human body is discharged into an integrated circuit. The body is charged as a result of friction, for example. Figure 7 shows the test circuit. In this circuit, a capacitor (C = 100 pF) is charged through a high-value resistor to ±2000 V, then discharged through a 1.5-kΩ resistor into the device under test.

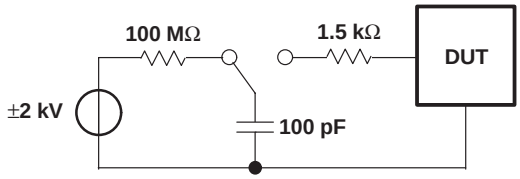

Figure 7. Human-Body Model Test Circuit

The 100-pF capacitor simulates the capacitance of the human body. However, the actual capacitance of the human body is between 150 pF and 500 pF, depending on size and contact area (shoe size). Also, the 1.5-kΩ value of the discharge resistor must be considered. The internal resistance of the human body ranges from a few kilohms to a few hundred kilohms, depending on various factors, which include the humidity of the skin. However, if the discharge takes place through a metallic object, such as a screwdriver, the discharge resistor can be assumed to be a few tens of ohms. For these reasons, the corresponding Standard IEC 802-2 prescribes a test circuit with a capacitance of 150 pF which, in practice, is more realistic and a lower value of discharge resistor (R = 330 Ω). This standard is, however, concerned with a test specification for equipment that is not directly applicable to integrated circuits. Using a value of 2000 V also is questionable because, when a discharge causes a tingling in the tips of the fingers, the body has been charged to at least 4000 V.

The energy of about 0.4 μWs that must be dissipated in the actual protection circuit is comparatively small. The major part of the energy stored in the capacitor is converted into heat in the discharge resistor. A considerably more-important parameter in the test, according to this method, is the rise time of the current during the discharge. Standard IEC 802-2 prescribes a rise time of about 0.7 ns at the actual location of the discharge. This value is of interest because, with a fast discharge, at the first instant only a small part of the protection circuit conducts. Only during the subsequent phase (a matter of nanoseconds) does the current spread over the complete conducting region of the protection circuit. Therefore, during the first moments of the discharge, the danger of a partial overload of the protection circuit exists. A similar effect can be observed with thyristors and triacs. With such components, the rate of current rise after triggering must be limited because, at first, only a small area of the semiconductor near the trigger electrode is conducting. A high current density can result in the destruction of the component. This effect is, however, in many cases responsible for the fact that, even with discharges from considerably higher voltages, the destruction of the circuit does not necessarily occur. The point at which the discharge occurs usually is not at the connections to the integrated circuit, but, instead, to the cabinet of the equipment or to the contact of a plug. Between this point and the endangered integrated circuit there is a length of conductor that has significant inductance. This inductance slows the rate of rise of the current, and helps ensure that the discharge current is spread evenly over the complete protection circuit.

3.2 Machine Model

The test using the machine model simulates the situation in machinery or other equipment that contains electronic components or modules. The casing of such equipment is constructed largely of metal, but often contains plastic bearings or other parts having a wide variety of shapes and sizes. When individual parts of the machine are in motion, these plastic bearings can generate electrostatic charges. Figure 8 shows the test circuit. In this test, a C = 200-pF capacitor is charged to ±500 V, then discharged, without a series resistor, into the device under test.

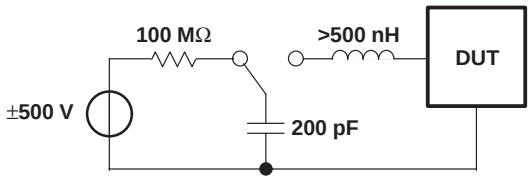

Figure 8. Machine-Model Test Circuit

Because the charged metal parts have a very low electrical resistance in this test circuit, no series resistor is used to limit the current. Therefore, the peak current in the device under test is significantly higher than in the previously described human-body test circuit. Whereas, in the human-body test circuit, extremely short rise times are required, as a result of the extremely low inductance of the construction used, considerably higher inductances of 500 nH are specified in the discharge circuit of the machine model. As a result, the rise time of the current and, consequently, its amplitude, are limited. Therefore, the problem of the partial overload of the protection circuit of the device under test is reduced significantly. The energy of 4 μWs to be dissipated is considerably higher than in the machine-model test.

Because of the high energy used in this test, integrated circuits usually cannot be tested with voltages of 500 V without damaging the device under test. As a guideline, assume that components that survive, without damage, the human-body model test with a voltage of up to 2000 V, also are not damaged by a machine-model test using voltages of up to ±200 V.

3.3 Charged-Device Model

Despite the informative tests conducted according to the methods described in the previous sections, in practice, damage due to electrostatic discharges also can occur during the processing of integrated circuits. It has not been possible to reproduce the profile of failures observed during processing by using normal test equipment. Intensive investigations show that electrostatic charging, and consequent discharging, of the device are responsible for the damage. Charging occurs when the integrated circuit slides along plastic transport rails before being inserted into circuit boards, and the discharge occurs when the component lands on the circuit board. Similarly, damage to the component can occur after it has been tested, when it slides from the test station onto the transport rail, and is damaged by the electrostatic charging that occurs. During testing, the integrated circuit was without fault, but it was damaged immediately afterward. Because the device package is small, the capacitances are only a few picofarads, but the inductances also are extremely low (see Figure 9).

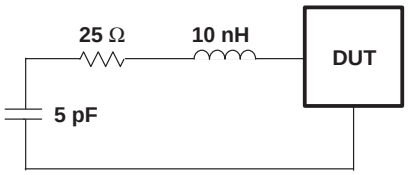

Figure 9. Equivalent Circuit of Discharge of the Charged-Device Model

Therefore, in this case, still shorter rise times (<200 ps) of the current can be expected. Because the protection circuit is only partially conducting, damage to the circuit can result. The simplified test setup is shown in Figure 10.

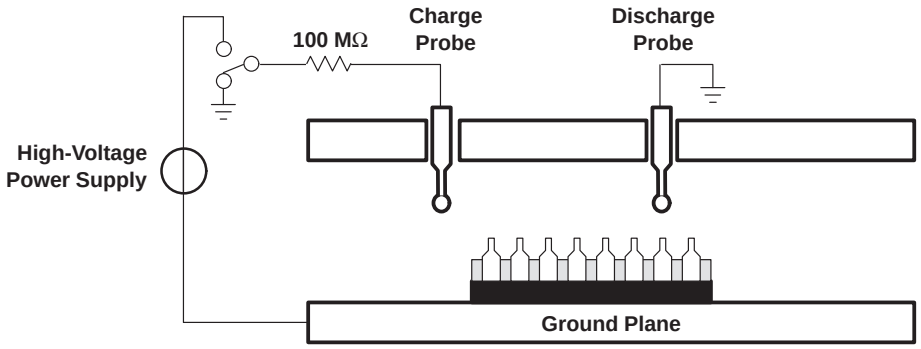

Figure 10. Charged-Device Model Test Setup

The device under test is placed on its back on a metal plate. In this way, the largest possible capacitance of the circuit to the environment is attained. The circuit is charged with a moveable charging test probe and discharged with a second test probe.

Investigations have shown that integrated circuits in this test that survive charging up to 1000 V and subsequent discharging without damage, can be processed without problems in assembly machinery if the usual precautions to prevent electrostatic charging are taken. There is no correlation between the results of the human-body and charged-device model tests. Components that survive the human-body model test without damage do not necessarily behave in the same way in a charged-device test. Conversely, a successful charged-device model test gives no indication of results when a component is tested according to the human-body model.

3.4 Charged-Cable Model

The three test methods discussed previously have their justifications, but they do not cover all situations that might arise. A typical problem that occurs with the use of electronic equipment is related to inserting connectors attached to cables. If a user walks on a nonconducting floor with the plug on the end of a 10-m cable in their hand, the person's body and the cable become charged. When the plug is inserted in the socket of a piece of equipment, the capacitance of the cable is discharged. The capacitance of a 10-m cable is about 1000 pF, producing a charging voltage of up to 1000 V. The 500 μWs of energy, which must be tolerated by the integrated circuit, is many times larger than in the tests described previously. The discharge current, which is determined by the line impedance of the cable (typically 100 Ω), is about 10 A. This current flows for a time corresponding to two signal-propagation times, namely, 100 ns. However, because of the comparatively high inductances of the connector and the line connected to it within the equipment in question, no exceptionally steep current-pulse edges arise. The problem of the partial conduction of the protection circuits is, to a large extent, eliminated. Therefore, it is possible to integrate protection circuits that survive such conditions without damage. The differential line driver and receiver interface device SN75LBC184 is a good example of a design that protects against damage due to electrostatic discharges.

3.5 ESD-Protection Circuits

ESD-protection circuits were first integrated into CMOS devices. The thin and, therefore, very vulnerable gate oxide of the MOS transistor makes protection against destruction as a result of electrostatic discharges essential. The protective precaution that was taken initially, and which is still the best method, is the integration of clamping diodes, which limit the dangerous voltages and conduct excess currents into regions of the circuit that are safe. The safe regions consist primarily of the supply-voltage connections. In the simplest case, the protection circuits consist of diodes that are oriented to be blocking in normal operation, and are situated between the connection to the component to be protected and the supply voltage lines (see Figure 11).

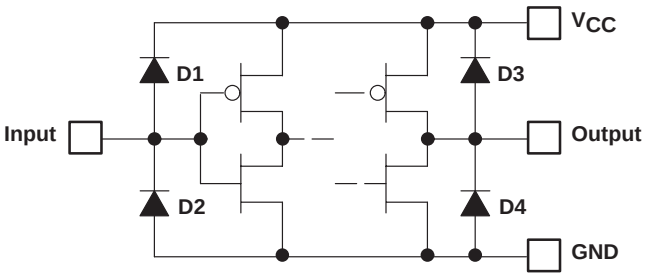

Figure 11. ESD-Protection Circuits Using Diodes

To tolerate even higher energy levels, and to protect the more sensitive parts of a circuit, two-stage protection circuits frequently are used at the inputs (see Figure 12). With this arrangement, the so-called coarse protection should conduct away the higher energy levels. In the example shown, the protective circuit against negative voltages consists of diode D1. Positive voltages are first limited by transistor Q1, which begins to conduct as soon as the input voltage ($V_{in} > V_{dd} + 0.7$ V) allows current to flow through resistor R1. If the input voltage increases further, at about 22 V to 26 V, the thick-oxide MOS field-effect transistor Q2 conducts. Q2 provides additional base current to the base of transistor Q1. In this way, the energy in the interfering pulse is conducted away reliably. The fine protection circuitry, which should protect the next device (primarily the gate oxide of the transistors) from excessive voltages, consists of resistor R2 and Zener diode D3.

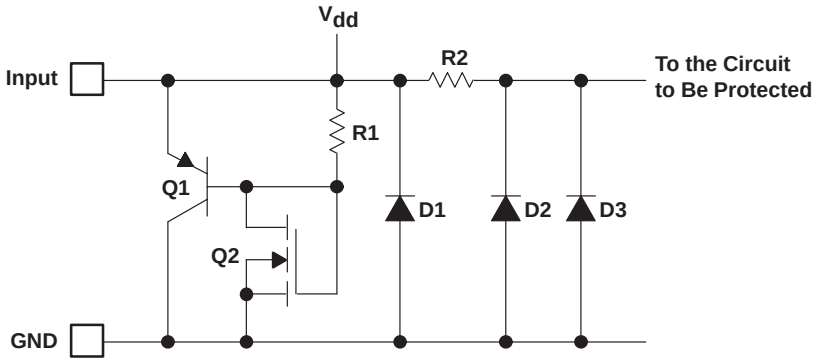

Figure 12. Two-Stage ESD-Protection Circuits

It is not practical to show all kinds of ESD-protection circuits that have been developed for every conceivable circuit configuration. The design of these parts of the circuit depends primarily on the application in which a device is used. Operational amplifiers that have, among other features, very high-resistance input circuits, use different protective circuits than, for example, interface devices for data-communications systems. In such interfaces, robustness of the device is an important characteristic.

3.6 Potentialities and Limitations of Protection Circuits

During design of the circuitry intended to protect an integrated circuit against destruction as a result of electrostatic discharges, the engineer must consider a number of conflicting requirements. The rate of thermal conduction in silicon is only 1 μm/μs. Therefore, the protection circuit must, at first, be able to withstand the total energy. Only later is the generated heat conducted to the surrounding circuit. By using data based on the charged-cable model, the approximate area necessary for a protection circuit that can withstand this stress should be calculated.

The formula for the temperature increase of a body, in this case the active protection circuit, is:

$$\Delta T = \left(\frac{1}{V \times C_s}\right)E \tag{1}$$

Where:

ΔT = Temperature increase
V = Volume of the body to be heated
C_S = Thermal capacitance of silicon = 1.89 Ws/(cm$^3 \times$ K)
E = Injected energy

Assuming that, following a discharge, a temperature increase (ΔT) of 150 K is permissible, and an energy (E) of 500 μWs is injected, thus:

$$150\ \text{K} = \left(\frac{1}{V \times 1.89\ \text{Ws}/(\text{cm}^3\ \times \text{K})}\right)500\ \mu\text{Ws} \tag{2}$$

Therefore, the necessary volume of the protection circuit is:

$$V = \frac{500\ \mu\text{Ws}}{150\ \text{K} \times 1.89\ \text{Ws}/(\text{cm}^3 \times \text{K})} = 1.76 \times 10^{-3}\ \text{mm}^3 \tag{3}$$

The injected energy is converted into heat in the very thin depletion layer of the protection circuit. If a thickness (D) of 2 μm for the depletion layer is assumed, the necessary area (A) of this part of the circuit is:

$$A = \frac{V}{D} = \frac{1.76 \times 10^{-3}\ \text{mm}^3}{2\ \mu\text{m}} = 0.88\ \text{mm}^2 \tag{4}$$

Such areas can be implemented in integrated circuits. However, when the total area of an integrated circuit is only a few square millimeters, this part of the circuit has a significant influence on the cost of the component. Also, large-area protection circuits significantly influence the characteristics of an integrated circuit. The protection circuits increase significantly the input capacitance of the circuit, and cause an increase in the leakage current of the input circuit. Input leakage current is an important consideration, especially for operational amplifiers, in which extremely high-resistance inputs are required. Therefore, the ESD-protection circuit characteristic could be a disadvantage for the intended implementation of a device.

3.7 External Protection Circuits

Despite all the care semiconductor manufacturers take in the development of protection circuits, not every conceivable situation that might arise in practice can be addressed. Users might need to take additional precautions using circuit-design techniques similar to those already discussed. In the example shown in Figure 13, excessive voltages at inputs and outputs are limited by additional diodes D1 through D4. These diodes should have a low forward voltage, even at high currents. If required by the application, this may extend into the range of several amperes. Series resistors R1 and R2 should limit the currents. Usually, there is no difficulty in choosing a suitable resistor for the input circuit. Resistor values of 1 kΩ to 10 kΩ usually are appropriate. In practice, it usually is adequate to use only a high-value resistor, without additional diodes. Together with the input capacitance of the subsequent circuit, the resistor provides a low-pass circuit that sufficiently slows down the fast rise times that can occur with electrostatic discharges. The choice of a suitable resistor at the outputs of the circuit to be protected can be more difficult. An important characteristic of outputs is that they have a low resistance because they are intended to drive heavy loads, for example, long lines. In this case, matching the output resistance to the line impedance is usually a sufficient protective precaution, this being commonly necessary for other reasons. The resulting value of the resistor lies in the range of only 33 Ω to 200 Ω. A resistor of this kind also protects a circuit sufficiently against the kind of disturbances that arise with the charged-cable model.

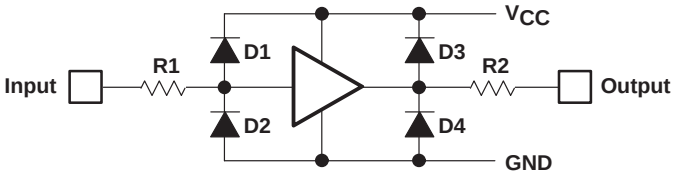

Figure 13. Protection Circuits for Integrated Circuits

The nuclear electromagnetic pulse (NEMP) was considered to be of particular significance at the time of the Cold War, under the threat of the nuclear conflict that might have occurred. As a result of the Compton effect, a nuclear explosion high above the surface of the earth (up to 80 km) would give rise to an electromagnetic pulse that could destroy electrical and electronic installations within a radius of hundreds of kilometers. However, comparatively trivial events also are able to cause similar damage on a local basis. Events of this kind include lightning strikes during a storm (LEMP, or lightning electromagnetic pulse). In close proximity to a lightning strike, voltages of several thousands of volts and currents of many hundred amperes can be induced into nearby conductors. Electronic equipment that should operate in such an environment must be protected from destruction by suitable precautions. Equipment in this category includes telecommunication and data-transmission installations, together with measuring equipment which, because of the functions it performs, may be particularly threatened by phenomena of this nature. It is obvious that the protection circuits previously described are inadequate under these conditions. For applications of this kind, special voltage limiters that can cope with currents and voltages of the magnitude previously mentioned have been developed. Figure 14 shows an example of the protection circuit for the input of an operational amplifier.

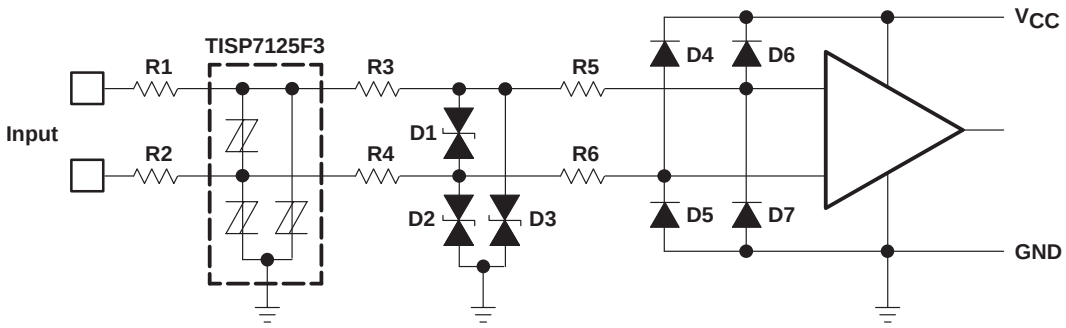

Figure 14. Protection Circuit for Extreme Requirements

Three-stage protection circuits are suitable for applications of this kind. The first limiting stage, consisting of the voltage limiter TISP7125F3, drains away currents on the order of several hundreds of amperes. In the second limiter stage, voltage-limiting diodes D1 through D3 (transient-voltage suppressors) lead off currents in the range of amperes. The third stage of the protection circuit is formed by the diodes D4 through D7. In most cases, at this point, the ESD-protection circuits already included in the integrated circuits are adequate. With the circuit concept shown in Figure 14, the input of the differential amplifier is protected against both unipolar and differential interference. In the mechanical construction of the system circuit, care must be taken in choosing suitable grounding points, so that currents caused by the interference are kept away from the circuit to be protected. The high current-carrying capacity of the conductors allows the use of low values for resistors R1 through R6. Therefore, this circuit concept also is suitable for protecting outputs.

4 Parasitic Transistors in Integrated Circuits

Because the parasitic transistors in CMOS integrated circuits form thyristors, they might be responsible for latch-up of the circuit. Bipolar and MOS circuits also contain additional parasitic transistors which, although not endangering the device, can affect the correct functioning of the circuit. Figure 15 shows a simplified representation of the relationships in a bipolar integrated circuit. A P-doped substrate, which is connected with the most-negative polarity of the voltage supply (GND) to the circuit, contains the N-doped collector of the npn transistor. In this region, the P-doped base and the N-doped emitter are diffused in, one after the other. Beside this transistor is a clamping diode that consists of the N-doped cathode in the P-doped substrate (anode). In addition to these intended components, an unwanted parasitic npn transistor is created, as shown in Figure 15.

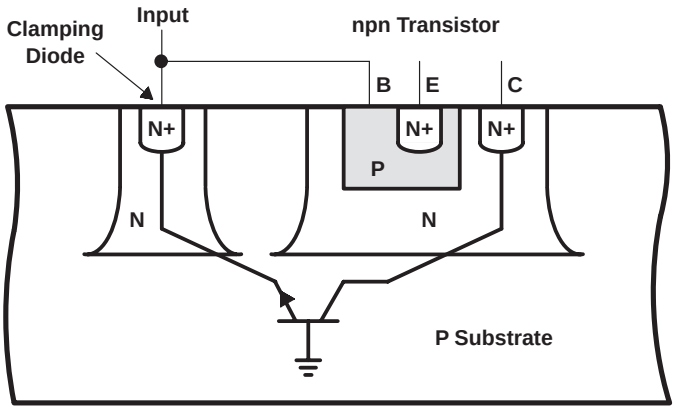

Figure 15. Parasitic Transistors in Bipolar Circuits

Figure 16 shows the complete input circuit, including the parasitic transistor. If a voltage (≈–0.7 V) is applied to the input of this circuit that brings this transistor into a conducting state, an unwanted current flows from the input into the collector circuit of the input transistor.

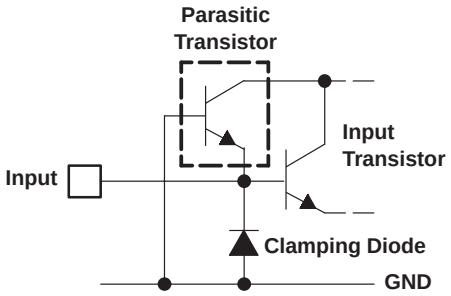

Figure 16. Input Circuit With Parasitic Transistor

The parasitic transistors in CMOS circuits are responsible for the potential latch-up effect that can occur with these components. However, far below the trigger threshold of the parasitic thyristors, the individual parasitic transistors begin to have undesirable effects on the behavior of the integrated circuit. Figure 17 shows the inside a CMOS circuit. A simplified input stage is shown in which the clamping diode, with the P-doped substrate and the N-doped region of an adjacent N-channel MOS transistor, forms a parasitic npn transistor. In this case also, negative voltages at the inputs of the circuit can result in unpredictable behavior by the component. With complementary MOS circuits, parasitic pnp transistors also are in the complementary part of the circuit, and these become active if the input voltage becomes more positive than the supply voltage by an amount equal to their base-emitter forward voltages.

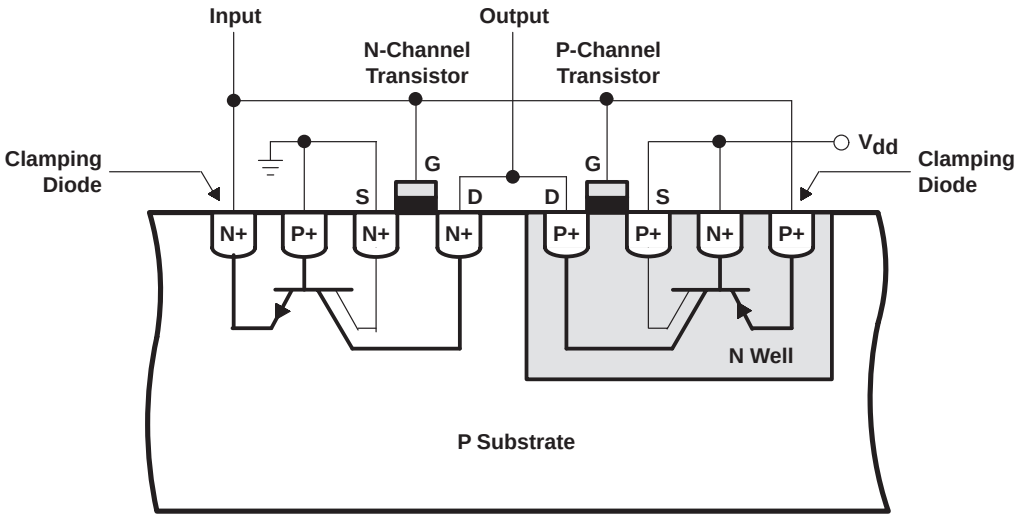

Figure 17. Parasitic Transistors in CMOS Circuits

If the input and output voltages are more positive than the ground connection (GND) and more negative than the positive supply voltage connection (V_{CC} or V_{dd}) to the circuit, as recommended in the data sheet, the parasitic transistors remain switched off. The proper operation of the circuit can be ensured. However, if a voltage that lies outside the previously stated limits is applied to the input of a circuit, the parasitic transistors switch on. Under these circumstances, the correct function of the circuit cannot be ensured. The parasitic transistors shown are only a few of the many in an integrated circuit. Under the conditions described previously, it is easy to provoke any number of undesirable reactions in an integrated circuit.

With analog circuits in particular, this behavior quickly can lead to serious malfunction of the circuit. Usually, analog circuits are constructed to have very high resistance. As a result, even the smallest currents are able to have an adverse influence on, for example, the apparent offset voltage of a differential amplifier. The only effective way to avoid these effects consists of keeping the input and output voltages of a circuit within a range that prevents unwanted switching on of the parasitic transistors. With analog integrated circuits, the data sheets, therefore, specify a range of input voltage:

$$-0.3\ V \le V_{in} \le V_{CC} + 0.3\ V \tag{5}$$

This specification accounts for the fact that the base-emitter diode of a transistor becomes conducting with voltages applied that are significantly less than 0.7 V. However, the base-emitter voltage of a transistor reduces with increasing temperature; therefore, the voltage limits must be considerably narrower.

The semiconductor manufacturer is limited in reducing the influence of the parasitic transistors. Sensitivity can be reduced by situating critical parts of a circuit as far as possible from each other. This results in reduced current gain of the parasitic transistors and, thus, sensitivity of the component. The integration of the guard rings described previously is an additional technique to improve the behavior of the circuit under abnormal operating conditions. However, as already shown, this does not eliminate the parasitic transistors; only their current gain is reduced and, therefore, also the probability that the component could show undesirable behavior under certain conditions.

4.1 Precautions to Protect Analog Circuits

Usually, within a system, it is simple to maintain the required voltage limits, ensuring the correct functioning of the integrated circuits. However, the relationships at the interfaces of the equipment to the outside world often are unpredictable. At these interfaces, significant interference voltages must be expected and, in some cases, may far exceed the limits discussed previously. Nevertheless, correct operation of the equipment must be ensured. The precautions mentioned previously, which should help prevent occurrences, such as destruction resulting from an electrostatic discharge, usually are ineffective at this point. The precautions limit the input and output voltages of the component in question to the extent that damage can be prevented with certainty. However, these protection circuits depend largely on the limiting properties of diodes; therefore, they are unable to prevent an interfering voltage from being generated at the inputs or outputs of the circuit that, briefly, exceeds the required limits. In such a case, attention should be paid less to the interference at the input of an integrated circuit; the output of this channel does, in such a case, show an incorrect result. It is more important to prevent other elements in the component, for example, in a double operational amplifier, from functioning incorrectly. Thus, taking additional precautions is prudent.

The use of silicon diodes is inadvisable because of their high forward voltage (V_f = 0.7 V); also, Schottky diodes (V_f = 0.4 V) cannot be used because of their comparatively high forward voltage. Germanium diodes are the most suitable from the point of view of forward voltage (V_f = 0.3 V), but must be excluded because of their limited temperature range (T_{max} = 90°C) and because they are difficult to obtain. To support applications of this kind, Texas Instruments has made available a special limiter circuit[2] (TL7726). In the TL7726 integrated circuit, the limiting function no longer is performed with simple diodes, but by transistors. By appropriately feeding the bases of these transistors, negative input voltages are limited to values >–0.2 V. Positive input voltages are limited to a value that is <0.2 V more positive than the reference voltage connection (V_{ref}) of this integrated circuit. This connection usually is made to the supply voltage connection of the circuit to be protected. Figure 18 shows the characteristics of this limiter, which is at an extremely high resistance within the working range of the circuit to be protected. Thus, the input current of the limiter, with an input voltage 50 mV ≤ V_{in} ≤ V_{ref} – 50 mV, is less than 1 μA. However, if the input voltage exceeds the value of the reference voltage or goes below ground potential, larger currents also are reliably diverted.

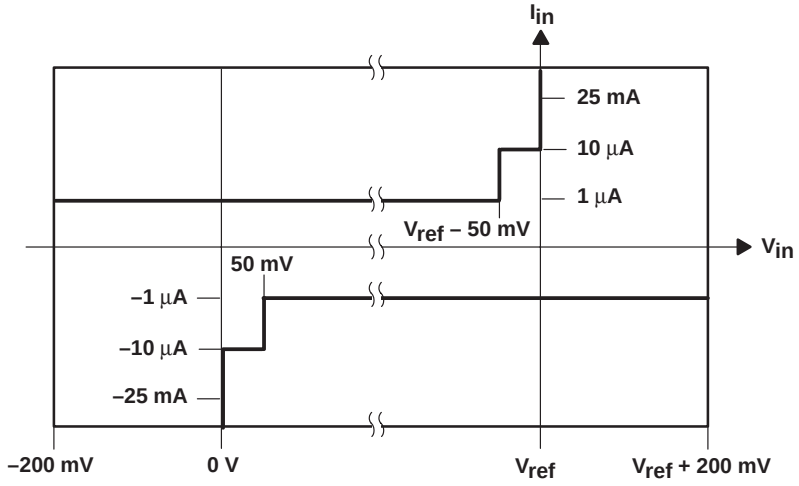

Figure 18. Characteristics of Voltage Limiter TL7726

The operation of this voltage limiter can be explained simply. The voltage limiter is connected in parallel with the inputs of the component to be protected (see Figure 19). In addition, a resistor (R_S) must be inserted in each input line to limit the input current to an acceptable value. There is usually no difficulty choosing a suitable resistor; the high input resistance of modern operational amplifiers and analog-to-digital (A/D) converters simplifies the choice of an appropriate component. However, the limiter circuit has a comparatively high input capacitance which, together with the series input resistance R_S, influences the upper frequency limit of the complete circuit. In addition, digital-to-analog (D/A) converters, which contain a capacitor network in the conversion part of their circuitry, contribute an additional comparatively high input capacitance. This increases still further the low-pass characteristics of the protection circuit. The TL7726 limiter tolerates high peak currents of short duration, making possible the use of low-ohmic-value input resistors.

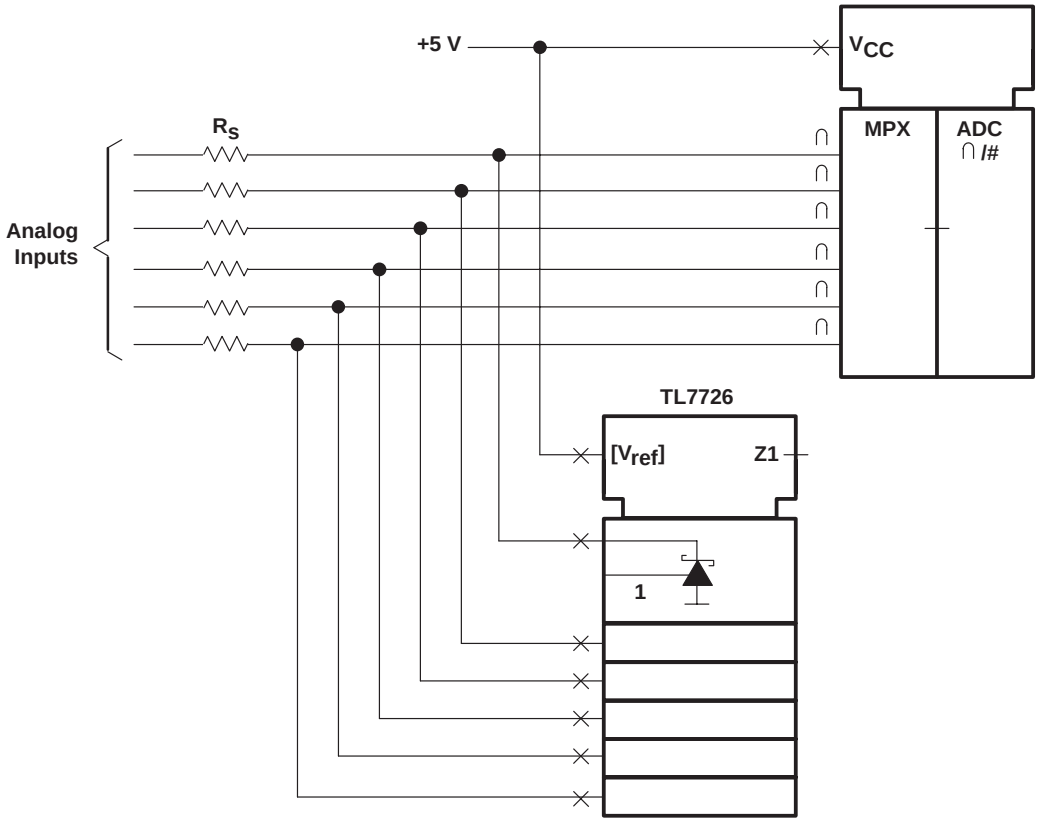

Figure 19. A/D Converter With Limitation of the Input Voltage

4.2 High-Frequency Effects

Analog circuits usually have limited bandwidth. Thus, the transit frequencies (f_T) of operational amplifiers are only a few megahertz. From this point of view, a disturbance to the operation of these components as a result of high-frequency signals should be unlikely. In practice, cases can arise of a disturbance to the circuit as a result of interfering signals, the frequency of which might be several hundred MHz. On closer examination, the component has not been disturbed directly by the high-frequency radiation. Instead, the high-frequency interfering signal that is received by the connection lines that operate as an antenna is rectified by the nonlinear P-N junctions in the semiconductor. These junctions include, for example, the diodes in the protection circuits of the integrated circuits that are affected (see Figure 20). The nonlinear input characteristic of an amplifier can cause it to function as a rectifier for high-frequency voltages or currents as a result of the audion effect. The dc voltage generated at this point can shift the working point of a circuit significantly, putting the correct operation of the circuit into question.

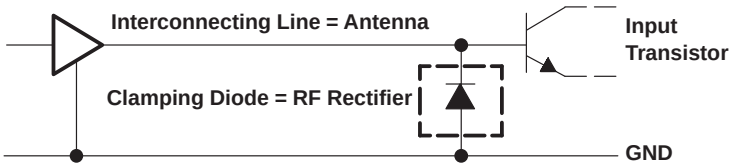

Figure 20. Rectification of High-Frequency Interference Signals

Precautions to counter the effects described here include all possible methods for high-frequency decoupling of critical parts of the circuit. These precautions comprise adequate screening of the sensitive parts of the circuit. Insertion of low-pass filters in sensitive input lines to attenuate high-frequency signals also can be effective.

4.3 Behavior of Logic Circuits

Parasitic transistors also are found in logic circuits, but the danger of a possible malfunction of the component as a result of unintentional switching on of a parasitic transistor is significantly less than with analog circuits. It is not that the parasitic transistors are less sensitive, rather, the high noise margin that is common to all digital circuits is advantageous. Whereas, with analog circuits, even the smallest currents that circulate in the substrate of the circuit can cause serious errors in the output signal, with logic circuits, considerably higher currents are necessary to produce an incorrect logic level. In addition, semiconductor manufacturers take additional precautions in the form of additional guard rings to exclude, as far as possible, the influence of parasitic transistors on the inputs and on the outputs of these devices.

Reflections that occur at the ends of lines that have not been terminated correctly cause overshoots and undershoots at the inputs and outputs of logic circuits. Figure 21 shows the waveforms at the beginning and end of an open-circuit line having a characteristic impedance of Z_O = 50 Ω, which is controlled by an SN74LVT244 device[3]. Because the end of the line is not terminated correctly, large overshoots and undershoots occur at this point. In theory, the amplitude would be double the voltage at the beginning of the line. As Figure 21 shows, reflections produce such overshoots and undershoots at the beginning of the line.

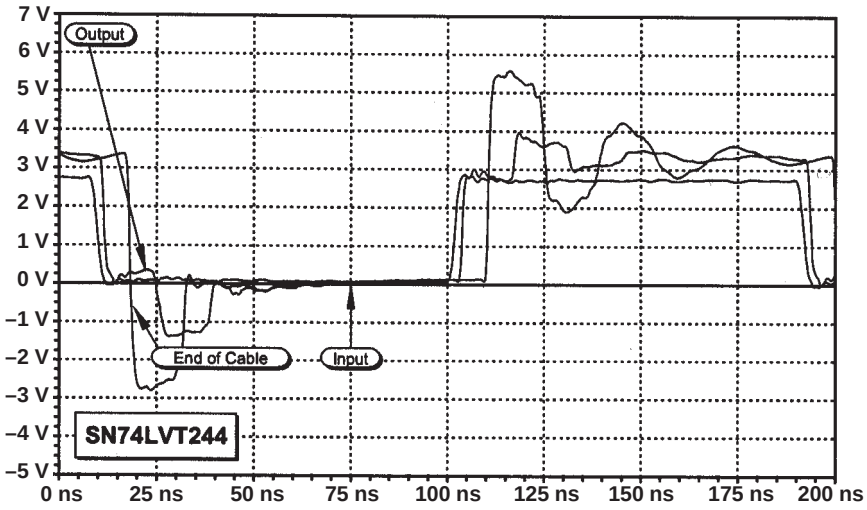

Figure 21. Waveforms on an Open-Circuit Line

In practice, clamping diodes limit the overshoots and undershoots in the integrated circuits to which they are connected. These diodes must be able to pass relatively high currents without compromising the function of the component. The amplitude of current I_D in the clamping diode can be calculated using equation 6.

$$I_D = \frac{2 \times V_{CC} \times \frac{Z_o}{R_o + Z_o} - \left(V_{CC} + V_{fD}\right)}{Z_o + R_{fD}} \quad (6)$$

Where:

V_{CC} = Supply voltage
Z_o = Characteristic impedance of the line
R_o = Internal resistance of the line driver
V_{fD} = Forward voltage of the clamping diode (≈0.7 V)
R_{fD} = Differential resistance of the clamping diode

Without introducing any serious error, it can be assumed that $R_o << Z_o$, and $R_{fD} << Z_o$. This simplifies equation 6 to:

$$I_D = \frac{V_{CC} - V_{fD}}{Z_o} \quad (7)$$

With a supply voltage of V_{CC} = 3.3 V and a characteristic impedance of Z_o = 30 Ω, which are found in typical bus systems, the result is:

$$I_D \approx \frac{3.3\ V - 0.7\ V}{30\ \Omega} \approx 80\ mA \quad (8)$$

Integrated-circuit design engineers lay out the clamping diodes, and the guard rings that surround them, so that currents that flow in the clamping diodes (and thus, inevitably, also in the substrate of the circuit) can be calculated to have approximate values of the magnitude in equation 8 and cause no malfunction of the circuit. This assumes that a switch-on duration of the current of only a maximum of 100 ns with a duty cycle <10% is permitted. This limitation does not affect the logic circuits, because the overshoots and undershoots exist for only a fraction of the period of the wanted signals. The limitation of the switch-on time also makes it possible to keep the area needed for the necessary guard rings within acceptable limits. Because the transit frequency of the parasitic transistors is only about 1 MHz, shorter pulses in the range of nanoseconds are unable to switch on these parasitic transistors. During testing, without powerful pulse generators, a direct-current test usually is performed. A current of I_D = 3 mA is injected into the clamping diodes for a duration of t_d = 10 μs to 20 μs. Extensive investigations show that, with 3 mA/10 μs, this test correlates sufficiently accurately to the assumed operating conditions of 80 mA/100 ns.

5 Summary

An adequate understanding of both the characteristics and the limitations of integrated circuits is necessary to develop a system that operates reliably under the required conditions. The information given in semiconductor device data sheets often is insufficient to answer all questions. This application report discusses relevant problems not covered in the data sheets, such as the latch-up effect in CMOS circuits. That semiconductor manufacturers take extensive precautions to prevent these problems arising in integrated circuits is reason enough for the design engineer to become acquainted with them. Care was taken in preparing this application report to differentiate between the latch-up effect and other phenomena, which arise for completely different reasons, but are called latch-up. The situation is different with the immunity of integrated circuits to electrostatic discharges. Many test methods have been developed to realistically test the robustness of devices. However, all of these tests can provide an answer only under particular operating conditions. Therefore, users must use data from the manufacturer to reach conclusions about the suitability of components in a specific situation and to take additional precautions as necessary.

The existence of so-called parasitic transistors in semiconductor devices can cause operational problems of which users should be aware. The basic cause of these problems has been examined in detail, together with the possible manifestation of parasitic transistors in actual circuits. The discussion on parasitic transistors concluded with several precautions in system design that can be taken to solve the latch-up problem.

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1. James E. Vilson and Juin J. Liou, Electrostatic Discharge in Semiconductor Devices: An Overview, *Proceedings of the IEEE*, Vol. 86, No. 2. February 1998.
2. Texas Instruments, *Using the TL7726 Hex Clamping Circuit* Application Report, literature number SLAA004. (see http://www.ti.com/sc/docs/psheets/app_msp.htm)
3. Texas Instruments, *Input and Output Characteristics of Logic Circuits* Application Report, literature number SDZAE05.

Additional information on this subject:

4. Texas Instruments, Digital Design Seminar Manual, literature number SDYDE01A.
5. Texas Instruments, Data Transmission Seminar Manual, literature number SLLDE01C.
6. Texas Instruments, Linear Design Seminar Manual, literature number SLYDE05.
7. Texas Instruments, Logic Application Reports and Product Selection CD-ROM, literature number SDZE01A.
8. Texas Instruments Internet site: http://www.ti.com

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