TEXAS INSTRUMENTS

THS1240 EVM

User's Guide

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AAP Data Conversion

SLAU053A

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Preface

Read This First

About This Manual

This user's guide describes the characteristics, operation, and use of the THS1240 EVM.

How to Use This Manual

This document contains the following chapters:

- Chapter 1 EVM Overview
- Chapter 2 Getting Started
- Chapter 3 User Configurations
- Chapter 4 Control Modes
- Appendix A Schematics

Related Documentation From Texas Instruments

To obtain a copy of any of the following TI documents, call the Texas Instruments Literature Response Center at (800) 477–8924 or the Product Information Center (PIC) at (972) 644–5580. When ordering, please identify the book by its title and literature number if possible.

Data Sheets:	**Literature Number**
THS1240	SLAS274
THS1060	SLAS212
THS1050	SLAS278
SN74AHC00	SCLS227F
THS4141	SLOS320A
THS3201	SLOS242
TLV2772ACD	SLOS209D
TL1431	SLVS062F
SN74ABT244	SCBS099I
SN74AHC574DW	SCLS148C
OPA681U	SBOS084

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PowerPAD™ is a trademark of Texas Instruments.

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Chapter 1

EVM Overview

Chapter 1 gives an overview of the THS1240 evaluation module (EVM), and provides a general description of the features and functions to be considered for proper use of this module.

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1.1 System Overview

The THS1240 EVM provides a practical platform for evaluating the THS1240 12-bit resolution, 40-MSPS, low-power CMOS, parallel data output, IF sampling communications analog-to-digital converter.

The THS1240 (sometimes referred to as the ADC or device) is designed to operate at a 40-MHz maximum clock frequency, making the device suitable for IF sampling of baseband radio signals. The device's internal reference can be powered down when using an external voltage reference.

The EVM supports the heat-dissipating TQFP (HTQFP) PowerPAD™ package style.

Table 1–1. Package Styles Available

Device	HTQFP Package† Supported
THS1240	48-pin (S-PQFP-G48)

† The HTQFP package is a high temperature plastic quad flatpack device, with pins on a 0.50-mm pitch.

The schematic diagram of the THS1240 EVM (see Appendix A) shows the actual circuit involved. It is formed by:

- Clock-input buffer circuits
- An external crystal (clock) oscillator
- ADC internal reference power-down control logic
- An external V_{ref} circuit
- An input voltage regulator circuit
- Data-bit output buffers
- A 1:2 voltage ratio step-up transformer (used for converting a single-ended input clock signal to a differential clock signal)
- A 1:1 voltage-ratio transformer (used for converting a single-ended analog input to a differential input signal)
- An analog input signal conditioning operational amplifier
- A differential amplifier used to drive the ADC analog inputs directly

The EVM is a four-layer board constructed from FR4 material. This type of system gives the user the opportunity to explore and test various clock-driving and analog-input interface circuits.

This description provides only a general overview of the EVM and is not meant to replace the circuit diagram, but to give a brief indication of the features and functions available. Therefore, in conjunction with the circuit diagram supplied, the user should also refer to Texas Instruments literature number SLMA002 *PowerPAD™ Thermally Enhanced Package* and to the device's data sheet, literature number SLAS274.

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1.2 THS1240 ADC System Outline

This printed wiring board (PWB) EVM supports the THS1050/1060/1240 analog-to-digital converters. In addition, the EVM can be used to evaluate several types of clock-driving and analog-input interface circuits provided on the EVM.

The THS1240 ADC generates 2s-complement data in parallel data form. The D[11:0] output lines are suitable for driving load capacitances up to 15 pF. General features of the ADC are given in Table 1-2.

Table 1–2. General ADC Features

Device	Resolution	Output Channels	Supports Vref_int/Vref_Ext	Throughput AV_{DD} =5 V DV_{DD} = 5 V	Available Package	EVM Order Number
THS1240	12-bit	D[11–0]	Vref_Int /Vref_Ext	40 MSPS	HTQFP(PHP)	THS1240

1.2.1 THS1240 ADC

The THS1240 CMOS pipelined ADC device integrates a nominal 2.4-V bandgap reference, a sample/hold circuit, timing/synchronizing logic, cascade gain stages (consisting of A/D, D/A, and amplifier), and digital error-correction logic for correcting the device outputs. The device has good linearity and excellent SFDR specification and can directly drive 15 pF of load capacitance. The THS1240 can tolerate up to 10 pS of analog input signal jitter and 250 ps skew between CLK+ and CLK– without noticeable performance degradation. This device operates from an analog supply of 5 V and a digital supply of 5 V. The power dissipation at 5 V is less than 380 mW. Reference voltages for the THS1240 are provided by the on-chip bandgap reference voltage or by an external precision reference voltage.

In addition to its peak processing performance of 40 MSPS, the THS1240 analog-to-digital converter (ADC) has an ENOB of 10.6, SFDR of 74 dBc, and is compatible with existing 10-, 12-, and 14-bit commsDAC™ devices from Texas Instruments. The THS1240 die is bonded directly to a copper (Cu) alloy plate on the bottom side of the device package. To improve heat conduction, the Cu alloy plate is often connected to the PCB ground plane.

The PWD input (pin 13) disables the device's internal voltage reference when set to logic high.

1.2.2 THS1240 Clocking Scheme

The clock driver circuit can be implemented with a differential amplifier. The schematic in Appendix A shows three circuits for implementing the ADC differential clock. When using a differential amplifier, transformer T2 and resistors R28 and R29 must be removed from the circuit. The device requires a differential clock input of ≥ 6.5 Vp-p. For the purpose of testing the device, a single-ended clock signal is normally derived from a signal source that can output a sine-wave or a square-wave clock (HP8133A pulse generator). Transformer T2 is used to convert the single-ended clock to differential inputs.

This conversion minimizes clock skew and simplifies the design task. It is good design practice to balance the differential outputs from the transformer feeding the ADC's CLK+/CLK- pins. Be aware that the transformer has a certain amount of insertion loss at the frequency of operation.

An SN74ABT244 is used to buffer a TLL level input clock, often the most readily available and convenient signal source. When testing the ADC, it may be convenient to plug in a crystal oscillator and use its output to provide the desired ADC clock. Crystal oscillator X1 provides the clock.

1.2.3 Analog Input Drive Circuits

The 1:1 RF transformer is used for impedance matching, dc isolation, and for interface between U6 (ADC) balanced differential pair input and an unbalanced single-ended analog input. Resistors R25 and R26 are used to form a network that reflects 50 Ω across the primary circuit (across J4).

The THS3201/OPA681 is used to provide gain and input-signal buffering.

The THS4141 differential amplifier is used to convert the single-ended analog input signal to differential output.

1.2.3.1 Operational Amplifier Interface Circuits

The THS3201/OPA681 is the basic circuit element of the operational amplifier interface circuit used in this design. The device is a high-speed, current-feedback operational amplifier suitable for driving a high capacitance load. Some of the other THS3201 device features are: 3300-V/μS slew rate, – 96-dBc distortion figure, 1-GHz bandwidth, 15-nS settling time to 0.01% of the input, and ±5-V supply voltages. The OPA681 features 200-V/μs slew rate, 280-MHz bandwidth, and 77-dBc distortion figure.

The operational amplifier interface circuit is used to buffer the analog input signal on its way to the ADC input channels. The amplifier provides a noninverting gain of 2.

The THS4141 differential amplifier is used to perform single-ended-to-differential output conversion, thereby eliminating the need for the RF transformer. The device features are 200-MHz –3-dB bandwidth, slew rate >650 V/μS, –84-dBc distortion figure, 304-nS settling time to 0.01% of the input, and a supply range of ±5 V to ±15 V.

1.2.3.2 Internal Reference Voltage Circuit

The on-chip bandgap circuit is used to generate the nominal 3-V REFOUT+ output and the nominal 2-V REFOUT– output. A fixed internal-reference voltage is produced when REFOUT+ is directly connected to REFIN+ and REFOUT– is connected to REFIN–. The reference-circuit input resistance is approximately 200 Ω – 240 Ω. W4, W5, and W14 are all opened when using the internal reference.

1.2.3.3 External Voltage Reference Circuit

A Max1682 charge pump, a Thaler Corp VRE3050 precision voltage reference, a resistor network, and two TLE2227 operational amplifiers, configured as unity-gain noninverting buffer amplifiers, are used to provide the device's adjustable-external-reference voltages VREF+ and VREF–. The VRE3050 has 0.01% initial accuracy and a temperature coefficient (TC) of 0.6 ppm/°C, making it a suitable voltage reference for the ADC. The Max1682 requires an input voltage ≥5 V for an output of 10 V.

Using the external-reference voltage requires W6 and W7 to be opened and W4 and W5 to be connected; W14 may or may not be connected.

Output Buffers
Two SN74AHC574s are used to buffer the ADC output to connector J7. The SN74AHC574s are required to drive load capacitances greater than 15 pF.

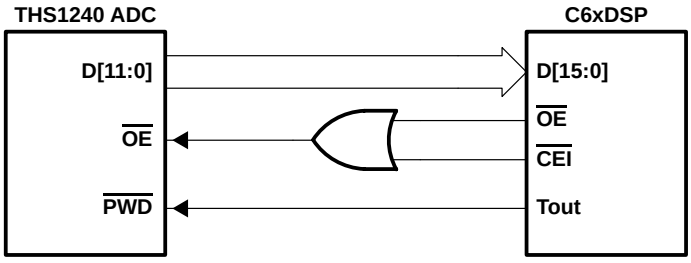
TL1431 Shunt Regulator
A TL1431 precision shunt voltage regulator is used to generate the 3.3-V DV_{CC} supply. The TL1431 has 0.4% initial accuracy and a temperature coefficient (TC) of 30 ppm/°C, making the device a suitable 3.3-V voltage regulator for a 10-bit ADC operating in a temperature controlled environment.

1.2.3.4 DSP interface

The THS1240 has 12 parallel data-output lines (D[11:0]). There are various DSP interface options; an interface to the C6201DSP is used in this document. Use a DSP to provide chip-select ($\overline{OE}$), input clock (CLKOUT), and power-down signal input (PWD\) for the device.

The schematic diagram in Figure 1–1 shows the pin-to-pin connections between the THS1240 EVM and the TMS320C6x EVM. It is relatively simple to use the DSP to collect the ADC samples and store them in DSP memory with the configuration shown in Figure 1–1.

Figure 1–1. THS1240 to C6X DSP Interface



1.2.3.5 Logic Analyzer/Signal Generator Interface

Connector J7 is used to interface a logic analyzer to the EVM. The SMA connector J5 interfaces directly to an HP8133A clock source, and connector J4, through a BNC to SMA cable, interfaces to an HP33120A or HP8644B signal generator used to provide the analog input to the EVM.

1.2.3.6 THS56X1 EVM Parallel DAC Interface

The THS56X1 EVM, with either a 12-bit resolution THS5661A or a 14-bit resolution THS5671A DAC, mates directly to connector J7 on the THS1050/

1060/1240 EVM board. The DAC outputs can each supply up to 20 mA of current. Twelve data lines (D[11:0]), two address lines (A0, A1), an $\overline{\text{IOSTROBE}}$ control line or W1 (grounded), and the CLK signal from the ADC are used to interface the DAC to the ADC.

1.3 EVM Operating Modes

The EVM can operate in two modes:

- DSK/microprocessor mode
- Logic analyzer/signal generator mode

See *DSP Interface* and *Logic Analyzer/Signal Generator Interface* sections for further information on these modes.

1.4 Power and Cabling Requirements

The EVM dc-supply voltages are analog ±5 V and digital 5 V. Supply these voltages to the EVM through shielded-twisted-pair wire for best performance. This type of power cabling minimizes any stray or transient pickup from the higher-frequency digital circuitry. A TLC1431 shunt regulator is used to generate 3.3-V DV_{CC} supply for the onboard output buffers U8 and U9—provided on the EVM for driving high capacitance load—and the ADC's output driver power supply DRVDD. The best SNR performance is achieved when both DRVDD and DV_{CC} are 3.3 V.

The crosstalk between adjacent conductors is minimized if a shielded ribbon cable is used for interfacing to J7.

1.5 ADC Output Configuration

The ADC generates 2s-complement data in a parallel format. It is not necessary to buffer the output from the device for load capacitances less than 15 pF.

1.6 Printed Circuit Assembly Options Available

A variety of input-drive circuits are provided on the THS1050/1060/1240 EVM to make it easy for the user to evaluate different drive techniques and to ensure the flexibility of the printed-circuit board (PCB).

Table 1–3. Possible ADCs

ADC Part No.	No. of Bits	Speed	EVM Order No.
THS1050	10	50 MSP	THS1050
THS1060	10	60 MSP	THS1060
THS1240	12	40 MSP	THS1240

Ensure that the printed-circuit assembly (PCA) has the correct check mark on the silkscreen.

Additional hardware may be required to install the PCA.

Chapter 2

Getting Started

This chapter describes the physical characteristics and PCB layout of the EVM and lists the components used on the module.

Topic **Page**

2.1 Physical Description

The PWB is constructed in four layers (FR4 material) as shown in Figures 2–2 through 2–5. The dimensions of the PWB are 4.625 in × 3.000 in (117,48 mm × 76,20 mm).

2.2 PowerPAD™

The THS1240 comes in a 48-pin HTQFP package with a Cu alloy plate on the bottom side of the package. The PowerPAD™ package provides good heat-transfer performance from the die to the surroundings. The THS1240 has power consumption of approximately 380 mW for 40-MHz operation.

The plots in Figures 2–2 and 2–3 show the actual size of the thermal pad used to connect the device copper alloy plate to the PCB ground plane. A 6-mil thick laser-cut stencil is used to dispense the solder paste during manufacturing of the EVM board.

Refer to the THS1240 data sheet for more information on the device performance with the PowerPAD™ soldered to the board versus the performance when the PowerPAD™ is not soldered to the board. The actual test results were taken using the THS1050/1060/1240 EVM.

Figures 2–1 through 2–5 show the tracking for each layer.

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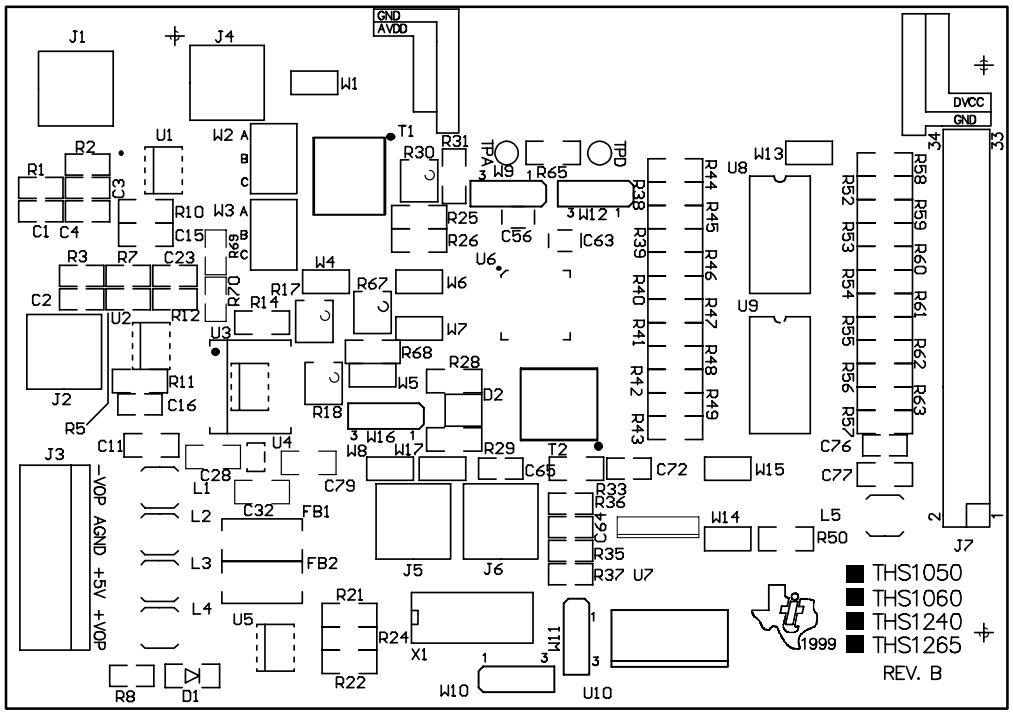
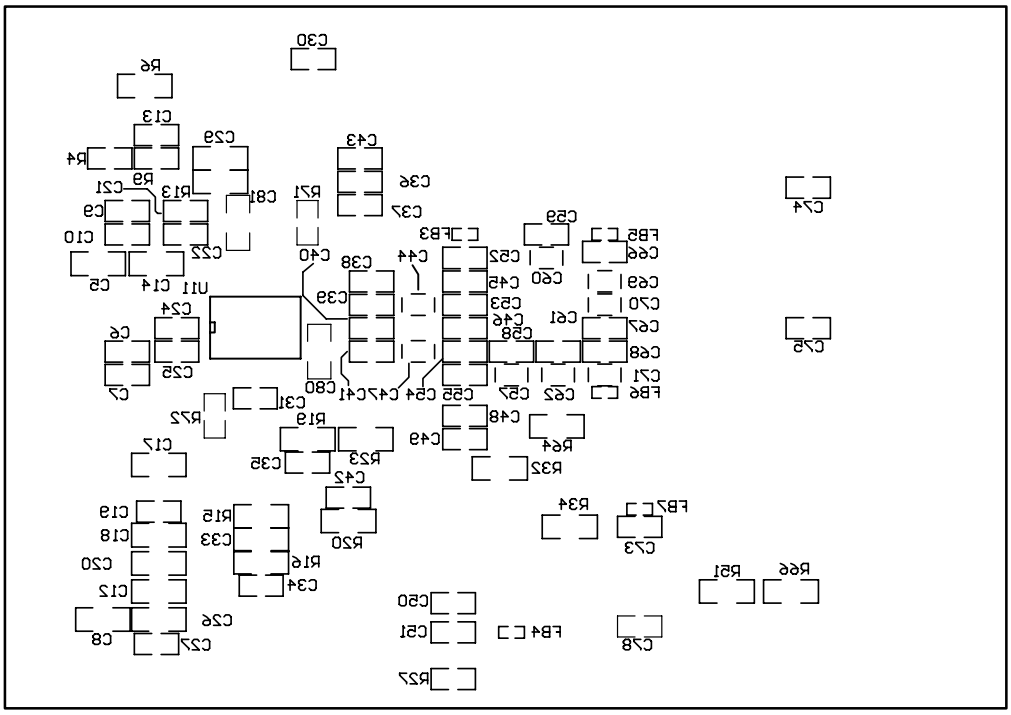
Figure 2–1. PWB Layers

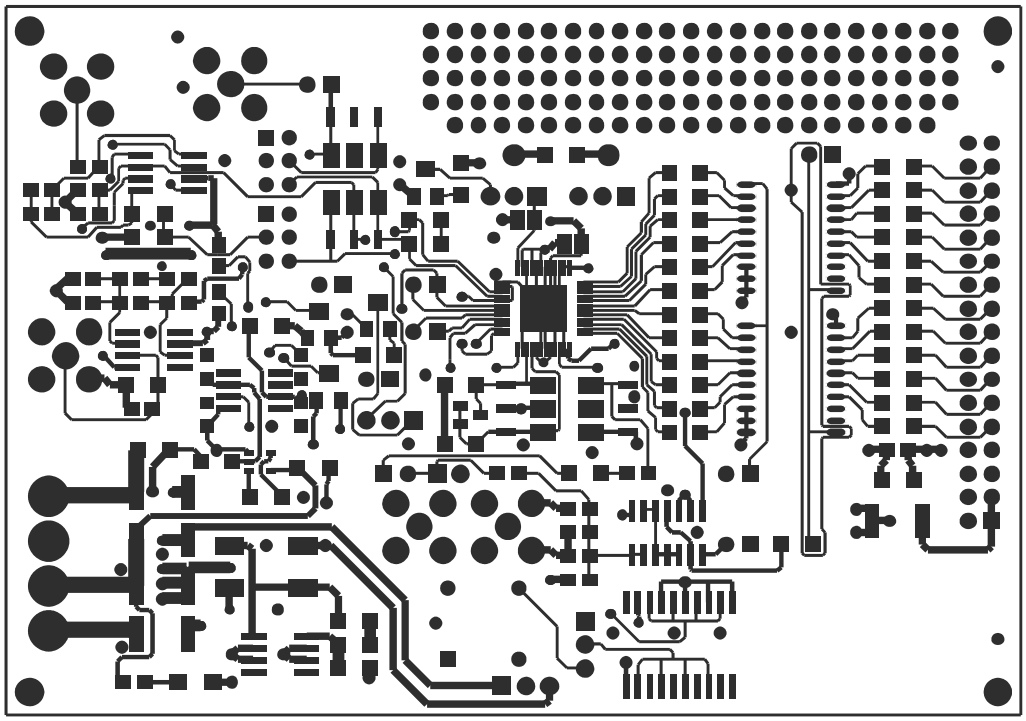


TOP VIEW



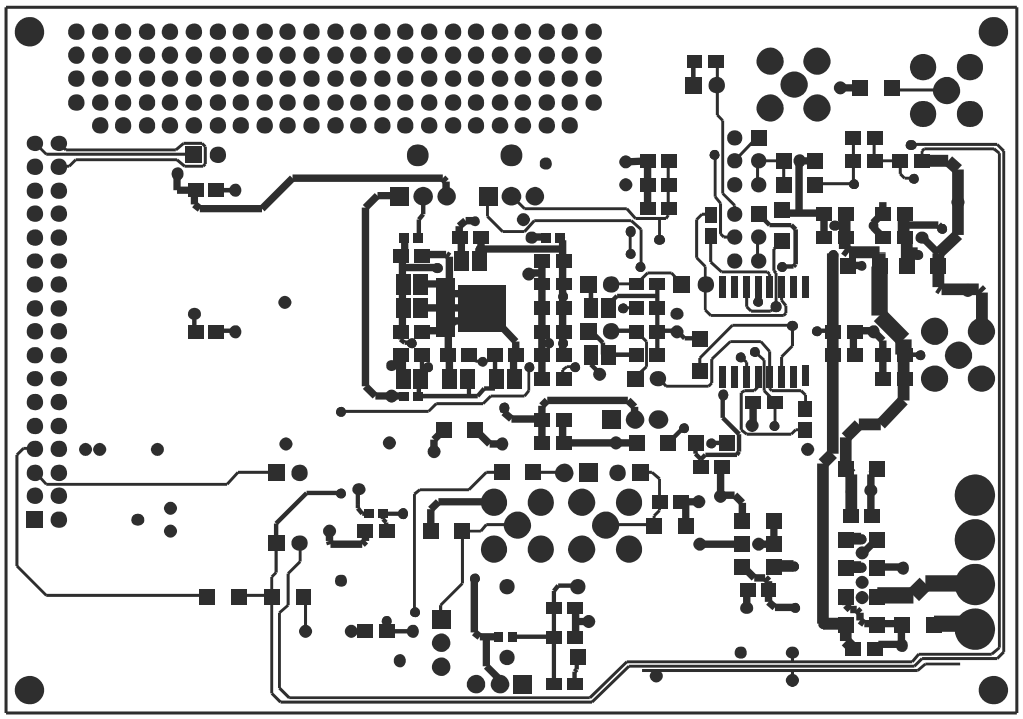
BOTTOM VIEW

Figure 2–2. Layer 1



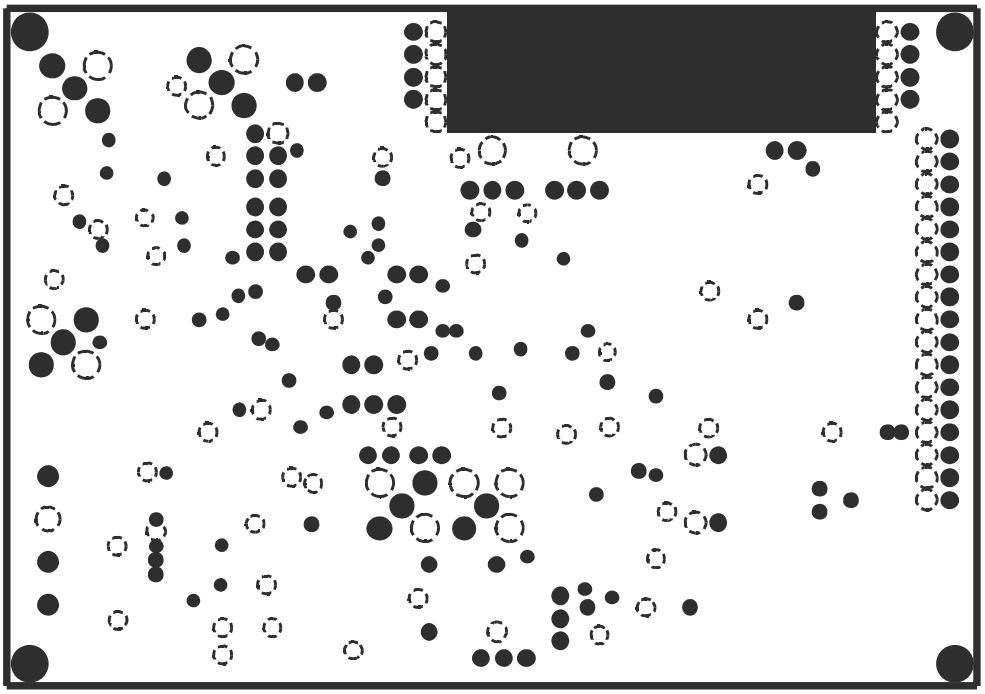
TOP VIEW

Figure 2–3. Layer 2



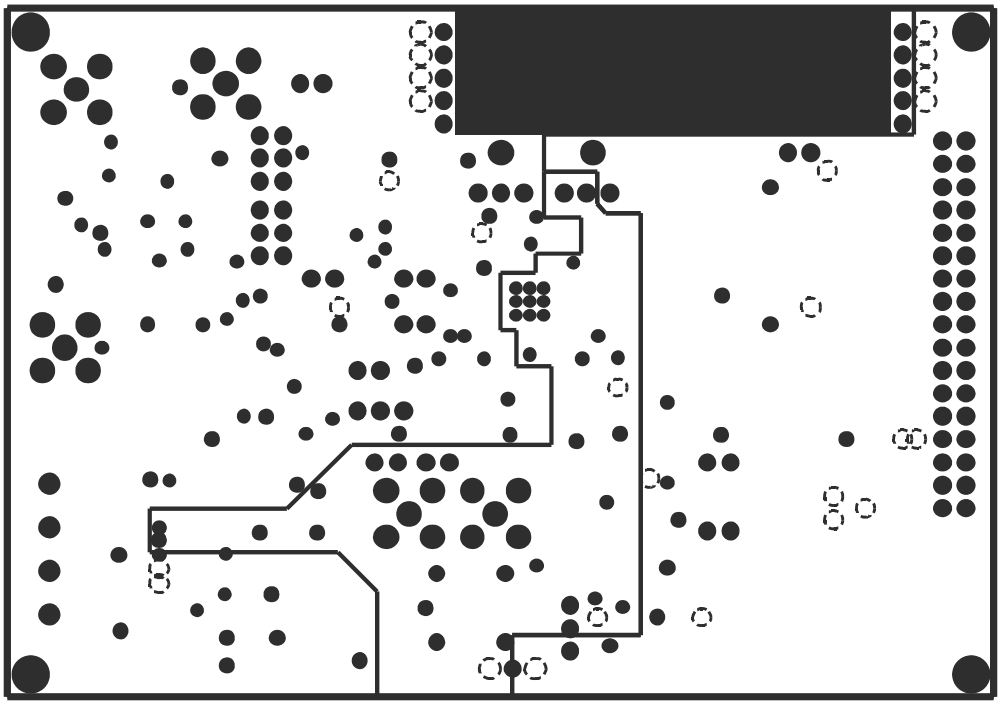
BOTTOM VIEW

Figure 2–4. Layer 3



GROUND PLANE

Figure 2–5. Layer 4



POWER PLANE

2.3 Parts List

QTY.	Reference Des.	Value	Footprint	Description	MFG	P/N
1	N/A	N/A	N/A	PCB fabrication		THS1265–REV C
12	C30 C44 C47 C56 C57 C60 C62 C63 C69 C70 C71 C72	0.1 µF	0508	Ceramic, X7R, 16 V, 15%	AVX / Murata	0508YC104MAT1W / LL0508X7R104K16
15	C10 C19 C22 C25 C27 C3 C34 C51 C65 C7 C73 C74 C75 C76 C78	0.1 µF	0805	Ceramic, X7R, 16 V, 10%	AVX / Murata	0805YC104KAT1A / GRM40X7R104K016A
16	C11 C12 C14 C17 C18 C20 C26 C28 C32 C33 C5 C77 C8 C79 C80 C81	10 µF	1206	Ceramic, Y5V, 10 V, 80/–20%	AVX / Murata	1206ZG106ZAT2A / GRM42–6Y5V106Z010A
2	C15 C29	22 pF	0805	Ceramic, COG, 25 V, 10%	AVX / Murata	08053A220KAT2A / GRM42–6COG220K025A
13	C21 C24 C4 C45 C46 C58 C59 C6 C61 C66 C67 C68 C9	0.01 µF	0805	Ceramic, X7R, 16 V, 10%	AVX / Murata	0805YC103KAT1A / GRM40X7R103K016A
1	C23	4.7 pF	0805	Ceramic, COG, 25 V, 10%	AVX / Murata	08053A4R7KAT2A / GRM40COG5R0C025A
3	C39 C41 C52	4.7 µF	0805	Ceramic, Y5V, 10 V, 80/–20%	AVX / Murata	0805ZG475ZAT1A / GRM40Y5V475Z010A
8	C31 C35 C36 C38 C40 C53 C54 C55	1 µF	0805	Ceramic, X7R, 10 V, 20%	AVX / Murata	0805ZC105MAT1A / GRM40X7R105M010A
2	C43 C48	0.47 µF	0805	Ceramic, X7R, 16 V, 10%	AVX / Murata	0805YC474KAT1A / GRM40X7R474K016A
3	C37 C49 C50	1 nF	0805	Ceramic, X7R, 16 V, 10%	AVX / Murata	0805YC102KAT1A / GRM40X7R102K016A
1	D1	Green LED	1206	Green 1206 size chip LED	Chicago Miniature	CMD15–21VGC
2	FB1 FB2	Ferrite bead		Surface-mount ferrite bead	Fair Rite	2743037447
5	FB3 FB4 FB5 FB6 FB7	Ferrite bead	0603	Surface-mount ferrite bead	Murata / Fair Rite	BLM11HB601SD / 2506033017Z0
6	J1 J2 J4 J5 J6 J8	SMA Jack		PCB mount SMA jack	Johnson Components / Lighthorse Tech.	142–0701–206 / LTI–SASF54NT

QTY.	Reference Des.	Value	Footprint	Description	MFG	P/N
1	J3	Terminal block		Four-terminal screw connector	Lumberg / Kaltron	KRMZ4 / TB–04SLA
1	J7	17 × 2 × 0.1		34-pin dual row header	Samtec	TWS–117–07–L–D
5	L1 L2 L3 L4 L5	4.7 µH	DO1608C	4.7 µH, ±20%, 1.5 A	Coil Craft	DO1608C–472
3	R1 R2 R9	511	0805	0805 chip resistor, 1%	Bourns	CR0805–FX–5110
32	R10 R11 R13 R34 R38 R39 R40 R41 R42 R43 R44 R45 R46 R47 R48 R49 R52 R53 R54 R55 R56 R57 R58 R59 R60 R61 R62 R63 R66 R6	49.9 Ω	1206	1206 chip resistor, 1%	Bourns	CR1206–FX–49R9
12	R12 R15 R24 R64 R65 R32 R33 R50 R69 R70 R71 R72	0 Ω	1206	1206 chip Res., 5%	Bourns	CR1206–FX–000
1	R14	2.21 kΩ	1206	1206 chip resistor, 1%	Bourns	CR1206–FX–2941
4	R17 R18 R30 R67	2K potentiometer		4mm, 5T, SM potentiometer	Bourns	3214W–2–202E
2	R28 R29	100 Ω	1206	1206 chip resistor, 1%	Bourns	CR1206–FX–1000
2	R31 R68	750 Ω	1206	1206 chip resistor, 1%	Bourns	CR1206–FX–7500
1	R19	1.1 kΩ	1206	1206 chip resistor, 1%	Bourns	CR1206–FX–1501
1	R23	1.05 kΩ	1206	1206 chip resistor, 1%	Bourns	CR1206–FX–1051
3	R16 R25 R26	24.9 Ω	1206	1206 chip resistor, 1%	Bourns	CR1206–FX–24R9
1	R22	24.9 kΩ	1206	1206 chip resistor, 1%	Bourns	CR1206–FX–2492
5	R27 R3 R36 R5 R8	1 kΩ	0805	805 chip resistor, 1%	Bourns	CR0805–FX–1001
2	R35 R37	383 Ω	0805	805 chip resistor, 1%	Bourns	CR0805–FX–3830
1	R4	523 Ω	0805	805 chip resistor, 1%	Bourns	CR0805–FX–5230
1	R51	10 kΩ	1206	1206 chip resistor, 5%	Bourns	CR1206–FX–103
1	R7	169 Ω	0805	805 chip resistor, 1%	Bourns	CR0805–FX–1690
1	R21	8.06 kΩ	1206	1206 chip resistor, 1%	Bourns	CR1206–FX–8061
2	R73 74	10 Ω	1206	1206 chip resistor, 1%	Bourns	CR1206–FX–10R0
1	T1	T1–6T–KK81	MC_KK81	RF transformer	Mini-Circuits	T1–6T–KK81 / ADT1–6T–3
1	T2	T4–1T–KK81	MC_KK81	RF transformer	Mini-Circuits	T4–1T–KK81 / ADT4–6T–1
2	TPA TPD	Test point		Turret-type test pin	Cambion	180–7337–02–05

QTY.	Reference Des.	Value	Footprint	Description	MFG	P/N
1	U1	THS4141	8–SOIC(D)	200-MHz Differential op amp	Texas Instruments	THS4141CD / THS4141ID
1	U2	THS3201/OPA681	8–SOIC(D)	420-MHz, high speed amp	Texas Instruments	THS3201CD / THS3201ID/OPA681U
1†	U3	VRE3050	8–SOP(D)	Precision voltage regulator	Thaler Corp.	VRE3050ASN / VRE3050JSN
1	U4	MAX1682	5–SOT(DBV)	Switched cap. voltage doubler	Maxim	MAX1682EUK–T
1	U5	TL1431	8–SOP(D)	Precision programmable reference	Texas Instruments	TL1431CD / TL1431QD
1	U6	THS1240	48–HTQFP(PHP)	12-bit, 40-MSPS ADC	Texas Instruments	THS1240CPHP / THS1240IPHP
1	U7	SN74AHC00	14–SOP(D)	Quad NAND gate	Texas Instruments	SN74AHC00DR
2	U8 U9	SN74AHC574	20–SOIC(DW)	3.3-V octal D-FF, 3-state	Texas Instruments	SN74AHC574DW
2	U10	SN74ABT244DW	20–SOIC(DW)	Octal buffer/driver	Texas Instruments	SN74ABT244DW
1	U11	TLE2227	16–SOIC(DW)	High speed, low noise, dual	Texas Instruments	TLS2227CDW
6	W14 W15 W4 W5 W6 W7	Shunt jumper	2X2X.1	0.025” sq, 2 pin header, 0.1” centers	Samtec	TWS–102–07–L–S
4	W10 W11 W12 W9 W16	2 position jumper	2X3X.1	0.025” sq, 3-pin header, 0.1” centers	Samtec	TWS–103–07–L–S
1	X1	40 MHz Oscillator		Crystal oscillator	Epson	SG–8002DC–40–MHz
†	U3 Alternate	MAX6250	8–SOP(D)	Precision voltage regulator	Maxim	MAX6250BCSA / MAX6250ACSA
Wire Jumper Defaults:						
MASK	W1 W13 W8	Jumper option		24 AWG solid bus wire		
MASK	W2 W3	Jumper option		24 AWG solid bus wire		
Customer Installed Options						
1	R20	49.9 Ω	1206	1206 chip resistors, 1%	Bourns	CR1206–FX–49R9
2	C42 C16	100 pF	0805	Ceramic, COG, 25 V, 10%	AVX / Murata	08053A101KAT2A / GRM40COG101K025A
1	C64	220 pF	0805	Ceramic, COG, 25 V, 10%	AVX / Murata	08053A221KAT2A / GRM40COG221K025A
1	C2	10 pF	0805	Ceramic, COG, 25 V, 10%	AVX	08053A100KAT2A / GRM40COG100K025A
1	D2	BAV99	SOT–23	Dual, small-signal diode	General Semiconductor	BAV99
2	C1 C13	1.8 pF	0805	Ceramic, COG, 25 V, 10%	AVX / Murata	08053A1R8KAT2A / GRM40COG1R8K025A

† Alternative device MAX6250

Chapter 3

User Configurations

This chapter describes the user-definable options.

Topic **Page**

3.1 User Options

The PCA ships in a state that enables immediate evaluation of the analog-to-digital converter (ADC). However, you can reconfigure various options through hardware. This chapter discusses these options to ensure that any reconfiguration is conducted properly.

The hardware on the PCA falls into various groups:

- Jumpers (shunts)
- Wire links

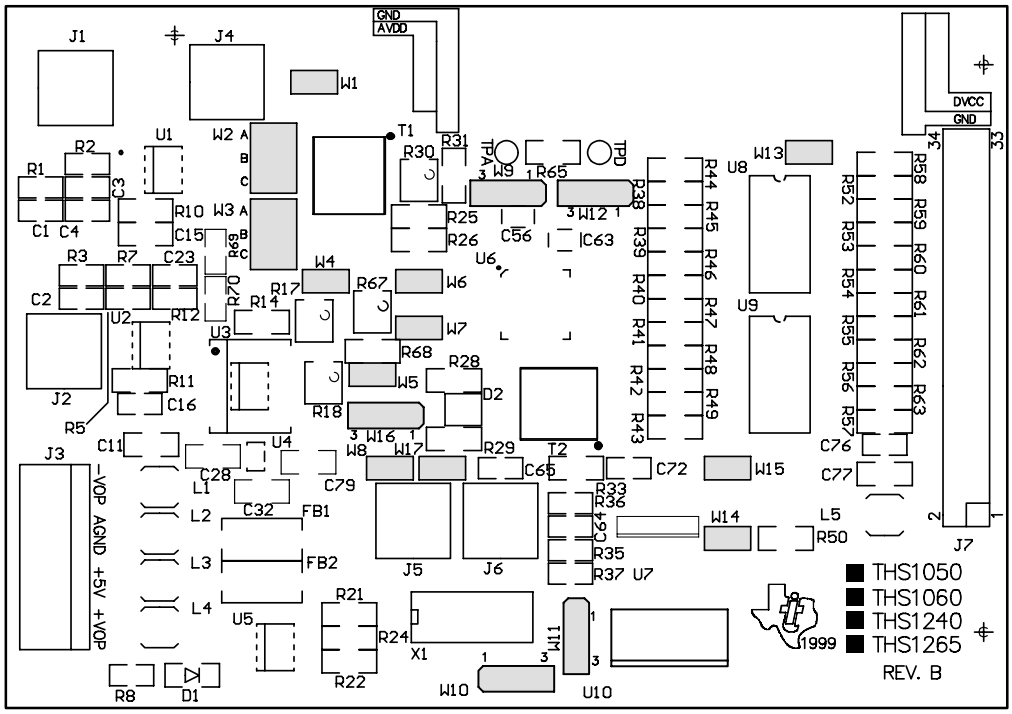
Table 3–1 lists jumper options, a brief description of each function, and information on where the option can be found.

Table 3–1. Jumper Functions

Jumper Reference	Function Description
W1	For bypassing C30
W2A	Connects pin 6 of transformer T1 to GND
W2B	Use to connect transformer T1 to a differential-voltage source
W2C	Connects –ve output of differential amp to the VIN– pin of the ADC
W3A	Connects amplifier THS3201/OPA681 to T1 primary winding
W3B	Use to connect transformer T1 to a differential voltage source
W3C	Connects +ve output of differential amp to the VIN+ pin of the ADC
W4	Connects external REF– to REFIN–
W5	Connects external REF+ to REFIN–
W6	Connects REFOUT– to REFIN–
W7	Connects REFOUT+ to REFIN+
W8	Connects the clock signal from J5 to circuit used to derive CLK signal
W9	Selects transformer T1 secondary dc bias: either Vcm from the ADC, or the external adjustable common-mode dc-biasing voltage
W10	Selects 5 V(DV_{DD}) or 3.3 V(DV_{CC}) as the V_{CC} supply to the on-board oscillator and the circuit used to generate the CLK output signal.
W11	Selects clock source J6 or 50, 60, or 65 MHz oscillator output
W12	Selects 3.3 V or 5 V as DRDD input voltage
W13	Connects CLK signal to J7
W14	GND W14 to disable internal VREF+/VREF–
W15	Use to GND $\overline{OE}$ of U8/U9
W16	Selects transformer T2 secondary dc bias, either Vcm from the ADC or the external adjustable common-mode dc-biasing voltage
W17	Connects U10A output to T2 and to the circuit that generates the CLK at J7–33

Figure 3–1 indicates the physical locations of this hardware.

Figure 3–1. Physical Locations of Each Jumper



TOP VIEW

3.2 Analog/Digital Supply Voltages

Two options supply power to the analog/digital sections of the EVM:

- 3.3 V (DV_{CC}) or 5 V digital DV_{DD} (the THS1240 output buffer is powered from 3.3 V or 5 V, while the V_{CC} input to the two SN74AHC574 buffers is tied to 3.3 V)
- 5 V analog AV_{DD}
- 5 V (+VOP) operational amplifier positive-supply voltage
- –5V (–VOP) operational amplifier negative-supply voltage

Configure the power supply voltages in accordance with Table 3–2.

Table 3–2. Analog Voltage Supply Configuration Options

J3 Connector	Function
J3–1	5 V (+VOP)
J2–2	5 V (AV_{DD})
J3–3	AGND
J3–4	–5 V (–VOP)

3.3 Digital Input Configurations

A variety of options are available to configure the digital inputs. This section describes these options, along with the jumper settings required.

Table 3–3. Digital Input Options

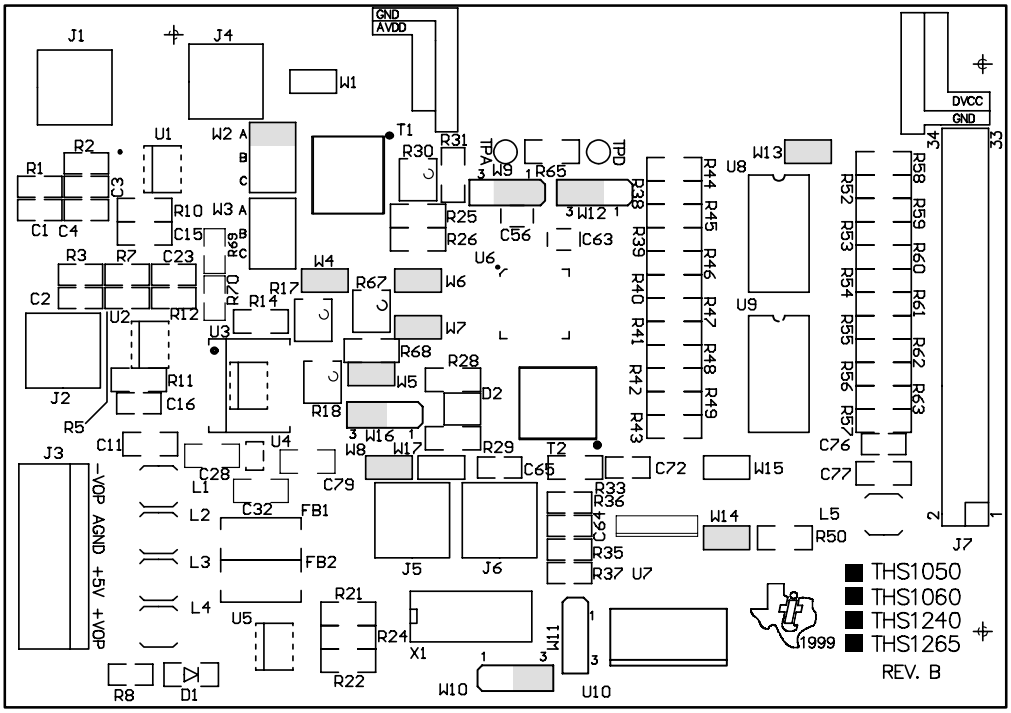
Digital Input Option	Connector Reference and Type
	IDC
Apply $\overline{\text{PWD}}$ signal from DSP to J7	J7 – 31 × 17 plug
Apply output buffers control signal, $\overline{\text{OE}}$, from DSP to J7 (pin 5)	J7 – 29 × 17 plug
External 3.3 V DV_{CC} supplied from J7	J7 – 25/27 × 17 plug

Select the above configurations according to the test equipment available. These are discussed below.

When jumper W15 is in place, the outputs of U8 and U9 are enabled. Use this configuration when the EVM is not hooked up to a DSP board. When using the EXT_VREF+/EXT_VREF– inputs, W14 can be used to power down the internal voltage reference. Thus, no connection to W14 may be made when using the internal-voltage reference.

Use J7 to effectively store in memory the 2s-complement ADC output data by using a few control lines from a DSP.

Figure 3–2. Direct Connect Jumper Configuration for THS1240 EVM



TOP VIEW

Table 3–4. Shipping Condition of Jumpers W1 Through W17

Jumper	Pins 1 and 2	Pins 2 and 3
W1	Jumper not installed	N/A
W2A	Jumper installed	N/A
W2B	Jumper not installed	N/A
W2C	Jumper not installed	N/A
W3A	Jumper not installed	N/A
W3B	Jumper not installed	N/A
W3C	Jumper not installed	N/A
W4	Jumper not installed	N/A
W5	Jumper not installed	N/A
W6	Jumper not installed	N/A
W7	Jumper installed	N/A
W8	Jumper installed	N/A
W9	Jumper installed	Jumper not installed
W10	Jumper installed	Jumper not installed
W11	Jumper installed	Jumper not installed
W12	Jumper not installed	Jumper installed
W13	Jumper installed	N/A
W14	Jumper not installed	N/A
W15	Jumper installed	N/A
W16	Jumper not installed	Jumper installed
W17	Jumper not installed	N/A

3.4 Generating a Voltage Reference

Two options provide the voltage reference:

- Internal reference
- Onboard external reference

3.4.1 Internal Reference

Setting the THS1240 to use REFOUT+ and REFOUT– as input voltages to the on-chip internal-reference circuit requires the jumper configuration shown in Table 3–5.

Table 3–5. Jumper Configuration for Internal Reference Voltage

Jumper	Pins 1 and 2	Pins 2 and 3
W4 (EXT_VREF+)	Jumper not installed	N/A
W5 (EXT_VREF–)	Jumper not installed	N/A
W6 (+2V)	Jumper installed	N/A
W7 (+3V)	Jumper installed	N/A
W14	Jumper not installed	N/A

3.4.2 Onboard External Reference

To select the on-board external reference voltage, follow the jumper configuration shown in Table 3–6.

Table 3–6. External VREF for U6 Jumper Configuration

Jumper	Pins 1 and 2	Pins 2 and 3
W4 (EXT_VREF+)	Jumper installed	N/A
W5 (EXT_VREF–)	Jumper installed	N/A
W6	Jumper not installed	N/A
W7	Jumper not installed	N/A

It is important to understand that the reference voltage plays a fundamental part in the conversion process. Changes in the value of the reference voltage are reflected in the full-scale range of the device. The variation in voltage for the reference should ideally contribute less than 1/2 an LSB of error to the total conversion process.

When using the onboard external precision voltage reference, install W14 or take the $\overline{\text{PWD}}$ line LOW to power down the device's internal-voltage reference. Disabling the internal-voltage reference while using an external-voltage reference avoids the need for the 4.7-μF capacitor on pins 8 and 9 of U6. The normal ADC operation with an external-voltage reference and U6–13 tied to GND requires a 1-μF (or greater) capacitor on pins 8 and 9 of U6.

3.5 Clock Source

The THS1240 requires an external clock. There are three possible external sources for the ADC clock on the EVM. To obtain optimum device performance, adhere to the minimum data-to-clock transition setup and hold times specified in data sheet SLAS274. Violating these timing parameters may result in increased converter-output noise level.

The clock for the ADC is derived from either the DSP, a crystal oscillator, a generator driving an ABT244 buffer, or a low-jitter clock source. The clock is normally a sine wave or square wave signal with amplitude ≥3.5 V peak.

3.5.1 External Clock Generation

The maximum operational speed of the THS1240 is 40 MHz when operating from 5-V AV_{DD} and DV_{DD} supplies. The clock signal is derived from either a low-jitter clock source, such as the HP8133A, or from the DSP CLKOUT signal, which usually is a less precise clock source.

3.5.2 Digital Output Circuit

Two SN74AHC574 buffers are used to interface the ADC to output connector J7. The resistor shown connected to Q[6:1] improves damping of the ADC buffered out lines.

3.6 Connector Pin and Function Assignments

This section details the pinouts and functions for all user connectors.

Table 3–7. Connector Pin and Function Assignments

Reference Designator	Function
J7	ADC 2s-complement parallel output/DSP interface
W11, J5, J6	Clock input
J3	Digital-circuit supply voltage
J3	Analog supply voltages
J1,J2,J4	Analog input

Table 3–8. J3 Power Connector

Pin Number	Function
J3–1	Operational amplifier +5 V power
J3–2	5-V analog power/5-V DV_{DD}
J3–3	AGND
J3–4	Operational amplifier –5-V power

Table 3–9. J1, J2, and J4 Analog Input Signal Connectors

SMA	Function	SMA	Function
J1–1	Single-ended analog input via differential amplifier	J1–2	AGND
J2–1	Single-ended analog input via operational amplifier	J6–2	AGND
J4–1	Single-ended input to T1 transformer	J4–2	AGND

Table 3–10. W11, J5, and J6 Clock Input Connectors

SMA	Function	SMA	Function
W11 pin 2/3	Single-ended clock oscillator input to T2 via SN74ABT244 buffer		
J5–1	Single-ended clock input to T2, 1:2 ratio step-up voltage transformer	J5–2	AGND
J6–1	Single-ended input via SN74ABT244 to T2, 1:2 ratio step-up transformer	J6–2	AGND

Table 3–11. J7, 2s Complement Parallel Data Connector/DSP Interface Connector

Pin Number	Function	Pin Number	Function
1	D11(MSB) (output)	2	Ground (digital)
3	D10 (output)	4	Ground (digital)
5	D09 (output)	6	Ground (digital)
7	D08 (output)	8	Ground (digital)
9	D07 (output)	10	Ground (digital)
11	D06 (output)	12	Ground (digital)
13	D05 (output)	14	Ground (digital)
15	D04 (output)	16	Ground (digital)
17	D03 (output)	18	Ground (digital)
19	D02 (output)	20	Ground (digital)
21	D01 (output)	22	Ground (digital)
23	D00 (LSB) (output)	24	Ground (digital)
25	DV_{CC} (3.3 V output)	26	Ground (digital)
27	DV_{CC} (3.3 V output)	28	Ground (digital)
29	$\overline{OE}$ (i/p)	30	Ground (digital)
31	$\overline{PWD}$ (i/P)	32	Ground (digital)
33	CLK/CLKOUT (input: W13 opened; output: W13 connected)	34	Ground (digital)

Chapter 4

Control Modes

The PWD, DRVDD REFIN+, REFIN–, REFOUT+, REFOUT–, and Vcm pins of the THS1240 control various ADC features and functions.

This section describes the function of these pins.

Topic **Page**

4.1 $\overline{\text{PWD}}$ Input Pin

The $\overline{\text{PWD}}$ pin is used for powering down the device's internal-voltage reference. It is an active-high asynchronous power-down input. The device has an internal pulldown. W14 or the $\overline{\text{PWD}}$ input signal is used to control the power-down input.

4.2 DRVDD Input Pin

DRVDD = 3.3 V
When the DRVDD pin is connected to 3.3 V (DV_{CC}), the device's output buffer is configured for 3-V logic-voltage levels.

DRVDD = 5 V
When the DRVDD pin is connected to 5 V, the device's output buffer is configured for 5-V logic-voltage levels.

4.3 REFOUT+ Output Pin

The REFOUT+ is nominally 3 V. Since the THS1240 voltage-reference circuit requires low current, REFOUT+ is ideal for supplying the REFIN+ input voltage. Jumper W7 is used to connect REFOUT+ to the REFIN+ pin.

When using the external-reference voltage provided through W5, remove shunt W7 from the board.

4.4 REFIN+ Input Pin

The REFIN+ dc-input voltage is provided either from the REFOUT+ output or from the onboard precision-voltage-reference circuit. When using the REFOUT+ to drive the REFIN+ input pin, connect W7 and make sure shunt W5 is removed from the board.

4.5 REFOUT– Output Pin

REFOUT– is nominally 2 V dc and is one of the two voltage sources used to supply input voltage to the REFIN– input pin of the THS1240. The other voltage source for supplying REFOUT– is via W4 from the precision-voltage reference circuit.

4.6 REFIN– Input Pin

The REFIN– dc-input voltage is provided either from the REFOUT– or from the onboard precision voltage reference circuit. When using REFOUT– to drive the REFIN– input pin, connect W6 and disconnect W4.

4.7 Vcm Output Pin

The THS1240 outputs a nominal 2.4-V-dc common-mode voltage (Vcm). This voltage is used to dc bias the secondary side of the two RF transformers and provide the common-mode voltage for the THS4141 differential amplifier.

Appendix A

Schematics

A complete schematic including all power supply line decoupling is shown in Appendix A.

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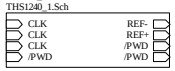
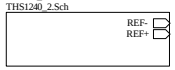
THS1240_1.Sch



1265RC_2
THS1240_2.Sch



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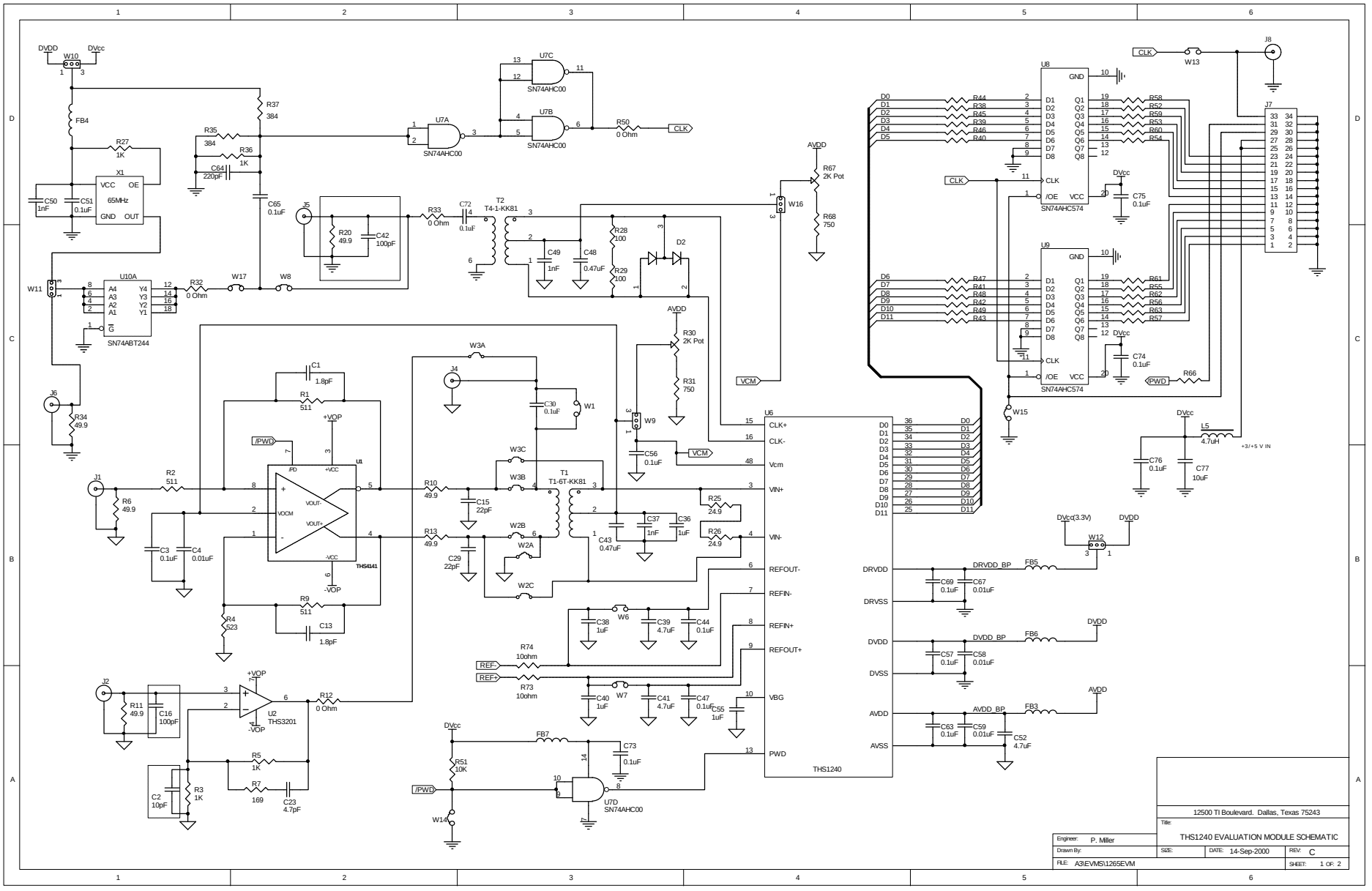
DVDD
DVcc
W10
FB4
R27 1K
X1
VCC OE
65MHz
GND OUT
C50 1nF
C51 0.1uF
R37 384
R35 384
R36 1K
C64 220pF
C65 0.1uF
U7A
U7B
U7C
SN74AHC00
R50 0 Ohm
CLK
AVDD
R67 2K Pot
R68 750
W16
J5
R20 49.9
C42 100pF
R33 0 Ohm
C72 0.1uF
T2
T4-1-KK81
C49 1nF
C48 0.47uF
R28 100
R29 100
D2
W11
U10A
SN74ABT244
R32 0 Ohm
W17
W8
J6
R34 49.9
W3A
J4
C30 0.1uF
W1
C1 1.8pF
R1 511
+VOP
/PWD
U1
THS4141
J1
R2 511
R6 49.9
C3 0.1uF
C4 0.01uF
R4 523
R9 511
C13 1.8pF
R10 49.9
C15 22pF
R13 49.9
C29 22pF
W3C
W3B
W2B
W2A
W2C
T1
T1-6T-KK81
C43 0.47uF
C37 1nF
C36 1uF
R25 24.9
R26 24.9
W9
R30 2K Pot
R31 750
VCM
C56 0.1uF
U6
THS1240
CLK+
CLK-
Vcm
VIN+
VIN-
REFOUT-
REFIN-
REFIN+
REFOUT+
VBG
PWD
W6
C38 1uF
C39 4.7uF
C44 0.1uF
R74 100ohm
R73 100ohm
REF-
REF+
W7
C40 1uF
C41 4.7uF
C47 0.1uF
C55 1uF
J2
R11 49.9
C16 100pF
U2
THS3201
R12 0 Ohm
R5 1K
R7 169
C23 4.7pF
C2 10pF
R3 1K
DVcc
FB7
C73 0.1uF
R51 10K
/PWD
W14
U7D
SN74AHC00
U8
U9
SN74AHC574
R44
R38
R45
R39
R46
R40
R58
R52
R59
R53
R60
R54
R47
R41
R48
R42
R49
R43
R61
R55
R62
R56
R63
R57
C75 0.1uF
C74 0.1uF
R66
W15
W13
J8
J7
L5 4.7uH
+3/+5 V IN
C76 0.1uF
C77 10uF
DVcc(3.3V)
W12
DRVDD
DRVSS
DVDD
DVSS
AVDD
AVSS
DRVDD_BP
DVDD_BP
AVDD_BP
FB5
FB6
FB3
C69 0.1uF
C67 0.01uF
C57 0.1uF
C58 0.01uF
C63 0.1uF
C59 0.01uF
C52 4.7uF
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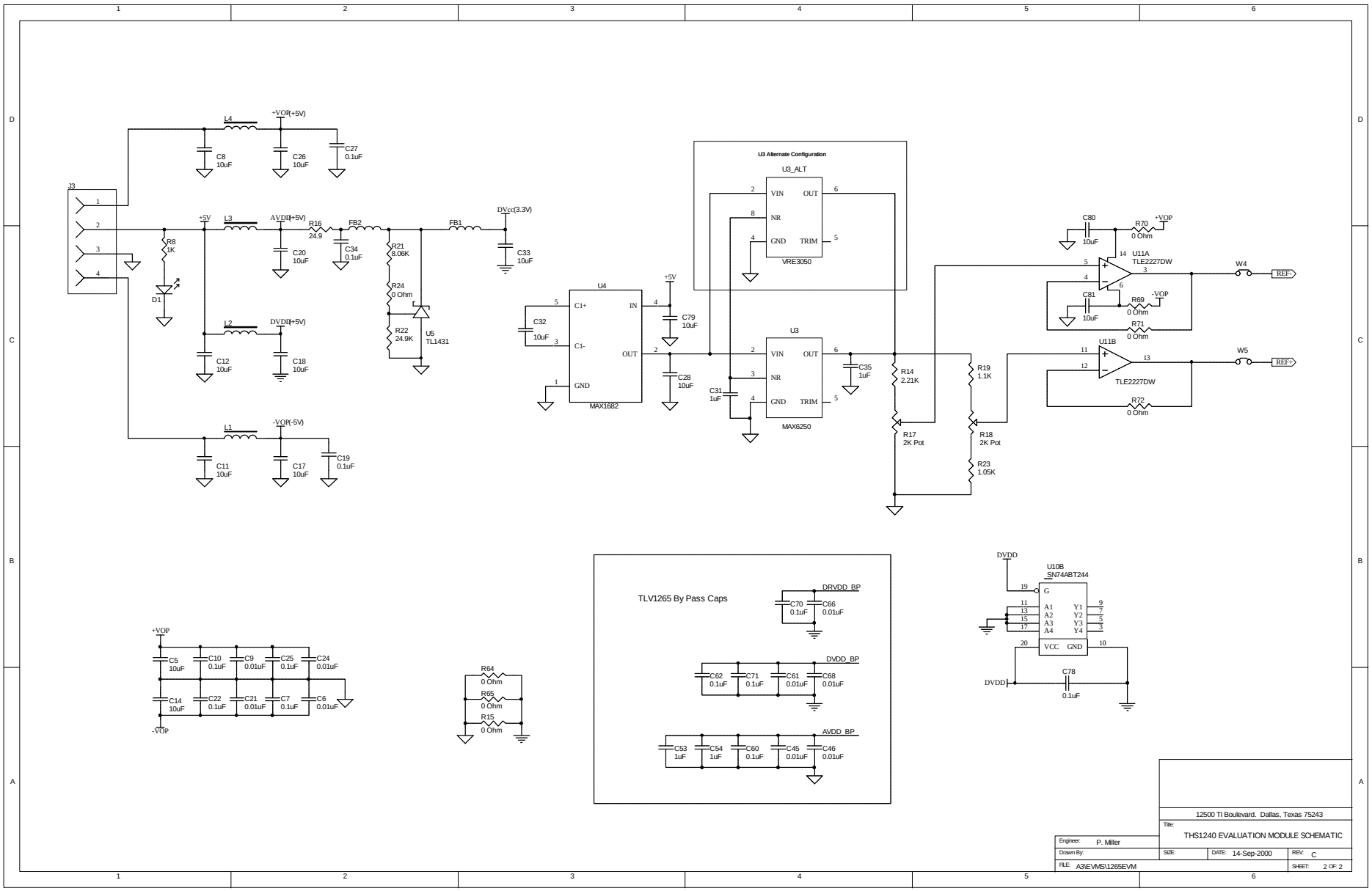

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