Managing Power in Dual-Supply Voltage Systems

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ABSTRACT

This application note describes the *design of a circuit using the Texas Instruments TPS2306 hot swap power manager to sequence the supply voltages, limit inrush current, and provide fault protection to a dual-supply voltage system*. The system uses both 3.3-V and 5-V power and is modeled as a resistor in parallel with a bulk filter capacitor at each input power rail. Component values are selected to meet a hypothetical design specification. The performance and specification of the circuit are compared to validate the TPS2306 design.

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1 Introduction

A microprocessor or programmable logic device with a 3.3-V core and 5-V I/O is a common example of dual supply voltage system. Improper voltage sequencing can trigger events like device latch-up and bus contention. The surge currents associated with these events can stress components and degrade system reliability. These issues can be avoided if the system power is properly managed with a device like the TPS2306. The TPS2306 sequences the turnon and turnoff of the load voltages, limits the load inrush current, and provides over-current protection.

2 A TPS2306 Overview

The TPS2306 has two identical channels of power control. Figure 1 is a simplified schematic that shows one of these channels in a design. Resistor R_{REF} sets the reference current I_{REF} and capacitor C_t sets the fault time τ_f for both TPS2306 channels.

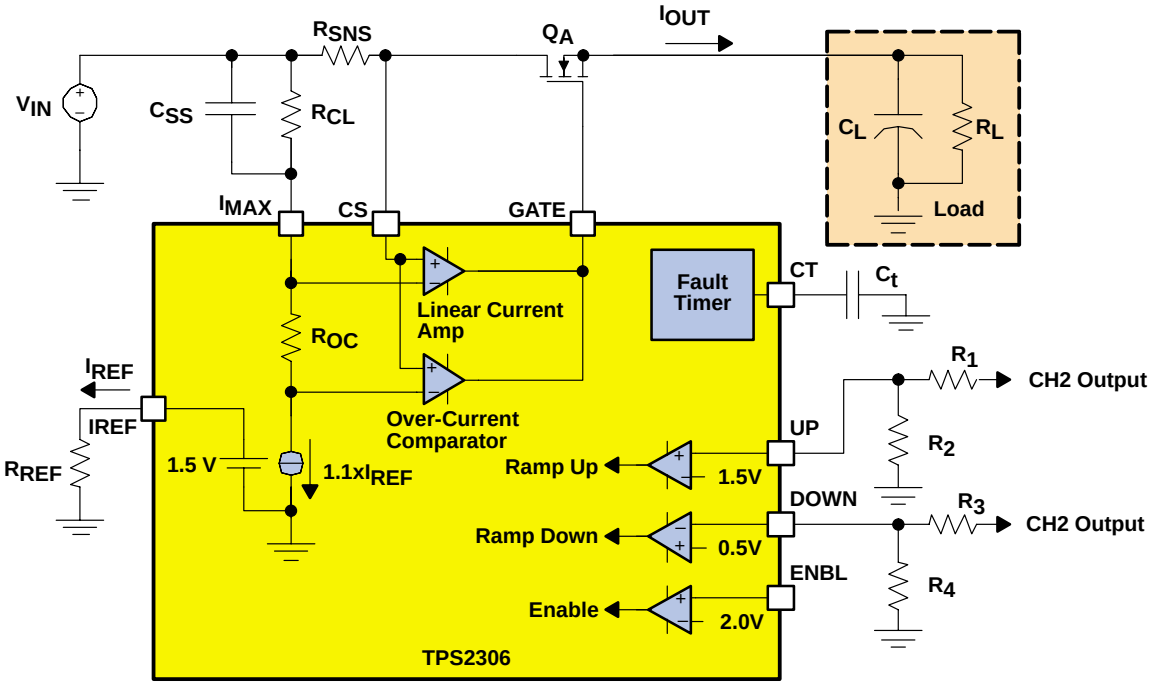


Figure 1. A TPS2306 Channel in a Typical Application

The load current I_{OUT} ramps up if the TPS2306 ENBL input is asserted and the UP input is greater than 1.5 V. The optional voltage divider at the UP input increases the turnon trigger voltage to above 1.5 V. The UP input is usually slaved to the output of another TPS2306 channel to sequence the *turnon* voltage. Tying the UP input to 1.5 V or higher disables turnon voltage sequencing.

MOSFET Q_A disconnects the load from the power supply if the ENBL input is de-asserted and the DOWN input is less than 0.5 V. The optional voltage divider at the DOWN input increases the *turnoff* trigger voltage to above 0.5 V. The DOWN input is usually slaved to the output of another TPS2306 channel to sequence the *turnoff* voltage. Tying the DOWN input to 0.5 V or lower disables turnoff voltage sequencing.

The TPS2306 linear current amplifier (LCA) modulates the transistor Q_A gate to force equal voltages across resistors R_{SNS} and R_{CL} at turnon or in an overload. This action limits the steady-state output current to equation (1) and the turnon output current to equation (2).

$$I_{CL} = \frac{1.1 \times I_{REF} \times R_{CL} \times R_{CL}}{R_{SNS}} \quad (1)$$

$$I_{OUT}(t) = I_{CL} \times \left(1 - e^{-t/\tau_{ss}}\right) \text{ for } t \geq 0 \text{ and } \tau_{ss} = R_{CL} \times C_{ss} \quad (2)$$

A 50-μA source charges capacitor C_t if the FET switch for either channel is operating in the linear region (i.e., at turnon or in current limit). At turnon, the output voltages must reach steady-state before capacitor C_t charges to 1.5 V, otherwise the circuit breaker trips and shuts off the FET switch for both channels. Equation (3) gives the fault time.

$$\tau_f = \frac{C_t \times V_{th}}{i_{chg}} \quad (3)$$

where V_{th} = 1.5 V and i_{chg} = 50 μA

The over-current comparator provides the circuit breaker function when transistor Q_A saturates. The over-current threshold that equation (4) describes is always higher than the current-limit threshold in equation (1).

$$I_{OC} = \frac{1.1 \times I_{REF} \times \left(R_{CL} + R_{OC}\right)}{R_{SNS}} \quad (4)$$

The over-current comparator bypasses the fault timer and immediately shuts off transistor Q_A to protect against a catastrophic fault.

The above equations are for nominal conditions. A worse case analysis is recommended when designing for production.

See the data sheet, SLVS368, for a more complete description of the TPS2306.

3 An Example

Table 1 lists the design specifications for the circuit shown in Figure 2. The load at each channel is modeled as a resistor in parallel with a bulk filter capacitor.

Table 1. Example Power Management Specifications

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
3.3-V Circuit					
Load capacitance		440	550	660	µF
Continuous output current		–	–	6	A
Voltage drop	Input-to-output	–	–	100	mV
Turnon slew rate		–	–	1.5	A/ms
Turnoff trigger voltage	From 5-V output	–	3.05	–	V
5-V Circuit					
Load capacitance		440	550	660	µF
Continuous output current		–	–	1.5	A
Voltage drop	Input-to-output	–	–	100	mV
Turnon slew rate		–	–	1.5	A/ms
Turnon trigger voltage	From 3.3-V output		2.63		V

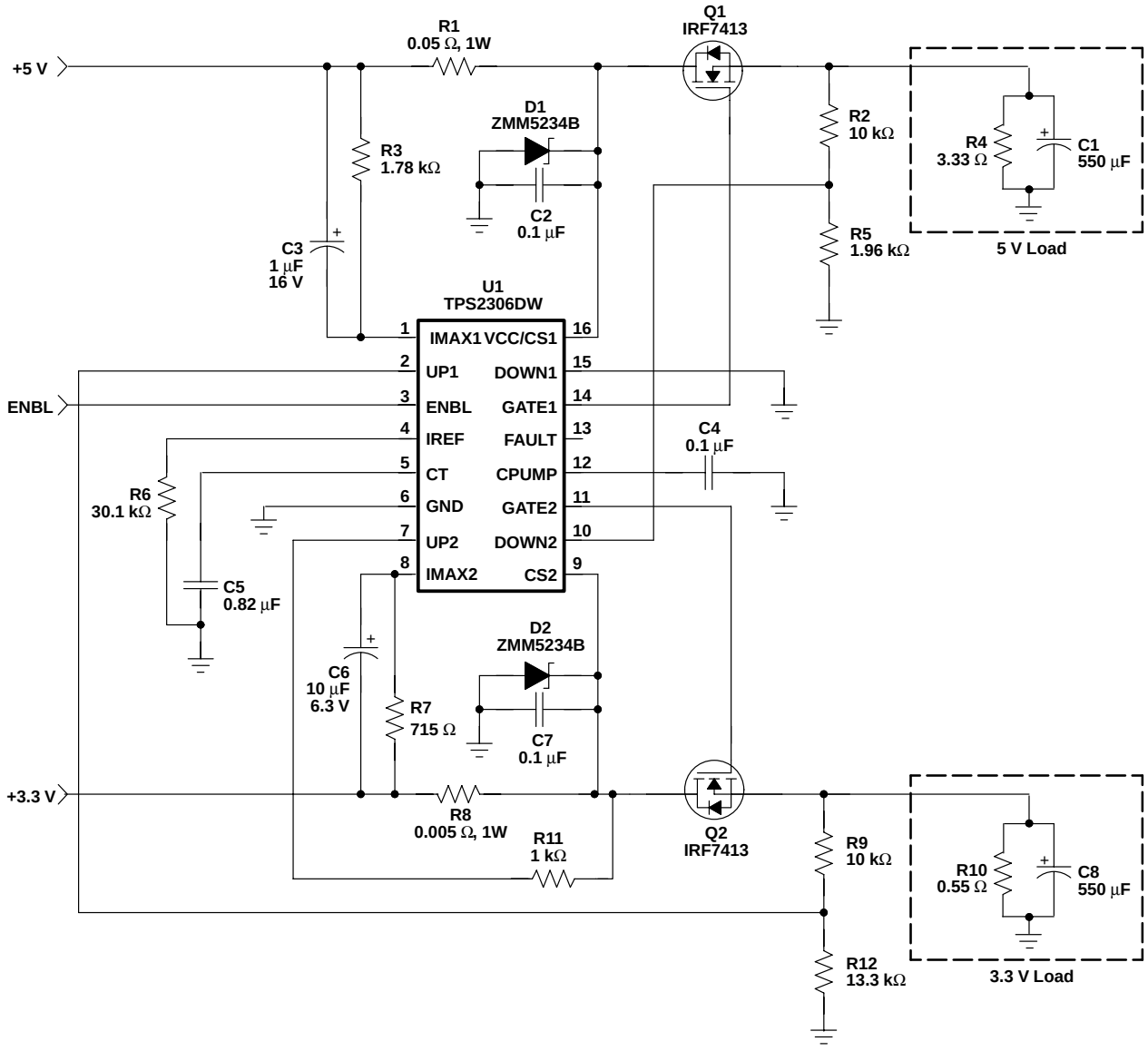


Figure 2. A Power Management Circuit That Meets the Specifications in Table 1

Channel 1 requires a higher voltage than channel 2 for the TPS2306 to operate correctly. For this reason, the 5-V supply drives channel 1 and the 3.3-V supply drives channel 2. The UP2 input ties high to disable turnon voltage sequencing for 3.3 V. The 3.3-V output ramps up when the ENBL input is asserted. Turnon of the 5-V channel is slaved to the 3.3-V output by the UP1 input. The 5-V output turns on when the 3.3-V output ramps up to 2.63 V. The DOWN1 input ties low to disable turnoff voltage sequencing for the 5-V channel. The 5-V output turns off when ENBL is de-asserted. Turn off of the 3.3-V channel is slaved to the 5-V output by way of the DOWN2 input. The 3.3-V output turns off as soon as the 5-V output decays to 3.05 V.

Although not required in all systems, Zener diodes D1 and D2 protect the TPS2306 from voltage spikes that can occur when the TPS2306 circuit breaker trips.

4 Component Selection

4.1 Select the Current-Sense Resistor R_{SNS} and Transistor Q_A

The 100-mV drop across the isolation circuit constrains the resistance of R_{SNS} and Q_A in Figure 1, so that

$$R_{ds(on)}\left(Q_A\right) + R_{SNS} \leq \frac{100\ mV}{I_{CL}(min)}\ ,\ \text{where } I_{CL}\ (min) \text{ is minimum current limit threshold.} \quad (5)$$

The resistor R_{SNS} voltage drop at current limit should be greater than the TPS2306 LCA input offset voltage to get reasonable current limit accuracy.

$$I_{CL}(min) \times R_{SNS} >> 5.5\ mV \quad (6)$$

The value of resistor R_{SNS} can increase to improve current-limit accuracy if there is a corresponding decrease in the transistor Q_A on-resistance to satisfy equation (5).

4.1.1 Select Resistor R_{SNS} and Transistor Q_A for the 5-V Channel

I_{CL}(min) is 1.5 A for the 5-V channel, so the isolation circuit resistance is less than 66.7 mΩ for this channel.

Choose a 10 mΩ IRF7413 MOSFET for transistor Q_A and a 50 mΩ resistor for R_{SNS} to satisfy equations (5) and (6) for the 5-V channel.

4.1.2 Select Resistor R_{SNS} and Transistor Q_A for the 3.3-V Channel

I_{CL}(min) is 6 A for the 3.3-V channel, so the isolation circuit resistance is less than 16.7 mΩ for this channel. Choose a 10 mΩ IRF7413 MOSFET for transistor Q_A and a 5 mΩ resistor for R_{SNS} satisfy equations (5) and (6) for the 3.3-V channel.

4.2 Set the I_{REF} Pin Current

Solve equation (1) and equation (4) for I_{REF} to get equation (7).

$$I_{REF} = \frac{R_{SNS}}{1.1 \times R_{OC}} \times \left(I_{OC} - I_{CL}\right) \quad (7)$$

For the 5 V channel,

$$I_{REF} = \frac{50\ m\Omega}{1.1 \times 2.5\ k\Omega} \times \left(I_{OC} - I_{CL}\right) = 1.82 \times 10^{-5} \times \left(I_{OC} - I_{CL}\right) \quad (8)$$

$$1.9\ A \leq \left(I_{OC} - I_{CL}\right) \leq 16.4\ A \text{ for } 35\ \mu A \leq I_{REF} \leq 300\ \mu A$$

For the 3.3-V channel,

$$I_{REF} = \frac{5\ m\Omega}{1.1 \times 2.5\ k\Omega} \times \left(I_{OC} - I_{CL}\right) = 1.82 \times 10^{-6} \times \left(I_{OC} - I_{CL}\right) \quad (9)$$

$$19\ A \leq \left(I_{OC} - I_{CL}\right) \leq 164\ A \text{ for } 35\ \mu A \leq I_{REF} \leq 300\ \mu A$$

The current I_{REF} controls the amount by which the over-current threshold exceeds the current-limit threshold. Clearly, the current I_{REF} should be as small as possible to avoid an excessively large over-current threshold. In this example, set the current I_{REF} to 50 μA so the I_{REF} programming resistor value is

$$R_{IREF} = \frac{1.5\ V}{I_{REF}} = \frac{1.5\ V}{50\ \mu A} \tag{10}$$

A standard resistance for R_{IREF} is 30.1 kΩ.

4.3 Select the Current-Limit Programming Resistor R_{CL}

The current limit threshold I_{CL} in equation (1) is valid for ideal components. In reality, components are imperfect and have errors that cause the current limit threshold to vary widely. Equation (11) accounts for these errors to prevent current limiting with a normal load.

$$1.1 \times I_{REF}(min) \times R_{CL}(min) - V_{IO(LCA)}(max) = I_{CL}(min) \times R_{SNS}(max) \tag{11}$$

where $V_{IO(LCA)}$ is the TPS2306 LCA input offset voltage.

4.3.1 Select Resistor R_{CL} for the 5-V Channel

$$R_{CL}(min) = \frac{I_{CL}(min) \times R_{SNS}(max) + V_{IO}(max)}{1.1 \times I_{REF}(min)} = \frac{1.5\ A \times (1.01 \times 50\ m\Omega) + 5.5\ mV}{1.1 \times \left(\frac{1.4\ V}{1.01 \times 30.1\ k\Omega}\right)} = 1.6\ k\Omega \tag{12}$$

For a 1% tolerance resistor,

$$R_{CL}(typ) = \frac{R_{CL}(min)}{0.99} = 1.62\ k\Omega \tag{13}$$

Therefore, choose a standard resistance of 1.78 kΩ for resistor R_{CL}.

4.3.2 Select Resistor R_{CL} for the 3.3-V Channel

$$R_{CL}(min) = \frac{I_{CL}(min) \times R_{SNS}(max) + V_{IO}(max)}{1.1 \times I_{REF}(min)}$$

$$= \frac{6\ A \times (1.01 \times 5\ m\Omega) + 5.5\ mV}{1.1 \times \left(\frac{1.4\ V}{1.01 \times 30.1\ k\Omega}\right)} = 706.7\ \Omega \tag{14}$$

$$R_{CL}(typ) = \frac{R_{CL}(min)}{0.99} = 713.8\ \Omega$$

Therefore, choose a standard resistance of 715 Ω for resistor R_{CL}.

4.4 Determine the Current-Limit Threshold Range

Include the linear current amplifier input offset voltage $V_{IO(LCA)}$ in equation (1) to get equation (15)

$$I_{CL} = \frac{1.1 \times I_{REF} \times R_{CL} + V_{IO(LCA)}}{R_{SNS}} \tag{15}$$

4.4.1 Calculate the Current-Limit Threshold Variation for the 5-V Channel

Using 1% tolerance resistors, the current limit variation for the 5-V channel is

$$I_{CL}(typ) = \frac{1.1 \times \left[\frac{1.5\ V}{30.1\ k\Omega}\right] \times 1.78\ k\Omega + 0\ mV}{50\ m\Omega} = 1.95\ A$$

$$I_{CL}(min) = \frac{1.1 \times \left[\frac{1.4\ V}{1.01 \times 30.1\ k\Omega}\right] \times 0.99 \times 1.78\ k\Omega - 5.5\ mV}{1.01 \times 50\ m\Omega} = 1.66\ A \quad (16)$$

$$I_{CL}(max) = \frac{1.1 \times \left[\frac{1.6\ V}{0.99 \times 30.1\ k\Omega}\right] \times 1.01 \times 1.78\ k\Omega + 5.5\ mV}{0.99 \times 50\ m\Omega} = 2.26\ A$$

4.4.2 Calculate the Current-Limit Threshold Variation for the 3.3-V Channel

Using 1% tolerance resistors, the current limit variation for the 3.3-V channel is

$$I_{CL}(typ) = \frac{1.1 \times \left[\frac{1.5\ V}{30.1\ k\Omega}\right] \times 715\ \Omega}{5\ m\Omega} = 7.84\ A$$

$$I_{CL}(min) = \frac{1.1 \times \left[\frac{1.4\ V}{1.01 \times 30.1\ k\Omega}\right] \times 0.99 \times 715\ \Omega - 5.5\ mV}{1.01 \times 5\ m\Omega} = 6.01\ A \quad (17)$$

$$I_{CL}(max) = \frac{1.1 \times \left[\frac{1.6\ V}{0.99 \times 30.1\ k\Omega}\right] \times 1.01 \times 715\ \Omega + 5.5\ mV}{0.99 \times 5\ m\Omega} = 9.73\ A$$

The 5-V and 3.3-V channels can handle a continuous current of 1.66 A and 6.01 A, respectively. This performance meets the specification in Table 1.

4.5 Calculate the Over-Current Threshold Range

The TPS2306 data sheet specifies the over-current amplifier input offset voltage $V_{IO(OCA)}$. In general, equation (4) can be written as

$$I_{OC} = \frac{1.1 \times I_{REF} \times R_{CL} + V_{IO(OCA)}}{R_{SNS}} \quad (18)$$

The TPS2306 data sheet specifies the over-current comparator input offset voltage $V_{IO(OCA)}$.

4.5.1 Calculate the Over-Current Threshold Variation for the 5-V Channel

Using 1% tolerance resistors, the over-current threshold variation for the 5-V channel is

$$I_{OC}(typ) = \frac{1.1 \times \left[\frac{1.5\ V}{30.1\ k\Omega}\right] \times (1.78\ k\Omega + 2500\ \Omega)}{50\ m\Omega} = 4.69\ A$$

$$I_{OC}(min) = \frac{1.1 \times \left[\frac{1.4\ V}{1.01 \times 30.1\ k\Omega}\right] \times 0.99 \times 1.78\ k\Omega + 0.6 \times \left[\frac{1.4\ V}{1.01 \times 30.1\ k\Omega}\right] \times 2500\ \Omega}{1.01 \times 50\ m\Omega} = 3.14\ A \quad (19)$$

$$I_{OC}(max) = \frac{1.1 \times \left[\frac{1.6\ V}{0.99 \times 30.1\ k\Omega}\right] \times 1.01 \times 1.78\ k\Omega + 1.5 \times \left[\frac{1.6\ V}{0.99 \times 30.1\ k\Omega}\right] \times 2500\ \Omega}{0.99 \times 50\ m\Omega} = 6.21\ A$$

4.5.2 Calculate the Over-Current Threshold Variation for the 3.3-V Channel

Using 1% tolerance resistors, the over-current threshold variation for the 3.3-V channel is

$$I_{OC}(typ) = \frac{1.1 \times \left[\frac{1.5\ V}{30.1\ k\Omega}\right] \times (715\ \Omega + 2500\ \Omega)}{5\ m\Omega} = 35.2\ A$$

$$I_{OC}(min) = \frac{1.1 \times \left[\frac{1.4\ V}{1.01 \times 30.1\ k\Omega}\right] \times 0.99 \times 715\ \Omega + 0.6 \times \left[\frac{1.4\ V}{1.01 \times 30.1\ k\Omega}\right] \times 2500\ \Omega}{1.01 \times 5\ m\Omega} = 20.8\ A \quad (20)$$

$$I_{OC}(max) = \frac{1.1 \times \left[\frac{1.6\ V}{0.99 \times 30.1\ k\Omega}\right] \times 1.01 \times 715\ \Omega + 1.5 \times \left[\frac{1.6\ V}{0.99 \times 30.1\ k\Omega}\right] \times 2500\ \Omega}{0.99 \times 5\ m\Omega} = 49.3\ A$$

4.6 Determine the Value of the Turn-On Current Slew-Rate Capacitor, C_{SS}

The maximum output current slew rate is given by equation (21).

$$\left.\frac{\partial I_{OUT}(t)}{\partial t}\right|_{t=0+} = \frac{I_{CL}(max)}{R_{CL}(min) \times C_{SS}(min)}$$

$$C_{SS}(min) = \frac{I_{CL}(max)}{R_{CL}(min) \times \frac{\partial I_{OUT}}{\partial t}(max)} \quad (21)$$

4.6.1 Select Capacitor C_{SS} for the 5-V Channel

$$C_{SS}(min) = \frac{2.26\ A}{0.99 \times 1.78\ k\Omega \times 1.5\ A/ms} = 0.85\ \mu F \quad (22)$$

For a 10% tolerance capacitor,

$$C_{SS}(typ) = \frac{C_{SS}(min)}{0.9} = \frac{0.85\ \mu F}{0.9} \approx 1\ \mu F \quad (23)$$

4.6.2 Select Capacitor C_{SS} for the 3.3-V Channel

$$C_{SS}(\text{min}) = \frac{9.73\ \text{A}}{0.99 \times 715\ \text{k}\Omega \times 1.5\ \text{A/ms}} = 9.2\ \mu\text{F} \tag{24}$$

For a 10% tolerance capacitor,

$$C_{SS}(\text{typ}) = \frac{C_{SS}(\text{min})}{0.9} = \frac{9.2\ \mu\text{F}}{0.9} \approx 10\ \mu\text{F} \tag{25}$$

4.7 Select the Fault Timing Capacitor

The fault timing capacitance must be large enough so that the load voltages ramp up without tripping the circuit breaker in a no fault. The timing capacitance can be determined by plotting the turnon voltage for each output.

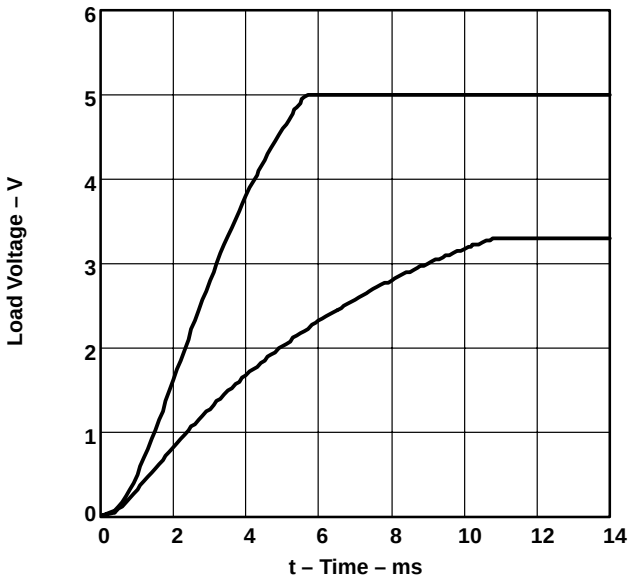
Solve equations (2) and (26) for $V_{OUT}(t)$ to get equation (27)

$$I_{OUT}(t) = C_L \times \frac{\partial V_{OUT}(t)}{\partial t} + \frac{V_{OUT}(t)}{R_L} \tag{26}$$

$$V_{OUT}(t) = I_{CL} \times R_L \times \left(\left[1 - e^{-t/\tau_L} \right] + \frac{\tau_{SS}}{\tau_L + \tau_{SS}} \times \left[e^{-t/\tau_{SS}} - e^{-t/\tau_L} \right] \right) \tag{27}$$

where $\tau_{SS} = R_{CL} \times C_{SS}$ and $\tau_L = R_L \times C_L$.

Equation (27) describes the turnon voltage across a parallel R-C load. Figure 3 plots equation (27) for the 5-V and 3.3-V outputs.



NOTE: The 5-V load is a 550 μF capacitor in parallel with a 3.33 Ω resistor, and the 3.3-V load is a 550 μF capacitor in parallel with a 0.55 Ω resistor.

Figure 3. Plot of Equation (27) for the 5-V and 3.3-V Outputs

The TPS2306 wakes up in 0.5 ms when the ENBL input is asserted. The 3.3-V output then rises from 0 V to 2.6 V in 7 ms (see Figure 3) and triggers the TPS2306 UP1 comparator, allowing the 5-V output to rise. The 5-V output rises from 0 V to its steady state value in 5.6 ms (see Figure 3). A 50-μA source charges the fault timing capacitor while the output voltages ramp up. The fault time-out in equation (28) then sets the fault timer capacitance in equation (29).

$$T > (0.5 + 7 + 5.6)\ \text{ms} = 13.1\ \text{ms} \tag{28}$$

$$C_t(\text{min}) = \frac{i_{chg}(\text{max}) \times T}{V_{th}(\text{min})} = \frac{65\ \mu\text{A} \times 13.1\ \text{ms}}{1.35\ \text{V}} = 0.63\ \mu\text{F} \tag{29}$$

If the fault timing capacitance 0.82 μF ± 10%, then the fault time is

$$\tau_f(\text{typ}) = \frac{C_t\ (\text{typ}) \times V_{th}(\text{typ})}{i_{chg}(\text{typ})} = \frac{0.82\ \mu\text{F} \times 1.5\ \text{V}}{50\ \mu\text{A}} = 25\ \text{ms} \tag{30}$$

This analytic technique for calculating the fault timing capacitance is a laborious process to be used if a breadboard is not available. If a breadboard is available, however, the fault timing capacitance can be calculated from the measured value of equation (28) with the C_t pin grounded to disable the TPS2306 fault timer. This empirical technique is much faster than the analytic technique for calculating the fault timing capacitance.

4.8 Design the UP/DOWN Voltage Dividers, $R_1 – R_4$

The UP input voltage divider satisfies equation (31) if the turnon trigger voltage is V_{T1}.

$$\frac{R_1}{R_2} = \left(\frac{V_{T1}}{1.5\ \text{V}} - 1\right) \tag{31}$$

Likewise, the DOWN input voltage divider satisfies equation (32) if the turnoff trigger voltage is V_{T2}.

$$\frac{R_3}{R_4} = \left(\frac{V_{T2}}{0.5\ \text{V}} - 1\right) \tag{32}$$

4.8.1 Select Resistors $R_1 – R_4$ for the 5-V Channel

Table 1 specifies a 2.63-V turnon trigger threshold for the 5-V channel, so

$$\frac{R_1}{R_2} = \left(\frac{2.63\ \text{V}}{1.5\ \text{V}} - 1\right) = 0.753 \tag{33}$$

A 10-kΩ value for resistor R_1 and a 13.3-kΩ value for resistor R_2 satisfy Equation (33).

The 5-V channel requires no turnoff voltage sequencing so the DOWN input ties to ground.

4.8.2 Select Resistors $R_1 – R_4$ for the 3.3-V Channel

Table 1 specifies a 3.05-V turnoff trigger threshold for the 3.3-V channel, so

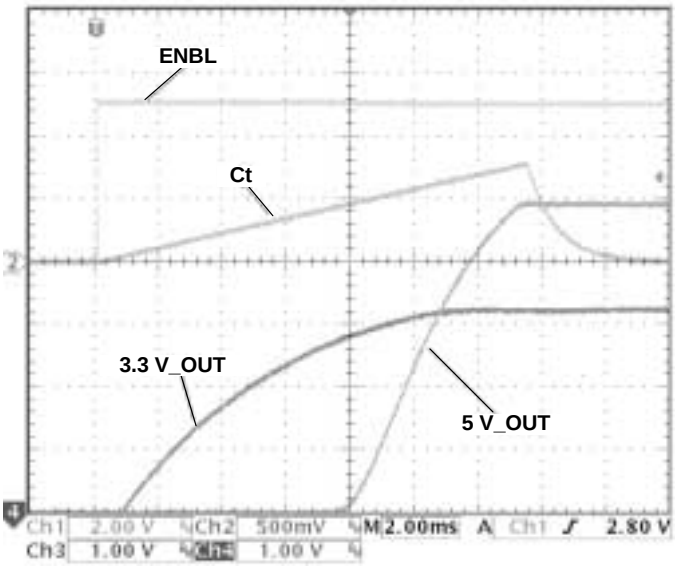
$$\frac{R_3}{R_4} = \left(\frac{3.05\ \text{V}}{0.5\ \text{V}} - 1\right) = 5.1 \tag{34}$$

A 10-kΩ value for resistor R_3 and a 1.96-kΩ value for resistor R_4 satisfy equation (34).

The 3.3-V channel requires no turnon voltage sequencing so the UP input ties to 3.3 V.

5 Actual Circuit Performance

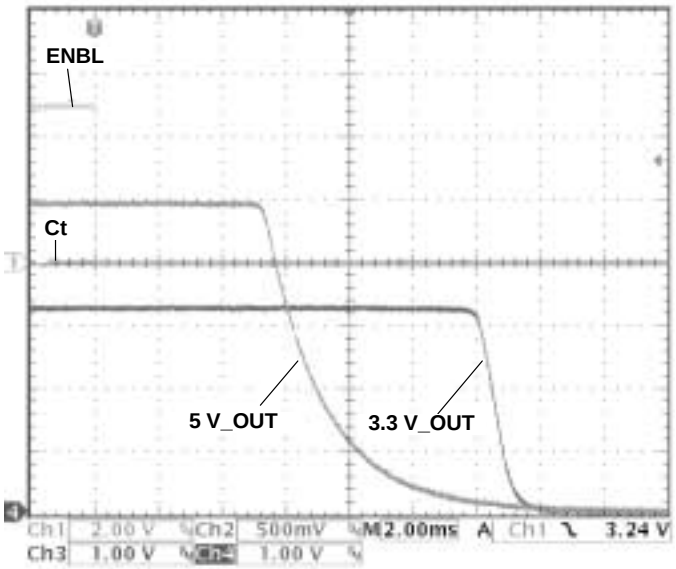
Measurements validate the TPS2306 design.



NOTE: The 5-V load is a 550-µF capacitor in parallel with a 3.33-Ω resistor and the 3.3-V load is a 550-µF capacitor in parallel with a 0.55-Ω load.

Figure 4. Turnon Output Voltages

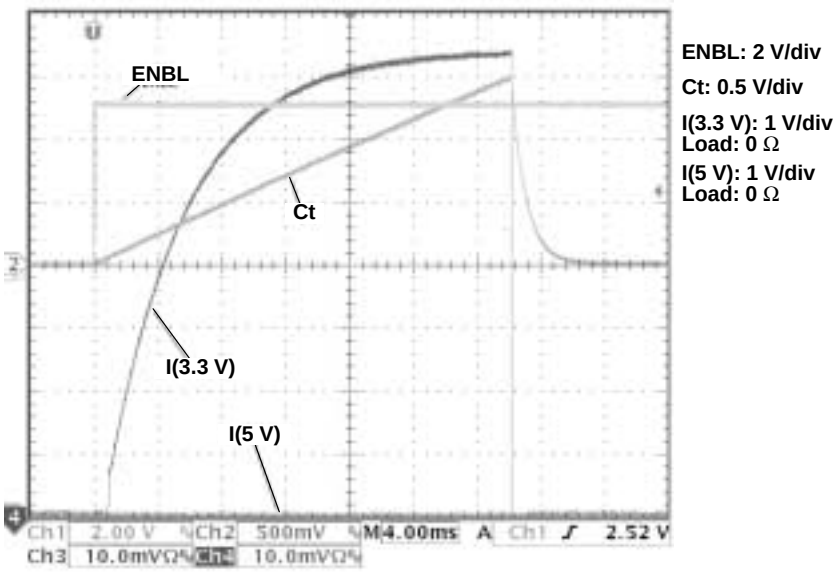
The 3.3-V output rises in Figure 4 when the TPS2306 ENBL input is asserted. When the output voltage reaches 2.63 V, it triggers the turnon of the 5-V channel. The load voltages ramp up before capacitor C_t charges to the 1.5-V fault threshold, so the circuit breaker does not trip. The output voltages reach steady state in 13.2 ms after the rising edge of the ENBL input, which compares favorably with the analysis result in equation (28).



NOTE: The 5-V load is a 550-µF capacitor in parallel with a 3.33-Ω resistor and the 3.3-V load is a 550-µF capacitor in parallel with a 0.55-Ω load.

Figure 5. Turnoff Output Voltages

An on-chip charge pump provides 20 V of gate drive to the FET switch. The TPS2306 discharges the 5-V FET gate with 10 μA if the ENBL input is de-asserted. The gate must discharge to 8 V before the 5-V FET switch can turn off. The gate discharge time causes a 5.2-ms turnoff delay in the 5-V FET switch (see Figure 5). When the 5-V output falls below 2.63 V, it triggers turnoff of the 3.3-V channel. Likewise, the gate discharge time causes a 4-ms turnoff delay in the 3.3-V output.



NOTE: The 5-V load is a 550-μF capacitor in parallel with a 3.33-Ω resistor.

Figure 6. Turnon Current Into a 3.3-V Load Fault

Figure 6 shows the output turnon current. A short circuit simulates a fault at the 3.3-V output. The circuit limits the 3.3-V output current to 7.5 A. The 3.3-V output never ramps to the turnon trigger threshold of the 5-V channel (i.e., 2.63 V), so the 5-V output does not turn on. The 3.3-V FET always operates in the linear region in this example, so capacitor C_t charges to 1.5 V and trips the TPS2306 circuit breaker.

6 Summary

The TPS2306 sequences the supply voltages, limits inrush current, and provides fault protection to effectively manage power to a dual supply voltage system. A 2.75-V through 13.6-V operating range allows the TPS2306 to handle a wide variety of applications like those requiring 12 V and 5 V, or 12 V and 3.3 V. In any application, the higher supply voltage must drive channel 1, and Zener diodes D1 and D2 (see Figure 2) must have the appropriate voltage rating. Systems that have more than two positive supply voltages can cascade multiple TPS2306 devices to manage system power. Proper power management reduces component stress and improves system reliability.

7 References

TPS2306 data sheet, *Dual Sequencing Hot Swap Power Manager* (SLVS368).

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