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Introduction

Analog Applications Journal is a collection of analog application articles designed to give readers a basic understanding of TI products and to provide simple but practical examples for typical applications. Written not only for design engineers but also for engineering managers, technicians, system designers and marketing and sales personnel, the book emphasizes general application concepts over lengthy mathematical analyses.

These applications are not intended as "how-to" instructions for specific circuits but as examples of how devices could be used to solve specific design requirements. Readers will find tutorial information as well as practical engineering solutions on components from the following product categories:

- Data Acquisition
- Power Management
- Interface (Data Transmission)
- Audio Amplifiers

Where applicable, readers will also find software routines and program structures. Finally, *Analog Applications Journal* includes helpful hints and rules of thumb to guide readers in preparing for their design.

Intelligent sensor system maximizes battery life: Interfacing the MSP430F123 Flash MCU, ADS7822, and TPS60311

By Mark Buccini
MSP430 Applications Manager

Introduction

This article describes how to use event-driven techniques to maintain the lowest possible power consumption in single-cell, battery-powered intelligent sensor applications. These applications detect such things as glass breakage, sound level, fire, and smoke. The same applications include a microcontroller unit (MCU) to control the system and a high-resolution, analog-to-digital converter (ADC) to search periodically for interesting real-time sensor output signals. To extend battery life, system power consumption must be managed to the absolute lowest possible level. To reduce power consumption, intuition points to a slowly operating data acquisition solution. On the surface this intuitive approach seems reasonable; but it is misleading, especially when analog circuitry is involved. Although power consumption does typically scale with conversion rate, it will be demonstrated that extending system time in standby modes is the largest contributor to total power reduction. Activity must occur as fast as possible in short "bursts," allowing the system to return quickly to a standby mode. A micropower intelligent sensor system using the MSP430F123 Flash MCU, ADS7822 12-bit ADC, and a single-cell TPS60311 dc/dc boost converter is examined. The entire system is powered from a common 1.5-V AA battery. See Figure 1.

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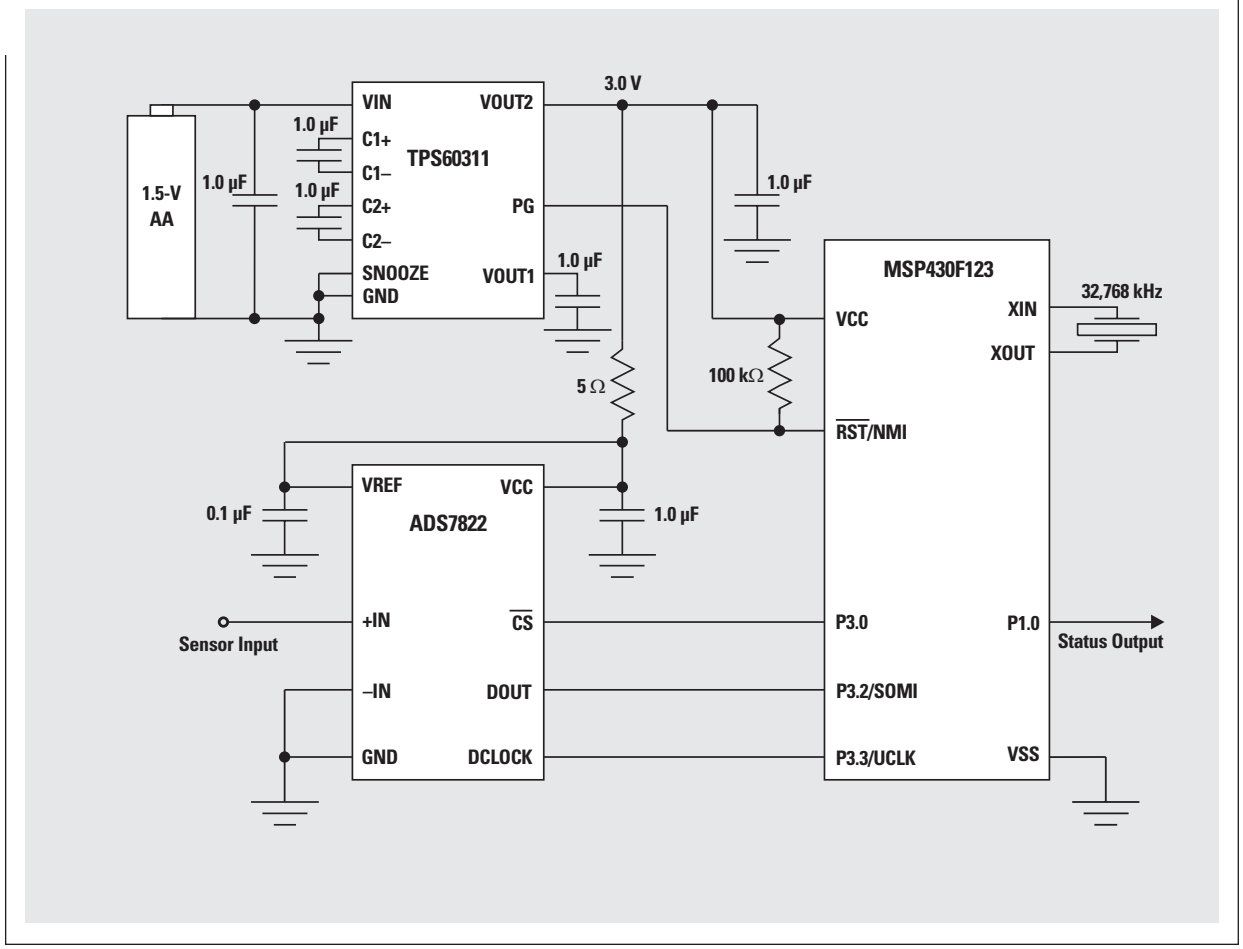
Figure 1. System solution using MSP430F123, ADS7822, and TPS60311



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Enabling single-cell, 3-year battery life

The example examined is powered from a single 1.5-V AA alkaline battery with a typical usable energy value of 1,000 mAh. If the application has a targeted 3-year battery life, total current consumption must be managed as follows:

1,000 mAh/3 years/365 days/24 hours = 38.0 µA.

The example presented also assumes that the sensor must be sampled at a 2-ms interval (512 samples per second) to acquire the necessary real-time data to detect an event such as glass breakage.

Serial interface

The interface between the MSP430F123 MCU and ADS7822 ADC is glueless. The MCU's integrated USART peripheral is used in SPI master mode to drive communication with the ADC. The USART clock (UCLK) is provided to the ADC (DCLOCK), and receives data on the slave out master (SOMI) from the ADC digital output DOUT. In the example, software uses port pin P3.0 to control the ADC chip select ($\overline{CS}$). Any available port pin can be used. With $\overline{CS}$ and software, the MCU directly enables and disables the ADC. The ADS7822 provides 15 bits of data: 2 bits for sampling, 1 null bit, and 12 bits of conversion code. Typically, SPI serial communication exchanges data as 8-bit bytes. To transfer the 15 bits from ADS7822 to the MSP430, two 8-bit transfers are made back-to-back and packed into a single 16-bit word by using software. The word data is rotated right to eliminate the erroneous extra bit and is then AND'ed with 0FFFh to expose only the interesting 12 bits of ADC conversion code. The result is right justified.

The MCU enables the ADC by resetting $\overline{CS}$. The conversion is started and timed with 16 bits of data exchanged by writing two dummy bytes back-to-back to the USART transmit buffer (TXBUF). TXBUF is double buffered, so back-to-back 8-bit writes will transfer a total of 16 bits. Though no data is actually transmitted from the MCU, writing to TXBUF automatically initiates a complete bidirectional SPI transfer, including UCLK generation that is required by the ADC DCLOCK. The data transmit function of the USART is simply ignored. After the first 8-bit byte of data is received from the ADC into the USART shift register, it is transferred automatically to the receive buffer (RXBUF). The second byte of data is automatically received next as software is recovering the first byte from RXBUF. The second byte of data is recovered; then the 16-bit result is packed into register R15. See Figure 2.

Slow operating system analysis

First consider the intuitive approach to saving power; that is, simply clock the entire system slow from the available 32-kHz watch crystal. With the MSP430 CPU master clock (MCLK) clocked continuously at 32 kHz, current consumption is approximately 10–12 µA. With this slow clocking, the MCU will be essentially 100% active in order to complete the required sample and decision loop at the 2-ms interval. No standby modes are possible. The SPI UCLK at 1,6384 Hz (32,768/2) can conveniently clock the ADC DCLOCK. With 16 clocks per sample, the ADC can complete a conversion in approximately 1 ms, leaving 1 ms for power-down and time for the MCU to complete the calculation. The active current of the ADS7822 is approximately 200 µA. Powered down, the ADC current consumption is a negligible 50 nA. The MCU will be 100% active, and the ADC 50% active.

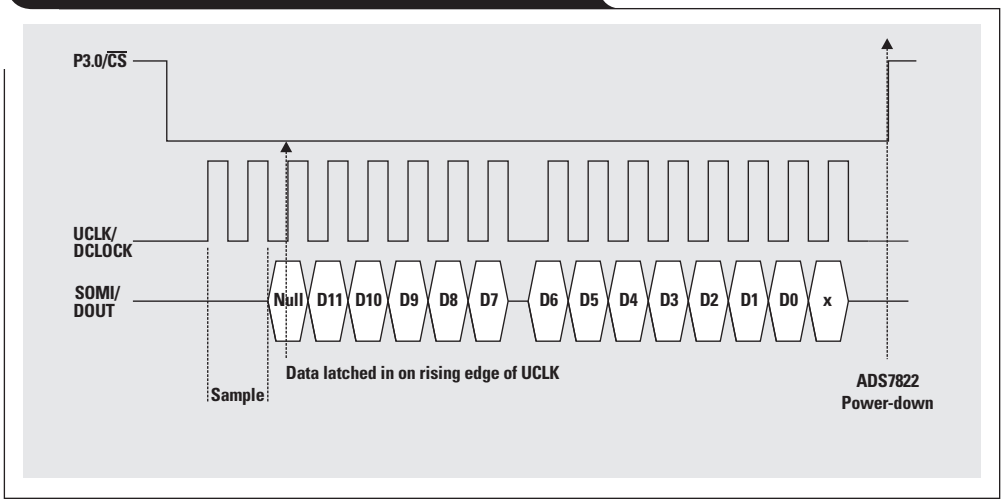
In snooze mode, quiescent current of the TPS60311 dc/dc charge pump is 2.0 µA typical and can deliver 2 mA to the system. Since the system should never use more than 2 mA, and the 2-µA TPS60311 snooze current will be a constant draw, snooze should be the only mode ever used.

With slow (32-kHz) processing, the system consumes an average current as calculated:

$$I_{BAT} = \text{MCU} + \text{ADC} + \text{dc/dc}$$
$$= (10\ \mu A \times 1.00) + (200\ \mu A \times 0.50) + (2\ \mu A)$$
$$= 10\ \mu A + 100\ \mu A + 2\ \mu A$$
$$= 112\ \mu A.$$

At an average current consumption of 112 µA, the system exceeds the 38-µA maximum for 3-year, single-cell battery life. The most significant current consumption is the 50%

Figure 2. MSP430F123/ADS7822 serial timing



active duty cycle for the ADC. The analog circuitry of the ADC is the prime current consumer and is largely unaffected by speed of conversion. The ADC's total current consumption is approximately 200 µA and is almost unchanged over the full DCLOCK range of operation at 10 kHz–1.2 MHz. With this in mind, it makes sense to convert as fast as possible and spend as much time as possible in power down. With a slow 32-kHz MCLK, the MCU is 100% active; no standby mode is possible and no processing bandwidth available for increased digital signal processing or additional sensor sampling.

Burst mode system analysis

Next consider a burst technique—fast, short active-mode intervals with extended system time in standby. The MSP430 is clocked by a single 32-kHz watch crystal that drives an internal auxiliary clock (ACLK). The ACLK is used in the example to drive only the watchdog timer (WDT), configured by software as a 2-ms-interval timer. As configured, the MCU operates normally in low-power mode 3 (LPM3) with only the ACLK and WDT interrupt active. At the programmed 2-ms interval, the WDT interrupts the system and activates the CPU, which is then driven by a high-speed MCLK clocked from the on-chip digitally controlled oscillator (DCO). It is important to note that the fast-starting DCO also allows the MCU to move from standby to high-speed active mode in less than 6 µs. The DCO has been configured by software to operate in the 1-MHz range. The sub-master clock (SMCLK) used by the USART has also been configured to clock from the DCO.

As defined by the programmed WDT interrupt interval, the ADC is sampled and a decision made every 2 ms.

The ADC measurement and decision code requires approximately 70 active CPU MCLK clocks. At 512 measurements/decisions per second, the CPU is active a total of 70 × 512 = 35,840 clocks per second. Assuming that the CPU is clocked at 1 MHz (1 µs per clock), the active duty cycle for the CPU is 35,840/1,000,000 = 3.5%. The MCU active current is approximately 300 µA. The standby mode LPM3 current is 1.6 µA and is dominant 96.5% of the application time. Using a 500-kHz DCLOCK (1 MHz/2), the system samples the ADS7822 512 times per second, with each sample taking 16 clocks. The ADC will be 1.6% active and 98.4% powered down.

For maximum power conservation, the MCU manages the system such that MCU and ADC spend the vast majority of time in standby mode, with an average standby current consumption of all components ~ 3.6 µA.

With a burst-mode technique, the system consumes an average current as calculated:

$$I_{BAT} = \text{MCU} + \text{ADC} + \text{dc/dc}$$

$$= (1.6\ \mu A \times 0.965 + 300\ \mu A \times 0.035) + (200\ \mu A \times 0.016) + (2.0\ \mu A)$$

$$= 11.54\ \mu A + 3.2\ \mu A + 2\ \mu A$$

$$= 17.2\ \mu A.$$

With burst-mode programming, the system consumes an average current of only 17.2 µA and easily surpasses the target of 38.0 µA required for 3-year battery life. The additional power reserve can be used to compensate for other requirements such as faster sampling, sensor signal conditioning, or weak/leaky batteries. Also, the current budgeting does not take into account the power required to support the activity if a trigger event occurs—i.e., glass breakage or fire detection. It is thought that these events would be very rare and clearly the exception to normal operation.

Further reduction in power consumption

It has been demonstrated that managing the system active duty cycle is of utmost importance for reducing power consumption in intelligent sensing applications. The primary goal should be to minimize active time and maximize time in standby and power-down modes. MCU code execution should be fast and efficient. MCU activity should be event-driven and use interrupts that identify the code to be executed as fast as possible; i.e., avoid cycle-wasting subroutine calls, polling, and bit-test skip chains. The watch crystal and DCO combination is ideal for battery-powered applications, providing both an ultra-low-power standby mode and a fast processor clock. The fact that the DCO can start and is stable in less than 6 µs provides very large power savings by reducing start-up time. The start-up time for a typical crystal or resonator is in the 10-ms range—time that would be wasted and consume significant power. Using the DCO can reduce standby-to-active wake-up time by over 1000×.

The ADC must also be powered down as long as possible. If more limited resolution data can be used, consider short cycling. That is, inspect only the first 8 bits of ADC conversion code (which represent the 5 MSB of the conversion) in the first of two SPI transfers required for a complete conversion. Determine if the first 5 bits are interesting; if not, terminate the second SPI transfer to power down the ADC.

In all cases, if a voltage regulator or step-up converter is used, reduce system V_{CC} as much as possible. All components will use less power at a lower V_{CC}.

Description of the demonstration program

The code is short, interrupt-driven, and programmed in assembler. This combination ensures that the MCU executes code as fast and effectively as possible with no power-wasting extra cycles.

The demonstration firmware is coded with a `Mainloop` and single active WDT interrupt service routine (ISR). Three MSP430F123 USART pins on port 3 are used to interface with the ADS7822 ADC, and port 1 pin P1.0 is used as a status indicator. All MSP430 port pins default to the input direction. In a final application, unused pins should be configured to the output direction to avoid power-consuming floating inputs.

The code demonstration firmware first initializes the peripherals. Next, inside the `Mainloop`, setting the appropriate bits in the CPU status register (SR) forces the processor to enter LPM3:

```
Mainloop    bis.w   #LPM3,SR     ; Enter LPM3
```

The CPU, DCO, and code execution halt at this point, but the pre-configured 2-ms WDT ISR is active with the timer clocked by the 32-kHz ACLK. It is at this point that the code spends the vast majority of time with the MCU and ADC in a battery-conserving standby mode; only the ACLK and WDT are active.

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As with all MSP430 ISRs, the program counter (PC) and SR are automatically saved on the stack, and the CPU is returned to active. This ensures that the ISR can always be processed, even from a low-power mode. The ISR places the WDT vector on the PC, and code execution begins. Inside the WDT ISR, P3.0 resets $\overline{CS}$, enabling the ADS7822. The ADC is sampled and then $\overline{CS}$ is set, returning the ADC to power-down. For demonstration purposes, if the 12-bit ADC code is greater than 2,048, the `Mainloop` is made active after the WDT ISR by clearing the LPM3 bit on the top of the stack (TOS) that holds the previous SR. Manipulating the PC on the TOS is an excellent technique for using events to manage system activity and low-power modes.

```
bic.w   #LPM3,0(SP) ; Exit LPM3 on reti
```

An active `Mainloop` will toggle port pin P1.0, indicating a trigger to action in a user application. If the ADC code is less than 2,048, the system returns to LPM3. The WDT ISR operates continuously at the programmed 2-ms interval. In an actual end application, a more complex decision/action than a simple comparison/pin toggling could be made when the sensor data is interesting.

References

For more information related to this article, you can download an Acrobat Reader file at www-s.ti.com/sc/techlit/*litnumber* and replace *"litnumber"* with the **TI Lit. #** for the materials listed below.

Document Title	**TI Lit. #**
1. MSP430x1xx Family User's Guide	slau049
2. "MSP430x12x Mixed Signal Microcontroller," Data Sheet	slas312
3. "12-Bit High-Speed 2.7 V microPower Sampling Analog-to-Digital Converter," ADS7822 Data Sheet	sbas062
4. "TPS60310, TPS60311, TPS60312, TPS60313 Single-Cell to 3-V/3.3-V, 20-mA Dual Output, High-Efficiency Charge Pump with Snooze Mode," Data Sheet	slvs362

Related Web sites

www.ti.com/sc/docs/products/analog/*device***.html**
Replace *device* with ads7822, msp430f123 or tps60311

MSP430F123/ADS7822 demonstration program

```
#include  "msp430x12x.h"
;-------------------------------------------------------------------------------
            ORG     0E000h                          ; Program Start
;-------------------------------------------------------------------------------
RESET       mov.w   #0300h,SP                       ; Initialize 'x12x stack
SetupWDT    mov.w   #WDT_ADLY_1_9,&WDTCTL           ; WDT 1.9ms, ACLK, interval timer
            bis.b   #WDTIE,&IE1                     ; Enable WDT interrupt
SetupDCO    mov.b   #0C0h,&DCOCTL                   ; DCO~1MHz
SetupP1     bis.b   #01h,&P1DIR                     ; P1.0 output direction
SetupP3     bis.b   #0Eh,&P3SEL                     ; P3.1-3 SPI option select
            bis.b   #01h,&P3DIR                     ; P3.0 output direction
SetupSPI    bis.b   #USPIE0,&ME2                    ; Enable USART0 SPI
            bis.b   #CKPH+SSEL1+SSEL0+STC,&UTCTL0 ; SMCLK, 3-pin mode
            mov.b   #CHAR+SYNC+MM,&UCTL0            ; 8-bit SPI Master **clear SWRST**
            mov.b   #02h,&UBR00                     ; SMCLK/2 for baud rate
            clr.b   &UBR10                          ;
            clr.b   &UMCTL0                         ; Clear modulation
            eint                                    ; Enable interrupts
                                                    ;
Mainloop    bis.w   #LPM3,SR                        ; Enter LPM3
ON          bis.b   #001h,&P1OUT                    ; P1.0 = 1 - LED ON
OFF         bic.b   #001h,&P1OUT                    ; P1.0 = 0 - LED OFF
            jmp     Mainloop                        ;
                                                    ;
```

MSP430F123/ADS7822 demonstration program (Continued)

```
;-------------------------------------------------------------------------------
WDT_ISR;
;-------------------------------------------------------------------------------
Meas_7822  bic.b   #CS,&P3OUT                  ; /CS reset, enable ADC
           mov.b   #00h,&TXBUF0                ; Dummy write to start SPI
           mov.b   #00h,&TXBUF0                ; Dummy write to start SPI
           bic.b   #URXIFG0,&IFG2              ; Clear errant RXBUF flag
RX_MSB     bit.b   #URXIFG0,&IFG2              ; RXBUF ready?
           jnc     RX_MSB                      ; 1 = empty
           mov.b   &RXBUF0,R15                 ; R15 =  00|MSB
           swpb    R15                         ; R15 = MSB|00
RX_LSB     bit.b   #URXIFG0,&IFG2              ; RXBUF ready?
           jnc     RX_LSB                      ; 1 = empty
           bis.b   #CS,&P3OUT                  ; /CS set, disable ADC
           mov.b   &RXBUF0,R14                 ; R14 =  00|LSB
           add.w   R14,R15                     ; R15 = MSB|LSB
           rrc.w   R15                         ;
           and.w   #0FFFh,R15                  ; Keep only databits
           cmp.w   #2048,R15                   ;
           jlo     No_action                   ; jump if 2048 < R15
           bic.w   #LPM3,0(SP)                 ; Exit LPM3 on reti
No_action  reti                                ;
                                               ;
;-------------------------------------------------------------------------------
;          Interrupt Vectors Used MSP430F12x
;-------------------------------------------------------------------------------
           ORG     0FFFEh                      ; MSP430 RESET Vector
           DW      RESET                       ;
           ORG     0FFF4h                      ; WDT Vector
           DW      WDT_ISR                     ;
           END
```

Power control design key to realizing InfiniBand℠ benefits

By Jonathan M. Bearfield
Power Interface Product Line Manager

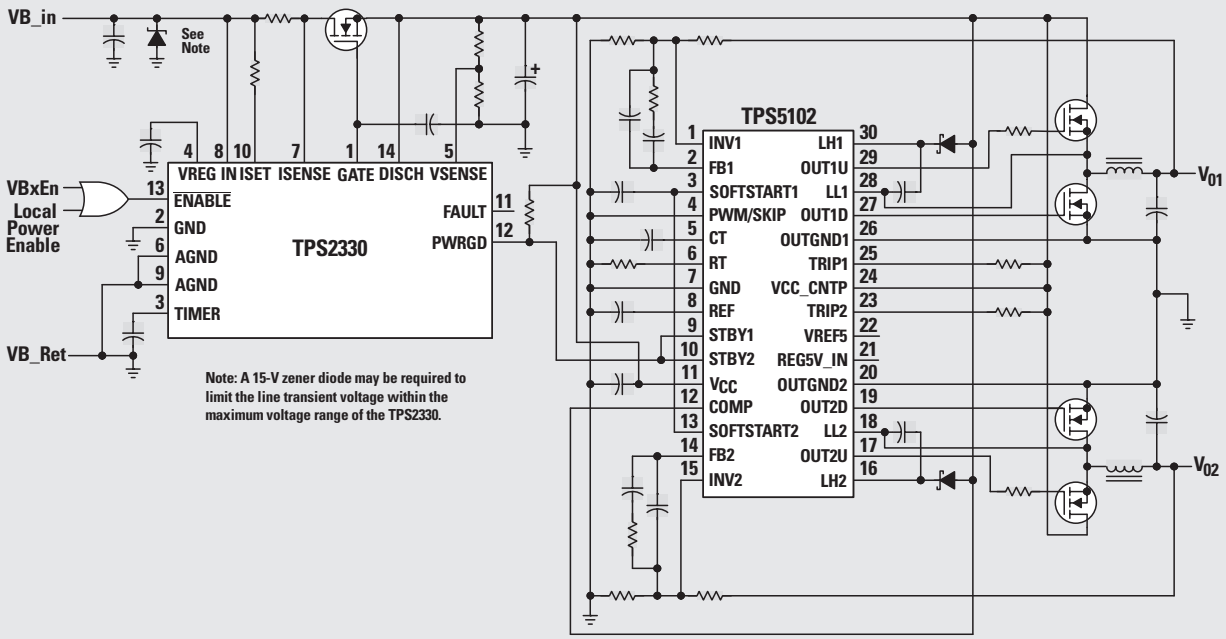
The InfiniBand technology is a modularly scalable switched-fabric architecture. It currently uses a 2.5-Gbit/sec bidirectional serial point-to-point interface whose roadmap extends from 500 Mbit/sec out to 6 Gbit/sec, with auto-speed sensing. It was defined to solve many of the problems seen in the parallel interconnects of today's servers and system area networks; and a great deal of time and effort has gone into defining the digital interface and control structure. However, the details of implementing appropriate power control have been left up to the designer.

From a power perspective, InfiniBand is a true hot-plug implementation. Power is not only applied to the main system during module insertion and removal but is also present at the connector. This is not true for compact PCI, PCIx, PCMCIA or most other hot-plug applications. The fact that this is a truly hot-swappable socket creates significant hurdles and places several limitations on the power interface designers. There is a need to manage and optimize inrush currents, system voltage droops, and module and backplane capacitance. The designer also needs to determine the level of fault protection required in both the system and the module.

The InfiniBand specification defines two power connections for the modules. The first is bulk power. It is a 12-V (±2 V), 2.5-A supply that is intended for all of the major functions of the module. The second is auxiliary power. It is a 5-V (±5%), 260-mA supply intended for standby or configuration modes of operation, but it can be implemented as the only supply required by the card for operation. Due to its low power, the auxiliary power rail is a rather straightforward implementation, especially since the card is always allowed to draw power from it. On the other hand, the bulk power rail can provide up to 50 W to a module, depending on the module's size and power configuration. Along with this, there are several modes of operation where the bulk power load on the card must be turned off.

In order for the bulk power hot-swap power management (HSPM) solution to be effective, it must have logic level controls and reporting capabilities. It is important for the

Figure 1. InfiniBand bulk power solution



HSPM to control the rise times of the power FETs in the circuit, limit current to the load, and report overloaded conditions to the system. In order to maintain a clean and stable power rail on the card, considerable capacitance may be required. This means that the HSPM selected must be able to turn on into a highly capacitive load and manage the di/dt demand characteristics of the circuit.

Managing the 12-V bulk power rail during the hot insertion and removal of modules is, however, only half of the solution. As most circuitry no longer runs at 12 V, it will be necessary to efficiently regulate 12 V down to 3.3 V, 1.8 V, or whatever other voltages the card requires. The switching regulator topology selected may add to the bulk capacitance required in the module and may also demand specific voltage ramp rates or enabling sequences for proper operation.

Of the various options for InfiniBand bulk power management, one solution that takes into consideration all of the hurdles and requirements mentioned uses an HSPM, such as TPS2330, and a power supply controller, such as TPS5102 (see Figure 1). With minimum external circuitry other than discretes, a truly effective solution is possible. The TPS2330 HSPM is designed to manage voltage rails with a nominal value from 2.7 V to 13.5 V. Its gate pins implement a voltage ramp drive topology, which provides a very graceful turn-on for the external FETs. It also has an integrated adjustable circuit breaker and a Power Good reporting function for system status updates. The TPS5102 is a high-efficiency, dual-output power controller. Its topology requires minimal input and output capacitance, and its operating frequency reduces the size requirements of other external components. It has several system control features that benefit InfiniBand, such as independent standby and soft-start configurations.

Related Web sites

www.ti.com/sc/docs/products/analog/tps2330.html
www.ti.com/sc/docs/products/analog/tps5102.html

Comparing magnetic and piezoelectric transformer approaches in CCFL applications

By Eddy Wells

Power Management Products Systems Specialist

Cold cathode fluorescent lamps (CCFLs) are commonly used as a backlight source for color liquid crystal displays (LCDs) used in notebook computers and portable electronic devices. These lamps require a high ac voltage for ignition and operation. The required ignition voltage is typically double the operating voltage and increases at cold temperatures. Figure 1 shows the operating voltage of lamps with 3-mm diameters and various lengths (100 mm, 150 mm, and 250 mm). Lamp voltage is primarily dependent on length and is fairly constant with current, giving a nonlinear characteristic. Lamp current is roughly proportional to brightness or intensity and is the controlled element of the backlight supply. The lamp requires a sinusoidal voltage to provide the best electrical-to-optical energy conversion.

The lamp and display enclosures used for next-generation portable products are becoming increasingly narrow, generating the need for a low-profile CCFL power supply. Advances in both magnetic and ceramic piezoelectric transformers (PZTs) have enabled efficient and smaller backlight converters to be built. The choice of transformer depends on several factors including cost, size, and efficiency. For example, a magnetic transformer may be thicker, heavier, and less efficient than a PZT at a particular power level; but it has the advantages of lower cost and the ability to function over a wider range of load conditions. The PZT transformer has the advantages of inherently sinusoidal operation, high strike voltage (which can be used with non-mercury lamps), nonflammability, and no electromagnetic noise. Some examples of transformers used in 3- to 4-W notebook computer applications are shown in Figure 2.

Figure 1. Typical voltage and current behavior in a CCFL

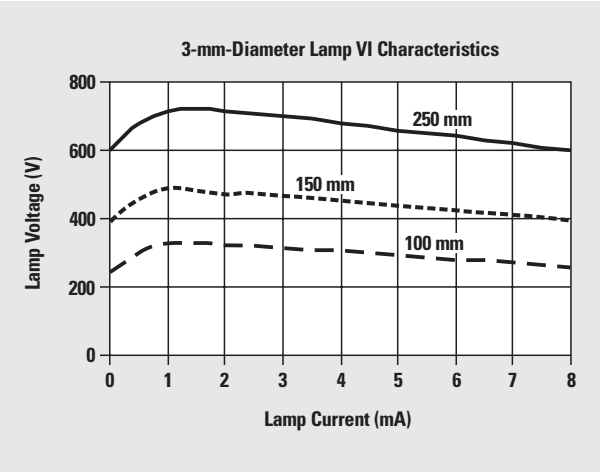
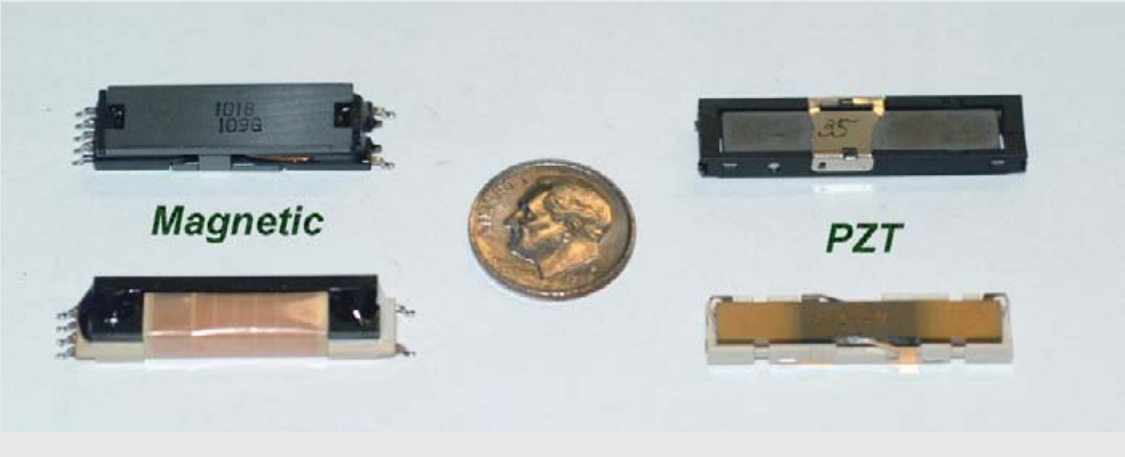


Figure 2. Size comparisons of magnetic and PZT transformers



A quick review of magnetic transformer operation

A high-frequency magnetic transformer consists of multiple wires wrapped around a common ferrite core, as shown in Figure 3. Energy transfer occurs in the core between flux and magnetic fields. This energy transfer can also be equated to volt-seconds and current:

$$\text{Energy} = \int I \times V dt = \int_{\text{volume}} H \times dB.$$

Flux density (B) is proportional to volt-seconds and inversely proportional to the cross-sectional area of the core and number of turns, according to Faraday's law:

$$B \approx \frac{V}{N \times A_{core} \times \text{Frequency}}.$$

Magnetic field (H) is proportional to amp turns and inversely proportional to path length, as described by Ampere's law:

$$H \approx \frac{N \times I}{L_{path}}.$$

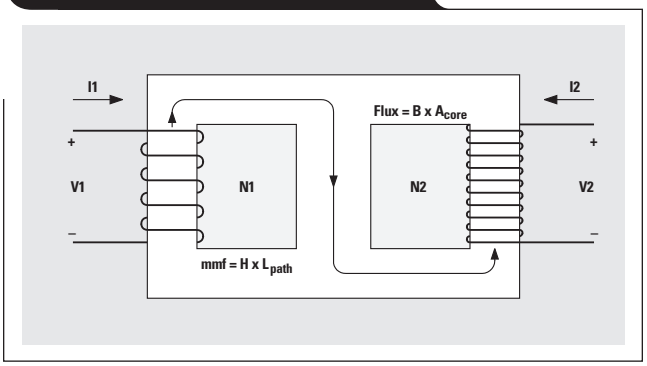
The relationship between the flux and magnetic fields is determined by the permeability of the core:

$$\mu = B/H.$$

The voltage gain of the transformer can be easily adjusted by the ratio of secondary to primary turns, N2/N1, where the current gain in the transformer is related by N1/N2.

When a transformer for a CCFL circuit is designed, the number of primary turns is determined by the required inductance of a resonant tank developed between the transformer's primary and an external capacitor. The number of secondary turns should provide sufficient ignition voltage for the lamp. The high number of secondary turns typically requires a large window area in the core. Leakage inductance in CCFL transformers is large due to the high-voltage spacing requirements between primary and secondary. This leakage inductance reduces the effective turns ratio but does not produce transient switching spikes in the application, as the transformer is operated with sinusoidal waveforms. Other issues with magnetic transformers include stray magnetic fields that may require shielding and the potential of electrical arcing if the secondary voltage is not controlled in a fault situation.

Figure 3. Magnetic transformer



Piezoelectric transformer operation

Unlike magnetic transformers that rely on electromagnetic energy transfer, piezoelectric transformers exchange electric potential with mechanical force. A typical multi-layer PZT with "longitudinal-mode" geometry is shown in Figure 4. An ac voltage is applied to the V_{IN} electrodes, causing mechanical expansion and compression in the thickness direction. This displacement on the primary is transferred as a force in the longitudinal or length direction. Supports at ¼ and ¾ wavelength provide a means for a standing wave to be generated at a resonant frequency, as shown.

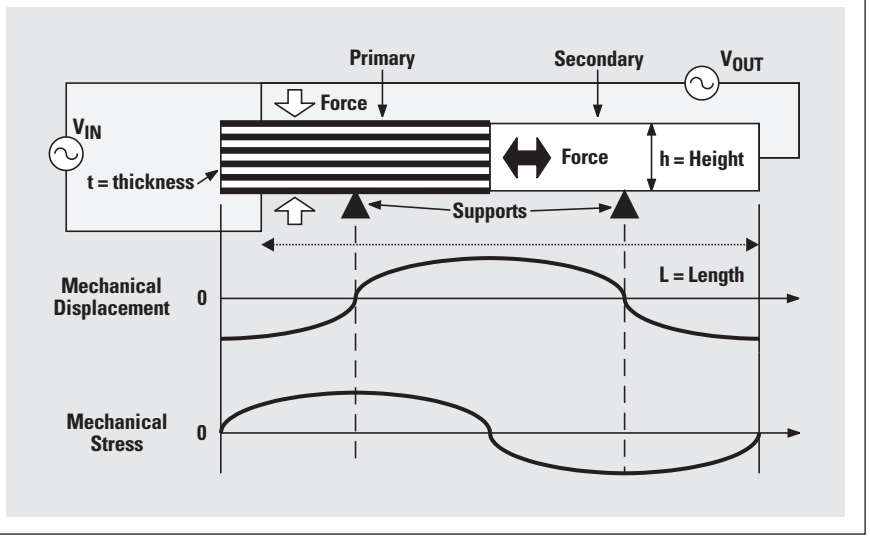
Mechanical resonance occurs at multiple standing-wave frequencies (n) based on the transformer's length and material velocity (V):

$$f_n = n\frac{\upsilon}{2 \times \text{Length}}.$$

Voltage gain is a function of the PZT material coefficient g(ω), the number of primary layers, the thickness of the material, and the overall length as follows:

$$V(\text{gain}) = \frac{\text{Length} \times \text{Layers}}{\text{Thickness}} \times g(\omega).$$

Figure 4. Typical longitudinal-mode piezoelectric transformer for CCFL applications



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An electrode at V_{OUT} is used to recover the amplified electrical potential at the secondary. To predict PZT performance in a system, it is useful to develop an electrical circuit model. The model shown in Figure 5 is often used to describe the behavior of a PZT near a single resonant frequency. Many PZT manufacturers will provide component values for the model based on measurements taken at various frequencies and output loads.

A large primary capacitance (C_{input}) is formed as a result of the multi-layer construction of the primary electrodes and material dielectric constant. The output capacitance is much smaller due to the distance between the primary and secondary electrodes. The mechanical resonant frequency (ω_0) of the PZT is proportional to the material elasticity (Y), density (ρ), and length:

$$\omega_0 \propto \frac{1}{\text{Length}}\sqrt{\frac{Y}{\rho}}.$$

The mechanical piezoelectric gain near a single resonant frequency can be modeled by a series R, L, and C circuit in the electrical equivalent model of Figure 5; whereas Figure 6 illustrates the gain versus output load and frequency characteristics for a PZT with the following values:

C_{input} = 0.2 µF, C_{OUT} = 30 pF, n = 30,
Series RLC (2 Ω, 1 mH, 6 nF).

As shown in Figure 6, the ceramic transformer provides high Q and gain under light or no-load conditions, producing a high strike potential. Once the lamp strikes, the transformer becomes loaded, causing the transformer gain to decrease and resonant frequency to shift. Because of the unique gain characteristics of the PZT transformer with load, no ballasting element is required between the transformer secondary and the lamp as with the magnetic transformer.

Operating a magnetic transformer with a current-fed, push-pull topology

A current-fed, push-pull topology is commonly used to power a magnetic transformer-based CCFL circuit, as shown in Figure 7. This topology accommodates a wide input voltage and dimming range while retaining sinusoidal operation of the lamp. The converter consists of a resonant push-pull stage, a PWM buck-derived control stage, and a high-voltage secondary stage.

The push-pull stage consists of transistors Q2 and Q3, which drive the center-tapped transformer T1. The transistors are driven 180° out of phase at 50% duty cycle with an auxiliary winding on the transformer. A resonant tank is formed between the primary inductance of T1 and a low-loss, external resonant capacitor (C4). The resonant tank provides a sinusoidal voltage to the transformer's primary and sets the operating frequency of the system.

Figure 5. Equivalent piezoelectric transformer circuit model

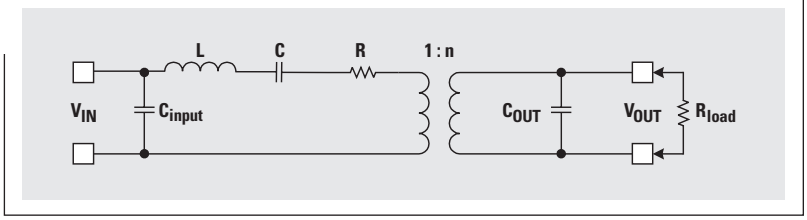


Figure 6. Typical piezoelectric gain characteristics vs. frequency and load

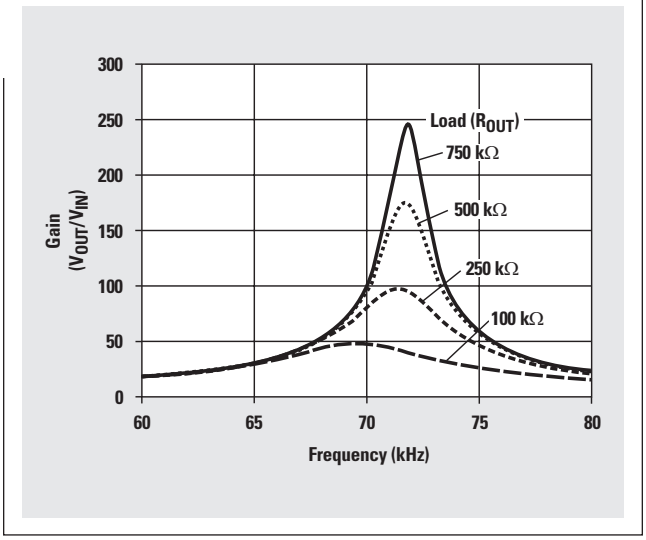
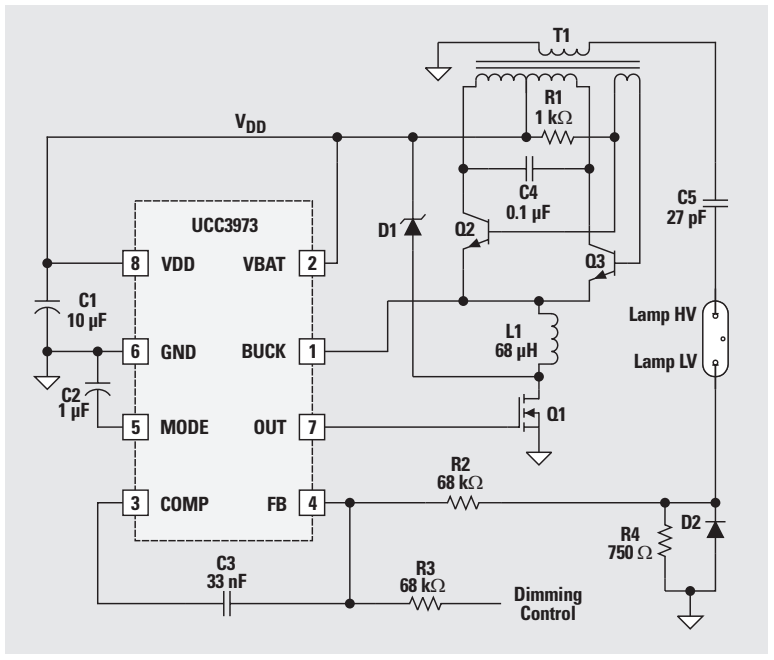


Figure 7. UCC3973-based CCFL power supply using a resonant half-bridge topology



The primary resonant tank is fed with a dc current from the buck stage consisting of Q1, D1, and L1. The UCC3973 synchronizes the buck frequency to the push-pull stage to prevent a beat frequency from occurring. The dc current in L1 is controlled by the duty cycle of Q1. The buck stage duty cycle is determined by the feedback network (at FB and COMP), which is used to regulate lamp current (sensed across R4).

The high voltage at the secondary of T1 is used to ignite and operate the lamp. Since the ignition or strike voltage is higher than the operating voltage, a high voltage capacitor (C5) is required to allow a voltage difference between the transformer secondary and lamp. This capacitor is also used as a ballasting element for the circuit to deal with the nonlinear nature of the lamp as it is dimmed. The transformer secondary can be designed with a high leakage inductance, allowing the ballast capacitor to be eliminated.

Waveforms for the buck, push-pull, and lamp circuits are shown in Figures 8 and 9. The square wave in Figure 8 is the common node of the buck stage where D1, Q1, and L1 connect. The rectified sinusoid of the push-pull resonant tank (Figures 8 and 9, top trace) is measured where L1 and the emitters of Q2 and Q3 connect. Lamp voltage is shown in Figure 9. The sinusoidal shape of the waveform provides good electrical-to-optical efficiency. Finally, Figure 10 shows system efficiency performance from V_{IN} to V_{lamp} over a wide range of input voltage and lamp current.

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Figure 8. Buck and push-pull waveforms

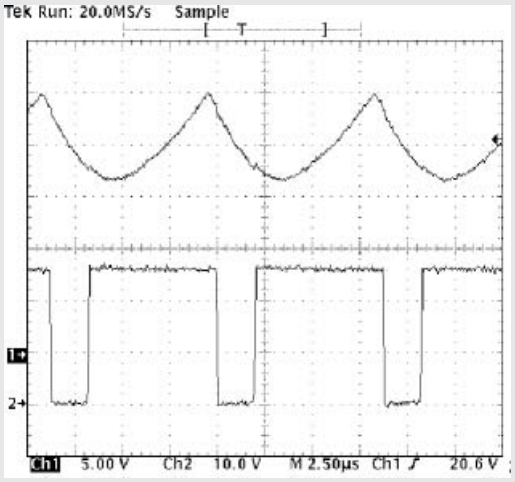


Figure 9. Push-pull and lamp waveforms

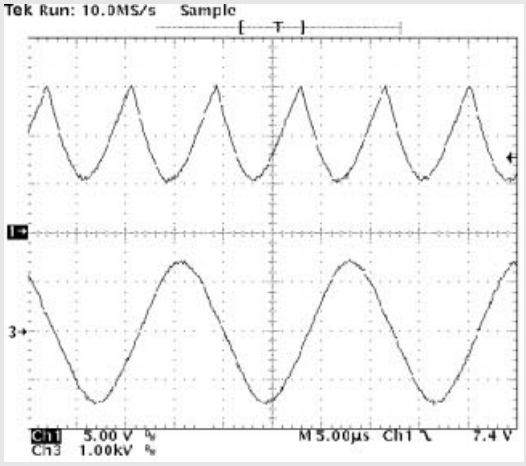
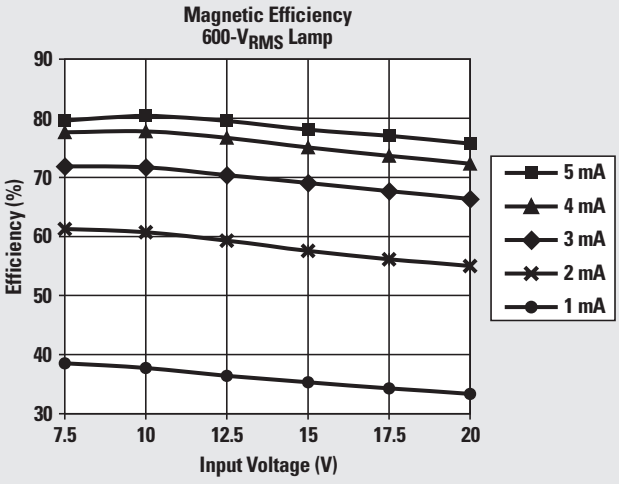


Figure 10. Electrical efficiency for magnetic-based backlight



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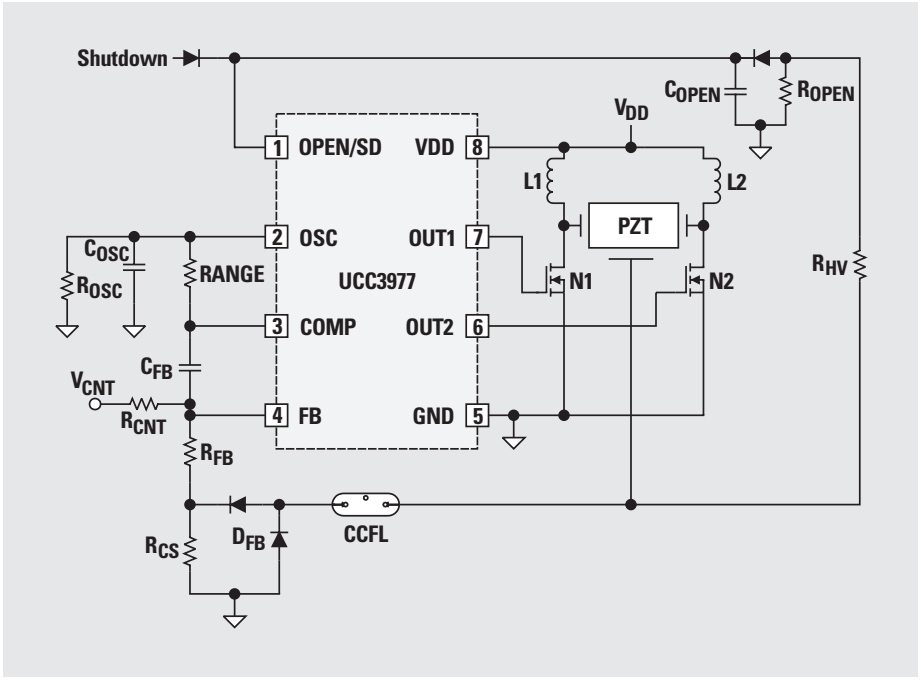
Operating a PZT with a voltage-fed, push-pull topology

A circuit used to control a piezoelectric transformer in a resonant push-pull topology is shown in Figure 11. This topology uses two standard inductors (L1 and L2) that are driven 180° out of phase at 50% duty cycle with the UCC3977 controller and MOSFETs N1 and N2. The push-pull circuit has the advantage of providing voltage gain from the dc input voltage to the piezoelectric transformer primary. Resonant operation is achieved with the LC relationship between the inductors and primary capacitance of the PZT.

Unlike the magnetic transformer circuit previously discussed, the PZT-based circuit uses frequency rather than duty cycle to control lamp current. The UCC3977 contains a programmable voltage-controlled oscillator (VCO) formed at the COMP and OSC pins. The VCO is used to set the system's operational frequency range, which must include the strike and operating frequencies of the PZT. Lamp current, sensed at the FB pin, is controlled by the gain-to-frequency characteristics of the PZT (see Figure 6). The gain of the PZT must provide sufficient lamp voltage at minimum input voltage to ensure that the control loop will always operate on the right side of resonance.

Figure 11. UCC3977-based CCFL power supply using a resonant push-pull topology



Operating waveforms for the push-pull circuit are shown in Figure 12. MOSFETs N1 and N2 are driven out of phase at 50% duty cycle (see Figure 12, trace 2). Inductors L1 and L2 resonate with the PZT primary capacitance, forming half sinusoids at the drain of N1 (trace 1) and S2 (trace 4). The resulting voltage across the PZT primary is a near sinusoid (trace M1). The lamp voltage, which is approximately 600 V in this application, is sinusoidal (trace 3) due to the high Q of the ceramic transformer.

To achieve zero-voltage switching, the drain voltage must return to zero before the next switching cycle. This dictates that the LC resonant frequency be greater than the switching frequency. The maximum inductance to meet these conditions can be found from:

$$L < \frac{1}{4 \times \pi^2 \times f^2 \times Cp}.$$

Figure 12. UCC3977 push-pull waveforms with V_{IN} 7-Vdc and 600-V lamp

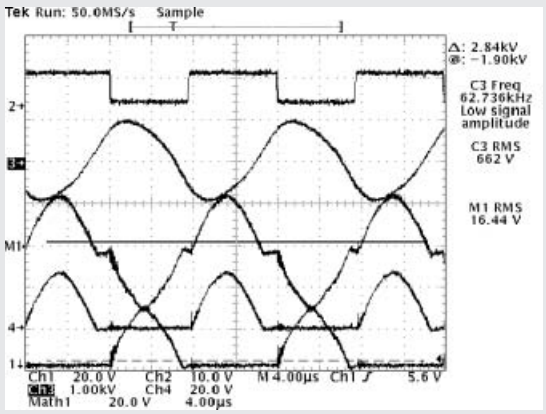


Figure 13 shows the efficiency performance of a 3-W-rated, multi-layer PZT configured with push-pull topology when operating a 600-V lamp. Electrical efficiency is greater than 85% at lower input voltages, decreasing at higher input voltages as the PZT gain is reduced.

Figure 14 shows plots of PZT operating frequency over the same lamp conditions as those shown in Figure 13. As expected, frequency decreases at higher lamp currents as the PZT characteristics shift to a lower operating frequency when loaded (see Figure 6). Frequency increases linearly with input voltage, since the required V_{OUT}/V_{IN} gain to operate the lamp is decreased.

Using a burst dimming technique

Dimming by linearly reducing lamp current causes the efficiency to degrade for both magnetic and PZT transformers. Light load efficiency decreases in the magnetic transformer circuit due to the circulating currents in the resonant tank, which are a constant loss regardless of lamp current. Efficiency degrades in the PZT circuit at light load because the system is operated at less than optimal gain. Efficiency can be improved with either circuit by using a burst dimming technique. This method involves running the lamp at full current and controlling the average lamp current by modulating the on/off duty cycle at a frequency higher than the eye can detect (>100 Hz).

Figure 15 shows burst-dimming waveforms of the PZT-based backlight circuit. Burst-dimming waveforms for the magnetic-transformer-based circuit would be similar. An external drive signal (trace 2) is used to command the duty cycle and frequency of the burst (125 Hz at 50% duty cycle in this case). Trace 1 is the gate of one of the MOSFETs; whereas trace 3 shows the COMP pin of the feedback network used to set the operating frequency. Lamp voltage is shown on trace 4. These pictures were taken with a digital oscilloscope, so aliasing is present. Strike voltage for the lamp is barely detectible, since the lamp is warm and operating from the previous burst cycles.

Summary

Characteristics of cold cathode fluorescent lamps used as backlight sources for portable applications have been presented. The operating principles of two transformer types (magnetic and piezoelectric) that address the high voltage requirements of these lamps have been discussed. The choice of transformer for a particular application depends on several factors including efficiency, size, and cost. Resonant power circuits that provide sinusoidal operation to increase optical efficiency were presented for both transformer types. Lamp brightness can be controlled by either a linear or burst dimming technique. Efficiency of greater than 80% can be achieved with either transformer type, increasing the run time of a battery-powered system.

Related Web sites

www.ti.com/sc/docs/products/analog/ucc3973.html
www.ti.com/sc/docs/products/analog/ucc3977.html

Figure 13. Typical PZT efficiency with input voltage and loading

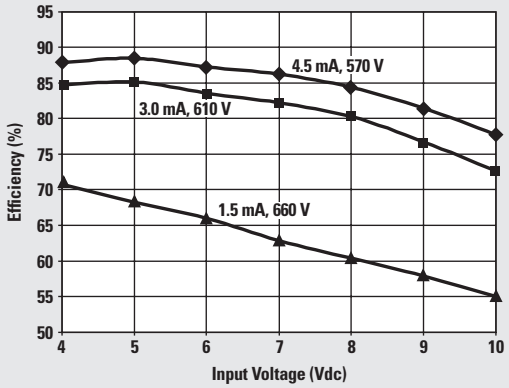


Figure 14. PZT operating frequency vs. input voltage and lamp load

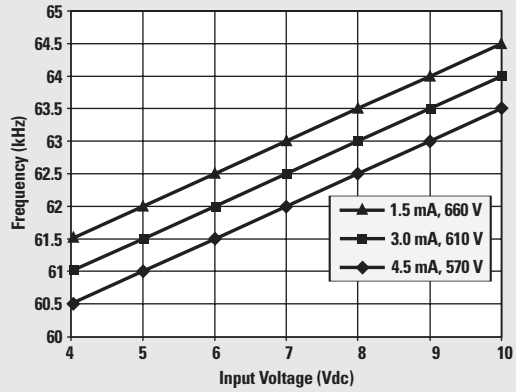
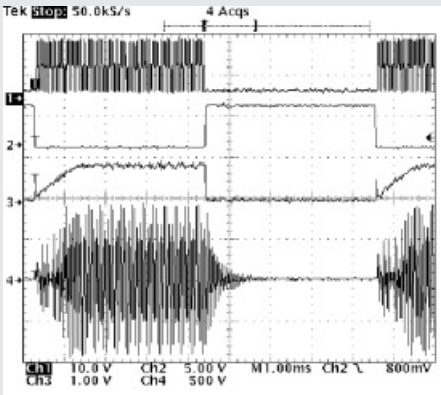


Figure 15. Burst dimming for a PZT-based backlight circuit



Why use a wall adapter for ac input power?

By Robert Kollman, *Senior Applications Manager, Power Management,*
and John Betten, *Applications Engineer, Member Group Technical Staff*

Introduction

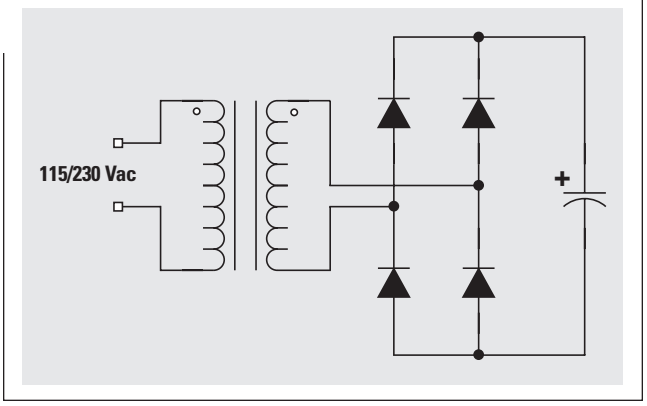
A DSL modem was chosen to examine the tradeoffs of using a wall adapter versus using an offline power supply. DSL modems are being widely deployed, with the number of new subscribers expected to grow at greater than a 50% compounded annual rate over the next four years. The number of new subscribers is expected to grow from 7 million this year to over 25 million in 2004. Because the DSL modem is a consumer product, cost is a very sensitive issue in its design; this cost ripples down into the power supply architecture selection. Designers are faced with two popular choices. In the first, a 50/60-Hz transformer, rectifier, and filter generate a low dc voltage that is then converted to well regulated outputs. In the second, ac input power is rectified and filtered, and a high-frequency switcher converts the resulting high-voltage dc to regulated voltages for the DSL electronics. While the second approach is generally cheaper in high-volume applications, it significantly complicates the modem design. The power supply is typically implemented on the same circuit card as the remainder of the electronics, and the high dc voltage introduces issues of agency approvals, noise, and size.

Table 1 presents typical VoIP DSL modem power supply requirements. Modems are generally required to run from ac wall power that has a wide voltage and frequency range. As with many modern systems, a number of low voltages power various analog and digital functions. In addition, two higher negative voltages power a telephony interface. The –24-V output provides power for the loop current while the telephone is in use. A –72-V output powers the phone ringing circuitry. As contrasted with the lower voltages, these outputs have widely varying load ranges, from essentially no load when the phone system is not in use, to full load on either output depending on whether the line is in use or simply ringing. Efficiency is generally not a critical issue as long as the heat can be removed; consequently, low-cost linear regulators are widely used.

Table 1. Typical VoIP DSL modem power supply requirements

PARAMETER	REQUIREMENTS			
Input voltage(s)	115/230 Vac, 50/60 Hz			
Output power	9.7 W max			
Output parameters	**Voltage (V)**	**Max Current (A)**	**Max Ripple (mV_{pp})**	**Regulation (%)**
	+5	0.65	50	±5
	+3.3	0.75	30	±3
	+1.8	0.40	30	±3
	+1.5	0.40	30	±3
	–28	0.05	500	±15
	–72	0.02	1000	±15
Efficiency	Very system-dependent from 50 to 85%			

Figure 1. A simple ac-to-dc unregulated wall adapter



What is an ac/dc wall adapter?

A wall adapter's function is to step down the raw 115/230-Vac line voltage into a safer, lower-voltage dc output that can be readily accepted by either the end use equipment or another power supply input. The output voltage tolerance over which the equipment being powered can operate determines whether additional voltage regulation is required. Some circuits, such as battery chargers, may not require a tightly regulated input voltage, and an unregulated dc input voltage may work just fine. In this case, the simplest way to generate that voltage is shown in Figure 1.

This circuit generates one output voltage; but multiple well regulated outputs are often needed. The most common ways to generate these voltages are with switching regulators, linear regulators, or a combination of both. If the unregulated input voltage is higher than the output voltages, multiple buck converters and/or linear regulators are often the best solution. Linear regulators would be used if the output current is not large so that excessive power is not dissipated in the device. In the case where only a single regulated output is needed, the switching converter can be placed either inside the ac/dc wall adapter, making this the entire power supply, or added as part of the end-use circuit. Depending on the goals of the overall product, either choice may be used. For example, if a smaller or lighter product is desired, then a regulated wall adapter would be used. If aesthetics, integration, or heavy loading are important goals, then putting the switcher with the end-use circuit would be the best solution.

Figure 2 shows the output voltage variation with an unregulated wall adapter. When loaded lightly, the output voltage is at its maximum because the output capacitor peak detects the transformer secondary. The capacitor stays fully charged during the entire line period due to low current draw. As the load is increased, the dc output voltage starts to droop. A large amount of primary winding resistance and leakage inductance is designed into the transformer to limit energy in a fault condition. A large portion of the leakage inductance is due to the separation between the primary and secondary windings required for UL approval. This can be in the form of either a split bobbin with the primary and secondary windings on opposite halves of the core or a large amount of insulating tape between the layer stacks. With increasing load current, a larger share of the transformer's voltage drops across the winding resistance and leakage inductance, reducing the output voltage. Since the output diodes only conduct when the secondary voltage on the transformer exceeds the voltage on the output capacitor, the output capacitor provides the load current during a large portion of the line period. The larger the load becomes, the more voltage droop there will be across the output capacitor, since it must support the load entirely. Eventually, as the load is increased beyond its design limits, the output diodes and/or the transformer windings will overheat and fail as open circuits, reducing the output to zero volts. This failure does not usually happen instantly; and, as Figure 3 shows, peak output powers of approximately 150% of maximum power can be obtained for a duration of several seconds. However, this peak power occurs at voltages significantly lower than nominal.

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Figure 2. A 9-V/1.2-A ac/dc unregulated wall adapter output voltage

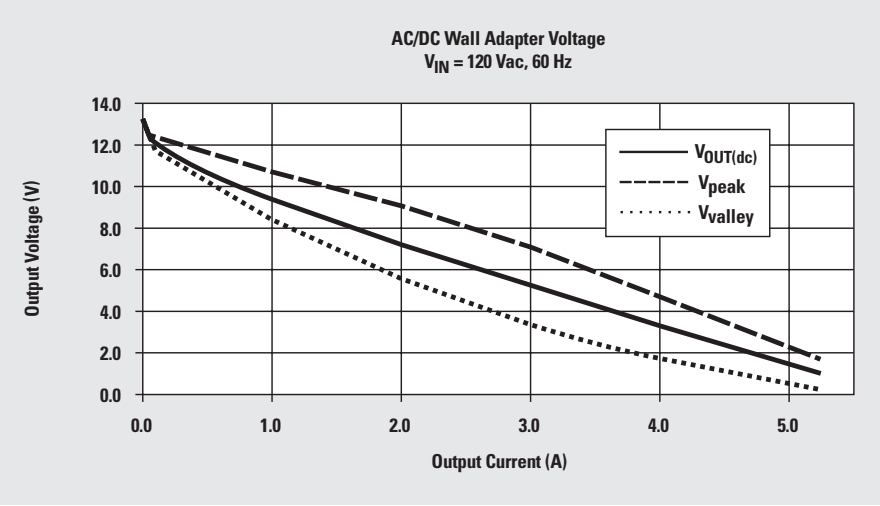
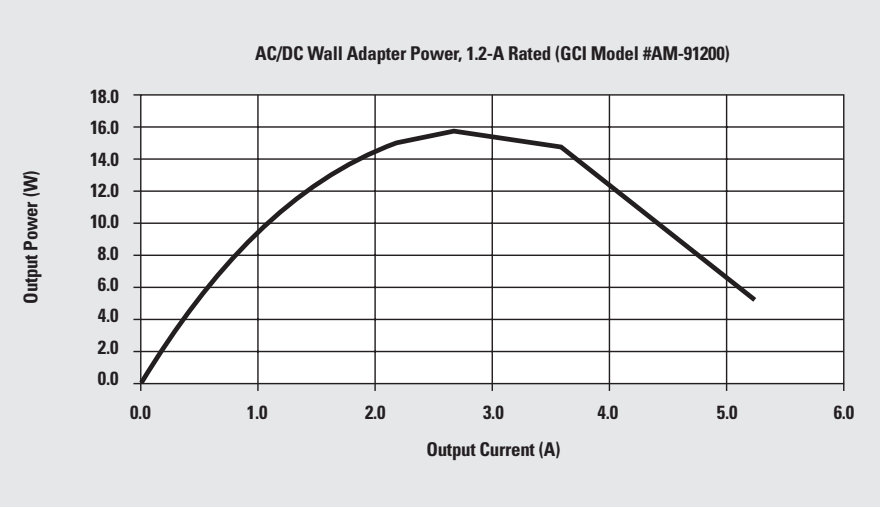


Figure 3. 50% additional peak power is available for short durations



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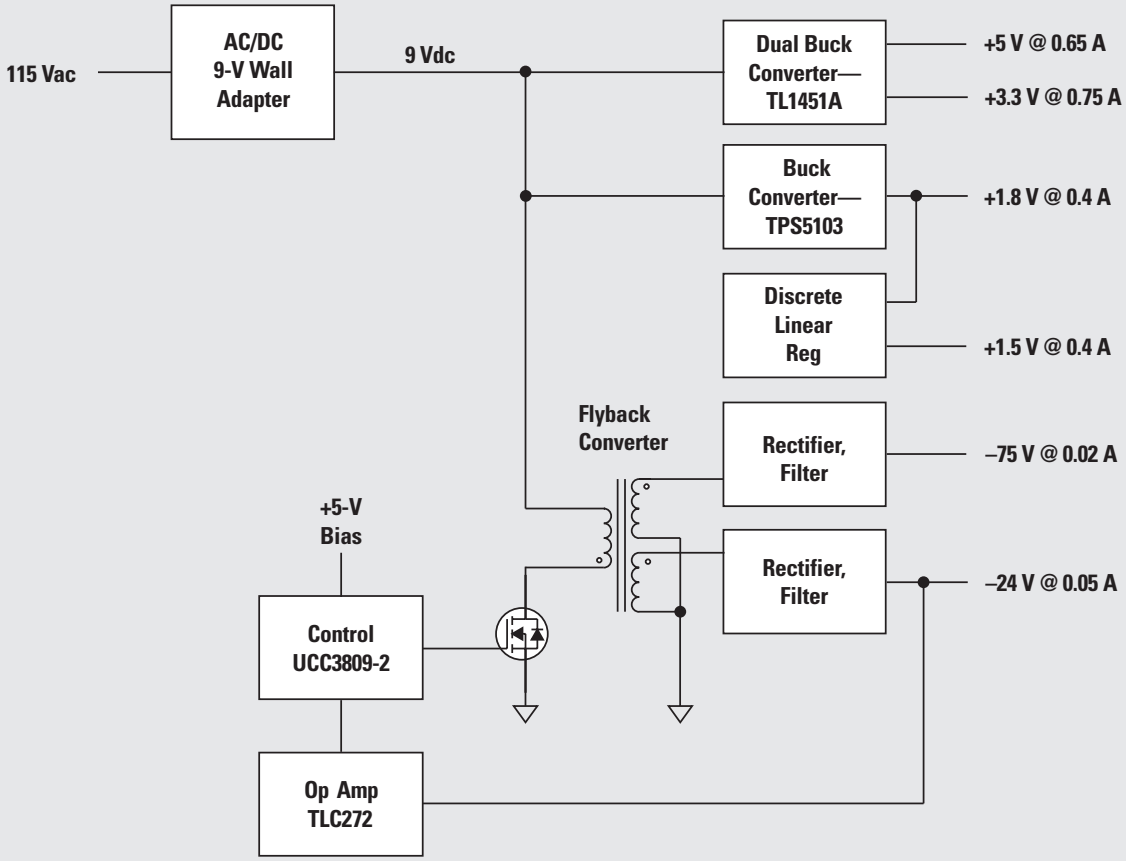
What's the wall adapter approach?

Figure 4 shows a sample design of a DSL modem powered by a wall adapter. A wall adapter converts wall power to an unregulated 9 Vdc. With load ranges from 0 to 100% and input voltage tolerances of greater than ±10%, the 9-V output can have a variation of over 6 to 15 V. Since the wall adapter is outside the modem and isolated, the 9-V input to the product does not represent a safety issue and can be simply routed within the modem. The 9-V input then drives multiple power stages to provide the user voltages. Buck converters and linear regulators generate the lower voltages for the digital and analog circuits, while a flyback power supply feeds the telephony interface circuits.

What's the offline approach?

Figure 5 represents the block diagram of an offline switcher for powering the DSL modem. The 115 Vac is rectified and filtered to provide an unregulated dc voltage of 240 Vdc to nearly 400 Vdc. This high voltage is switched by the flyback converter primary FET and rectified into dc on the secondary side. The main regulated output voltage is sensed and feedback to the primary side is used to maintain regulation over input line and output load variations. The telephony output voltages are unregulated and will vary some with line/load, while the lower voltage secondaries use linear regulators. The power transformer and the feedback optocoupler provide the required isolation between the primary input and secondary outputs. Care must be taken in the design of the power transformer to assure that proper spacing is maintained between primary and secondary windings to prevent arcing. Interwinding capacitances, improper grounding, and poor layouts can allow differential and common-mode currents to flow in the primary and/or secondaries and create noise voltages on the outputs as well as put EMI back into the source voltage. The input filter must be designed to suppress these currents to meet agency approvals. The designer must also be careful to use the proper voltage clearances between the optocoupler leads and between the transformer primary and secondary leads on the PWB itself, as well as between adjacent layers. The high voltage and isolation requirements present on the offline converter make the design somewhat more complicated than the wall adapter power supply.

Figure 4. Wall adapter power supply block diagram



So which approach should you use?

Figure 6 shows the two approaches in approximately the same scale, and many of the differences are very apparent. The wall adapter is large since it must operate at line frequency; however, it is generally located outside the product and will not impact the product size. The adapter is very aesthetically unpleasing, as it can take up more than one slot on a power strip or hang from a wall plug. However, as you look further downstream, it becomes clear why so many products use the adapter. The wiring from it to the product is simpler due to lack of safety issues. The power supply in the product is simpler since it does not need to provide safety isolation or significant EMI filtering. As shown in the power supply in Figure 6b, EMI filter components and clearances can represent a third of the offline switcher board area. In addition, the offline power supply is another 20–30% larger since it has a transformer on board.

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Figure 5. Offline power supply block diagram

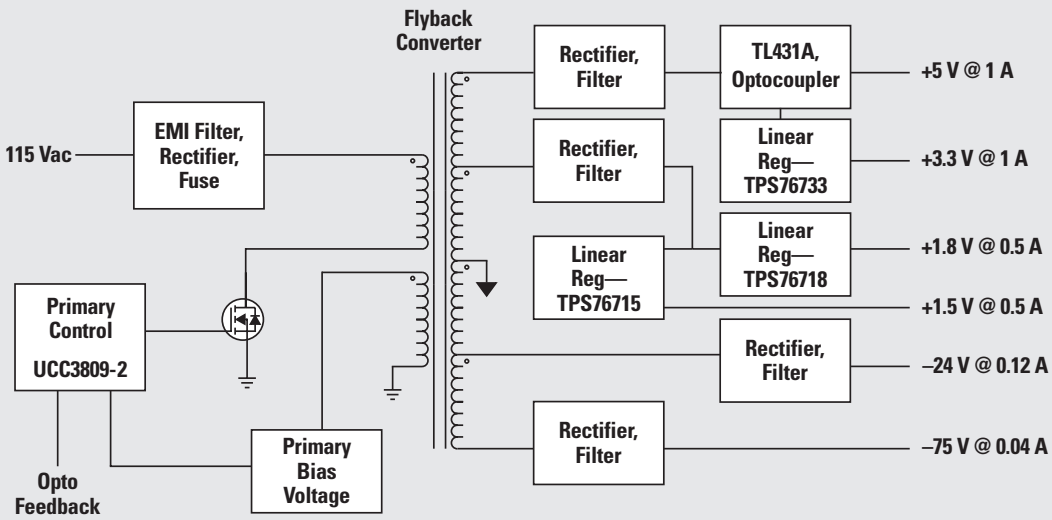
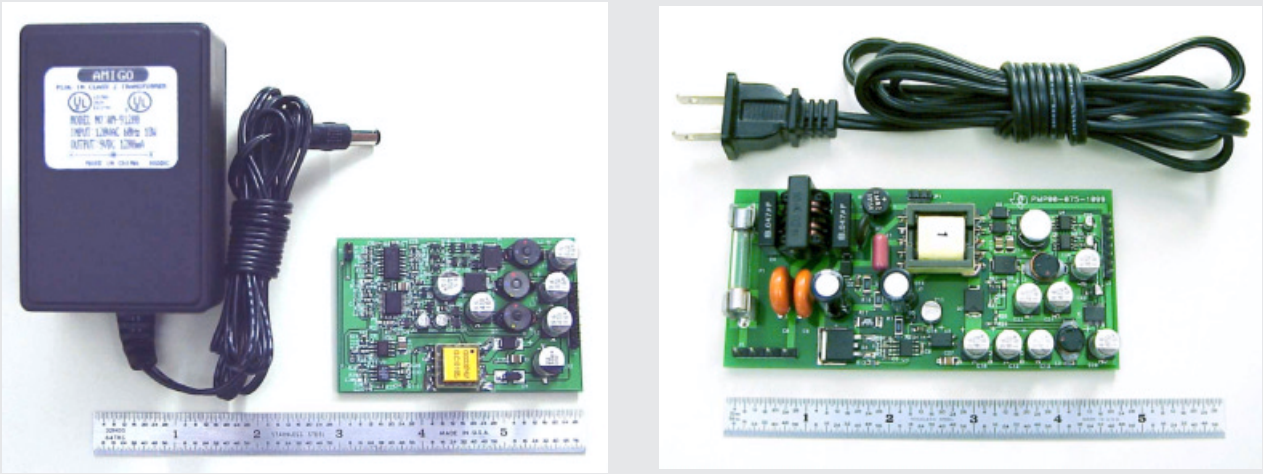


Figure 6. Wall adapter approach (a) requires significantly less PWB area



(a) (b)

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Table 2 presents a comparison of the two approaches. The first comparison is physical size. As shown in Figure 6, the wall adapter approach results in the smallest modem size, with an advantage of at least 4 in^2. The size of the design could be further reduced with the substitution of linear regulators for the buck power supplies. Component height favors the wall adapter approach also, as the input EMI filter components and power transformer of the offline approach drive its height 0.2 inches taller. Overall power supply weight favors the offline approach with its high-frequency transformer versus the very heavy line frequency transformer of the wall adapter approach.

Table 2 also includes relative costs of the two approaches. It includes product cost as well as engineering development time. In the very high-volume applications, where development cost does not represent a significant portion of the total cost, the offline approach has a slight cost advantage. Additionally, the offline inventory costs will be lower because a $0.25 line cord will be needed rather than a $2.00 wall adapter. However, in the lower-volume applications, the wall adapter has an advantage because it represents a simpler design with much lower qualification costs. Amortizing agency approvals over small production runs increases the costs of the offline approach. UL will take a much closer look at products with high voltage in them versus those where the high voltage is isolated within an approved wall adapter. The additional safety concerns will lengthen the time to market, necessitating additional time to make sure the design is correct before it is qualified. The DSL modems are also sensitive to power supply noise. The offline approach will switch 400 V on the primary that will have a higher likelihood of generating noise problems. All these factors raise the schedule risk of the offline approach, as the layout of the PWB will be more critical. Consequently, the offline approach will take a little more debug time.

So when is a wall adapter an appropriate choice? It is when production volumes are low, or when getting the product out quickly is key. It is typically not when production volumes are going to be high.

Table 2. Offline approach is cheaper but carries higher risk

	AC/DC POWER SUPPLY	WALL ADAPTER AND DC/DC POWER SUPPLY
PWB area (in^2)	10	6
Component height (in)	0.5	0.3
Weight (lbs)	0.4	1.6
Aesthetics	Integrated in product	Big ugly tacky transformer
Relative cost (10K units)	2.5	2.0
Relative cost (1M units)	1.0	1.1
UL	HV in product	Simpler approval
Relative time to market	Additional 2–4 weeks	Baseline
Relative risk	Highest	Lowest

For further information, contact:

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Power consumption of LVPECL and LVDS

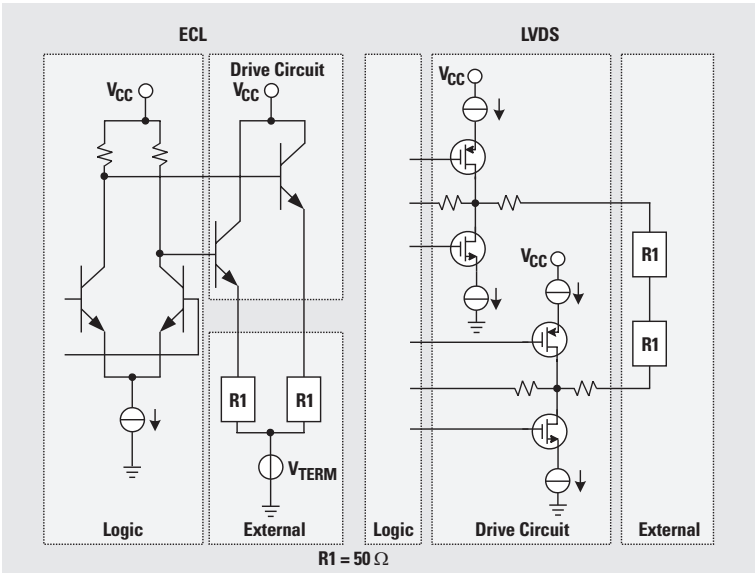
By Chris Sterzik
Applications Specialist, Interface Products

Introduction

Single-ended emitter-coupled logic (ECL) has been in existence for over 30 years and is a proven high-speed technology. More recently, differential ECL has been introduced along with the variants of positive ECL (PECL) and low-voltage PECL (LVPECL). The common feature of all these devices is high signaling rates. ECL and its variants use bipolar technology to obtain these high data rates. The major benefit of bipolar technology is the relatively constant consumption of power over frequency, while a major cost of bipolar technology is the required termination.

Even more recent than the introduction of differential ECL is the TIA/EIA-644 introduction of LVDS. While the standard does not specify a technology, CMOS and BiCMOS are common implementations. CMOS technology is often generalized as being low-power and low-speed. While it is true that the power consumption of CMOS devices increases linearly with speed,[1-2] new technologies using LinBiCMOS, such as the Texas Instruments LVDS product line, provide the benefits of both high speed and low power consumption.

Figure 1. Models of ECL and LVDS output drivers and terminations



Power definition

Power, in the context of this document, is broken down into categories of external, drive circuit, and logic power, as shown in Figure 1. The external power consumption is simply the power consumed in the external termination. The drive circuit power is dissipated within the device and is a function of the output currents and the voltage drop across the driver circuit. The logic power is best described as the switch and bias power required by the IC.

The following discussion presents a theoretical approach to calculating the quiescent power dissipation for each of the categories. The devices being compared are LVPECL 1 to 10, LVDS 1 to 8 (SN65LVDS108), and LVDS 1 to 16 (SN65LVDS116) channel repeaters. Table 1 shows the values provided in the data sheets for the LVPECL and LVDS devices.

Logic power dissipation

The logic power dissipation includes quiescent and active power. The bipolar device consumes a significant amount of quiescent power but almost no active power; that is to say, the power consumption is expected to be constant over frequency. In contrast, the BiCMOS device consumes very little quiescent power, but more power is consumed as the frequency increases. Since no real insight is given about the bias structures or the switching nodes for either device, the 250 and 330 mW calculated from the LVPECL device parameters represents the quiescent logic power dissipation. This assumption is made because only I_{EE} is provided in the LVPECL parameters and not I_{CC}. The LVDS logic power is calculated by subtracting the drive circuit and external power from the total quiescent power dissipation of 205 mW and 264 mW in Table 1.

Continued on next page

Table 1. Data sheet power consumption

	LVPECL	LVPECL	SN65LVDS108	SN65LVDS116
V_{CC}	2.5 V	3.3 V	3.3 V	3.3 V
V_{EE}	GND	GND	NA*	NA*
I_{EE} (typical)	100 mA	100 mA	NA*	NA*
I_{CC} (typical)	Not given**	Not given**	62 mA	80 mA
Power	250 mW	330 mW	204.6 mW	264 mW

*NA = Not applicable. V_{EE} and I_{EE} are defined only on the LVPECL data sheet.
**I_{CC} is not provided in the LVPECL data sheet.

Continued from previous page

Drive circuit dissipation

The drive circuit power consumption does not include power dissipated in the line or the termination. The active components of the circuit driver are also difficult to calculate from the data sheet. However, by using Figure 1 and Equations 1 and 2 (pp. 49 and 51 in Reference 2), the amount of quiescent power consumed in the output structures for both the LVDS and LVPECL repeaters can be calculated. Table 2 lists the output specifications and the calculated drive circuit dissipation.

External power dissipation

The external power consumption is assumed to have no active component, and any capacitive effects are negligible. The power loss through the media to the load is also considered to be negligible. Therefore, the only source of power dissipation is in the load and termination voltage. Table 3 shows the external power consumption obtained from Equations 3 and 4.

Table 2. Theoretical quiescent power consumption of driver circuit

	LVPECL 1:10	LVPECL 1:10	SN65LVDS108	SN65LVDS116
V_{CC}	2.5 V	3.3 V	3.3 V	3.3 V
R1	50 Ω	50 Ω	50 Ω	50 Ω
V_{OH} (typical)	1.48 V	2.28 V	1.41 V	1.41 V
V_{OL} (typical)	0.68 V	1.48 V	1.09 V	1.09 V
V_{TERM} (V_{CC}–2 V)	0 V*	1.3 V*	NA**	NA**
Power/channel	54.9 mW	26.5 mW	9.55 mW	9.55 mW
Number of channels	10	10	8	16
Total power	549 mW	265 mW	76.4 mW	152.8 mW

* V_{TERM} is the recommended data sheet value.
** NA = Not applicable. No termination voltage is required for LVDS.

Table 3. Calculated external power consumption

	LVPECL 1:10	LVPECL 1:10	SN65LVDS108	SN65LVDS116
V_{CC}	2.5 V	3.3 V	3.3 V	3.3 V
Power/channel	53.1 mW	50.0 mW	1.156 mW	1.156 mW
Number of channels	10	10	8	16
Total power	531 mW	500 mW	9.25 mW	18.5 mW

$$P_{ECL} = \frac{(V_{CC} - V_{OH})(V_{OH} - V_{TERM}) + (V_{CC} - V_{OL})(V_{OL} - V_{TERM})}{R1} \quad \textbf{(1)}$$

$$P_{LVDS} = R_B \times I^2 + R_A \times I^2 \quad \textbf{(2)}$$

$$I = \frac{(V_{OH} - V_{OL})}{2 \times R1}$$

$$R_B = \frac{(V_{CC} - V_{OH})}{I}; \quad R_A = \frac{(V_{OL} - V_{GND})}{I}$$

$$V_{GND} = 0\ V$$

$$P_{ECL} = \frac{(V_{OH} - V_{TERM})^2}{R1} + \frac{(V_{OL} - V_{TERM})^2}{R1} + V_{TERM}\left[\frac{(V_{OH} - V_{TERM})}{R1} + \frac{(V_{OH} - V_{TERM})}{R1}\right] \quad \textbf{(3)}$$

$$P_{LVDS} = \frac{(V_{OH} - V_{OL})^2}{2 \times R1} \quad \textbf{(4)}$$

Expected power dissipation of the LVPECL 1:10 repeater and LVDS repeaters

Figure 2 combines the quiescent power calculated from Tables 2 and 3 and uses the quiescent logic power of the LVPECL device and the total quiescent power of the LVDS devices in Table 1. The quiescent power consumption for the LVPECL device is much greater than that for the LVDS devices, even when only a 2.5-V V_{CC} is used. The only caveat is that this is quiescent power. While this is not significant for the bipolar LVPECL device, it is very significant for the CMOS devices, since the power consumption increases as a function of frequency. Figure 3 shows the expected power consumption of the three devices over frequency and extrapolated beyond the 622 Mbps maximum of the LVDS devices. The data over frequency is taken from the SN65LVDS108 and SN65LVDS116 data sheets, and the LVPECL device is assumed to be constant with no active power dissipation over frequency. With the data sheet values, the LVDS repeaters have an obvious power advantage over the LVPECL repeaters.

Figure 2. Expected quiescent power allocation

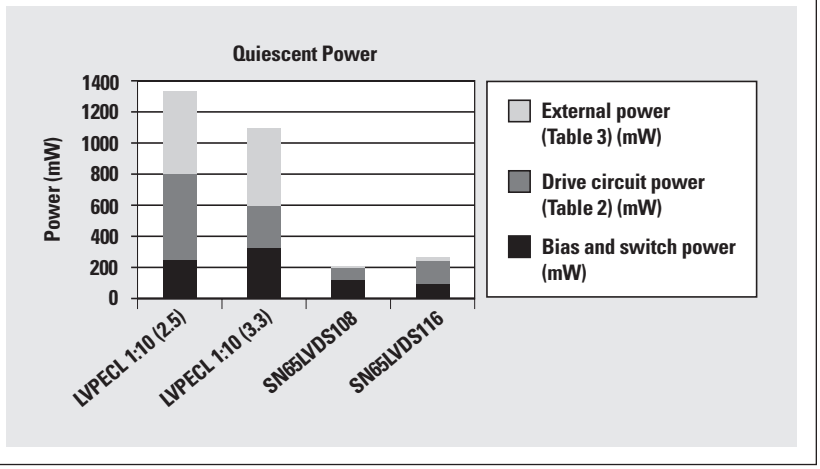
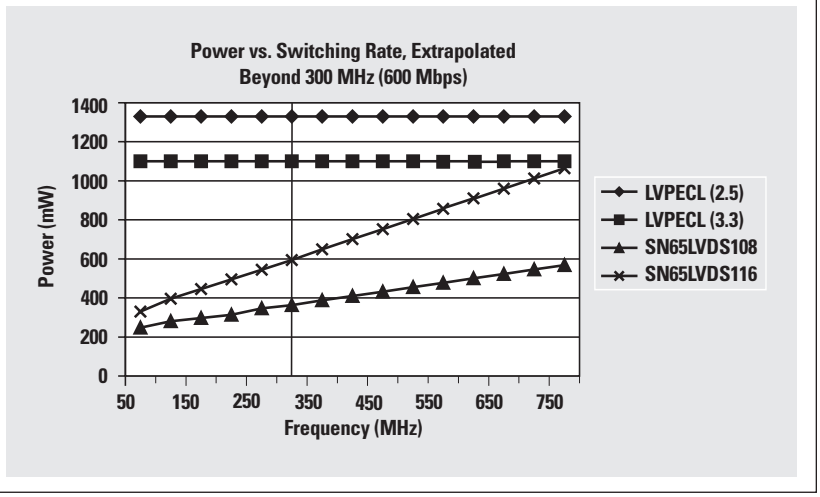


Figure 3. Expected power consumption over frequency



Conclusion

Actual results of the SN65LVDS116 and the LVPECL repeater are presented in Reference 5. The variances in the LVDS measurements with the expected values in Figure 3 are attributed to differences in the loads used; the values in Figure 3 are taken from the SN65LVDS116 and SN65LVDS108 data sheets, where the loads have a capacitive component. The differences between expected and measured values for the 2.5-V and 3.3-V LVPECL are 9.8% and 4.8%, respectively. While there is a variance between the results in Figure 3 and the actual measurements, the trends are the same and the LVDS device provides low-power performance over the LVPECL from 50 to 600 Mbps operation.

References

For more information related to this article, you can download an Acrobat Reader file at www-s.ti.com/sc/techlit/*litnumber* and replace *"litnumber"* with the **TI Lit. #** for the materials listed below.

Document Title	TI Lit. #
1. *High-Speed CMOS Data*, Data Book, DL129/D Rev. 7 (ON Semiconductor, March 2000).	—
2. Howard Johnson and Martin Graham, *High-Speed Digital Design, A Handbook of Black Magic* (Prentice-Hall PTR, 1993).	—
3. "SN65LVDS116 16-Port LVDS Repeater," Data Sheet	slls370
4. "SN65LVDS108 8-Port LVDS Repeater," Data Sheet	slls399
5. "LVPECL and LVDS Power Comparison," Application Report	slla103

Related Web sites

www.ti.com/sc/docs/products/analog/sn65lvds108.html
www.ti.com/sc/docs/products/analog/sn65lvds116.html

Audio power amplifier measurements, Part 2

By Richard Palmer
Application Specialist, Audio Amplifiers

Introduction

This article is a continuation of "Audio power amplifier measurements," which first appeared in the July 2001 issue of *Analog Applications Journal* (see Reference 1) and which contains guidelines for measuring the following three parameters:

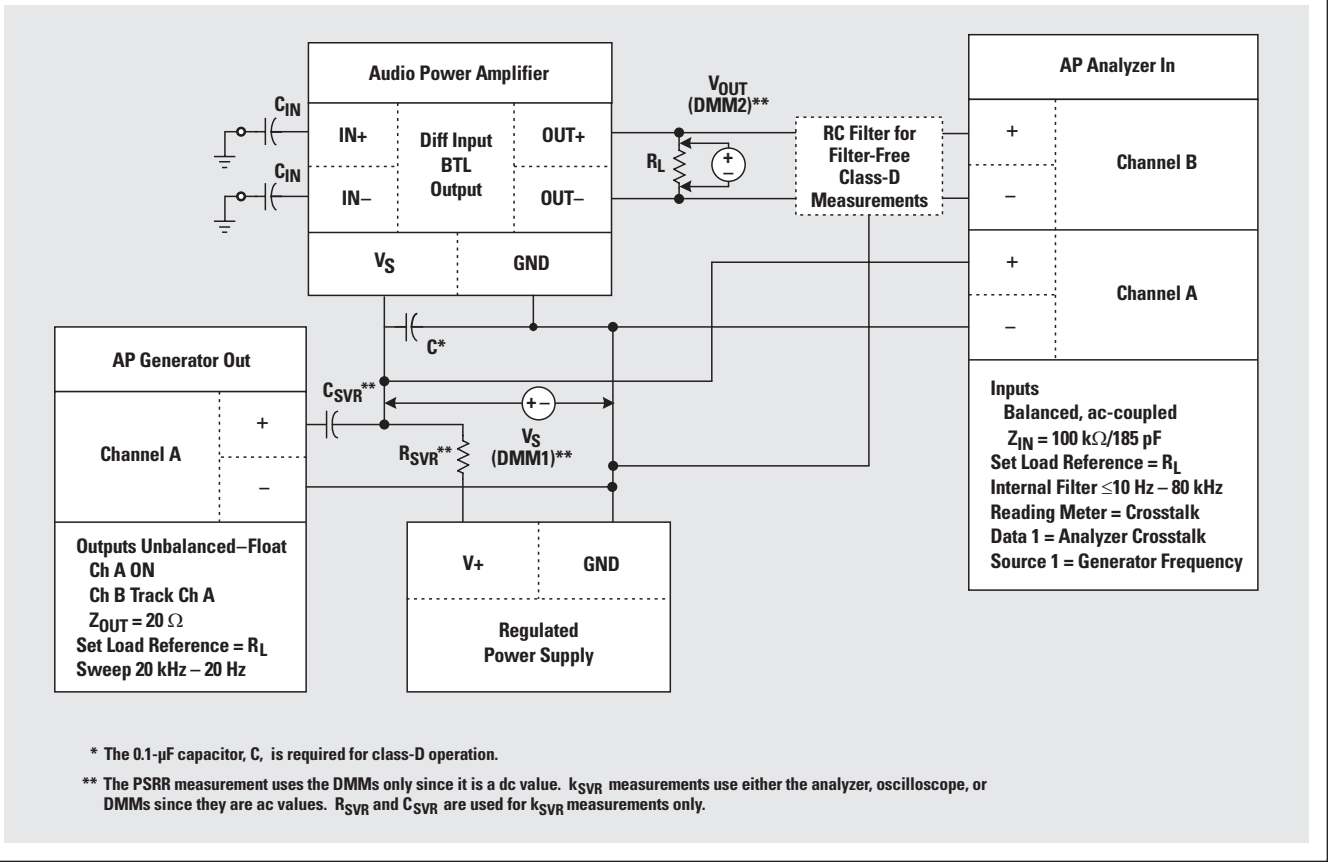
- power supply rejection ratio (PSRR),
- supply ripple voltage rejection ratio (k_{SVR}), and
- efficiency.

All measurements were made by using TI Plug-n-Play APA evaluation modules (EVMs) for the TPA2001D1 filter-free class-D and the TPA731 class-AB mono devices. Note that the graphs in the data sheets reflect typical specifications and were measured on test boards specifically designed to allow accuracy and ease of measurement. Board space, layout, and components were not constrained by size/cost requirements. The measurements in this article, however, were taken by using circuits on EVMs that reflect real-world layout constraints. The measurements of a particular audio circuit may vary from the typical specifications. A large variance is usually indicative of a PCB layout or measurement system issue. Reference 2 provides more details about the measurements in this article.

Supply rejection

Two types of supply rejection specifications exist: power-supply rejection ratio (PSRR) and supply ripple voltage rejection ratio (k_{SVR}). The only difference between them is that PSRR is a dc specification and k_{SVR} is an ac specification that measures the ability of the APA to reject ac-ripple voltage on the power supply bus. All power supply decoupling capacitors are removed from class-AB circuits, and class-D circuits have a small 0.1-µF decoupling capacitor, C, placed close to the APA power pins to provide a reverse path for recovery switching currents. It is recommended that the designer use equal decoupling capacitance values when comparing devices from different manufacturers to

Figure 1. PSRR and k_{SVR} measurement circuit



* The 0.1-µF capacitor, C, is required for class-D operation.

** The PSRR measurement uses the DMMs only since it is a dc value. k_{SVR} measurements use either the analyzer, oscilloscope, or DMMs since they are ac values. R_{SVR} and C_{SVR} are used for k_{SVR} measurements only.

get a valid comparison of the performance, since a higher capacitance equates to a better k_{SVR}.

PSRR is the ratio of the change in the output voltage, $V_{OUT(dc)}$, to a change in the power supply voltage, V_S, expressed in dB as shown in Equation 1.

$$PSRR = 20\log\left(\frac{\Delta V_{OUT(dc)}}{\Delta V_S}\right) \quad (1)$$

For example, the output voltage of an audio power amplifier that has a PSRR equal to –70 dB would change by 31.6 µV if the supply voltage changed by 0.1 V.

k_{SVR} is the ratio of the output ripple voltage, $V_{OUT(ac)}$, to a change in the supply ripple voltage, V_S, expressed in dB as shown in Equation 2.

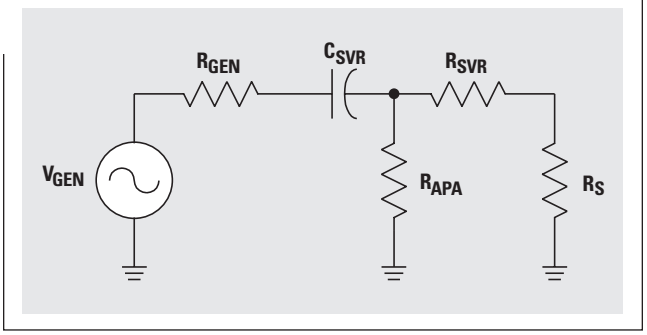
$$k_{SVR} = 20\log\left(\frac{V_{OUT(ac)}}{V_S}\right) \quad (2)$$

This parameter is normally listed as a typical value in the data sheet tables at a specified frequency and temperature of 1 kHz and 25°C, respectively. A graph is provided in the data sheet of the typical values of k_{SVR} over the audio bandwidth because it is a frequency-dependent term.

The PSRR and k_{SVR} measurement circuit is shown in Figure 1. All inputs are ac-coupled to ground. The PSRR measurement requires only the two DMMs. The power supply voltage, V_S, is initially set, then read from the meter on the power supply. When the power supply meter does not have the desired resolution, DMM1 is used to measure V_S. DMM2 then measures V_{OUT} across the load. V_S is then stepped up or down by a specific amount, and the corresponding value of V_{OUT} is measured. The differences of the two measurements are then substituted into Equation 1, and the PSRR is calculated for that specific change in supply voltage. PSRR is specified as a typical value that is valid for a given supply voltage range at 25°C.

The k_{SVR} measurement requires the signal generator, analyzer, a DMM, and the k_{SVR} filter components R_{SVR} and C_{SVR}. The RC measurement filter[1, 2] is used when the analyzer cannot accurately process the square wave output of the filter-free class-D APAs. DMM1 is used to measure V_S at the APA power pin. The generator injects a small sine wave signal onto the power bus, and the audio analyzer measures this ac voltage at the APA power pin and at the output. Here the analyzer, an Audio Precision System–II, is configured for a crosstalk measurement[1, 2]; it sweeps the ac voltage at constant amplitude over the audio band, measuring and presenting a graph of the data points in dB.

Figure 2. k_{SVR} filter circuit



The k_{SVR} filter circuit is shown in Figure 2. The dc power supply output impedance, R_S, is very low (milliohms); and the impedance of the APA to ground, R_{APA}, as seen by the power supply or signal generator, is very high (hundreds of ohms). The value of R_{SVR} is added to the circuit to increase the equivalent impedance of the power supply and is chosen to be approximately equal to the ac signal source generator output impedance, R_{GEN}. A voltage divider is formed between R_{SVR} and R_{GEN} that provides a reasonable amplitude ac signal at the APA power pin.

C_{SVR} is added to ac-couple the signal generator to the APA. The filter cutoff frequency, f_C, should be set 3 dB below the lowest frequency of the audio band, f_{MIN}, which in this case is 20 Hz. Equation 3 provides the value for f_C, which is ~14 Hz.

$$f_C = \frac{f_{MIN}}{\sqrt{2}} \quad (3)$$

The equivalent resistance is then calculated with Equation 4, where R_{APA} is the supply voltage divided by the quiescent current of the device (V_S/I_Q).

$$R_{EQ} = R_{GEN} + R_{APA} \parallel (R_{SVR} + R_S) \approx R_{GEN} + R_{SVR} \quad (4)$$

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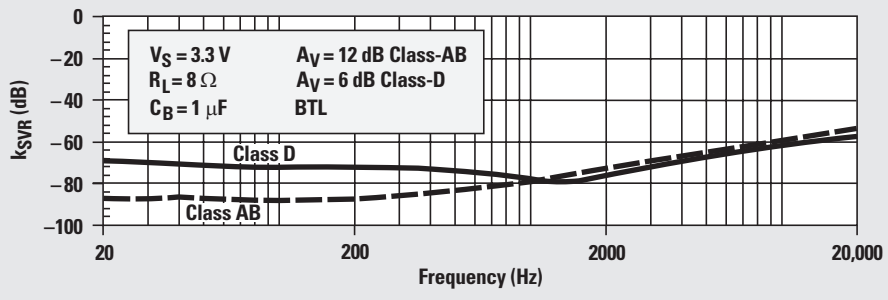
Figure 3. k_{SVR} of the TPA2001D1 and the TPA731



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The value for C_{SVR} is then calculated with Equation 5.

$$C_{SVR} = \frac{1}{2\pi \times f_C \times R_{EQ}} \quad (5)$$

The capacitor will most likely be electrolytic due to the value required. It will have some reactance that will vary with frequency as shown by Equation 6.

$$X_{C_{SVR}} = \frac{1}{2\pi \times f_C \times C_{SVR}} \quad (6)$$

At 20 Hz the impedance will be quite high—approximately the value of R_{GEN} and R_{SVR}; and at 20 kHz the value will be in the milliohms.

The actual values for the measurement circuit were R_{GEN} = 20 Ω, $R_S \approx 0$, R_{APA} = 5 V/6 mA = 833 Ω, C_{SVR} = 330 µF, R_{SVR} = 20 Ω, and f_C = 12 Hz. This yields a capacitive reactance of 24 Ω at 20 Hz, and 24 mΩ at 20 kHz. The value of the ac signal must be adjusted at low frequencies so that the desired voltage is applied to the APA power pin. The value of the dc voltage from the power supply must also be adjusted, since I_Q will create a small voltage drop across R_{SVR}.

Those devices with BYPASS pins will have improved k_{SVR} as the capacitance on the pin is increased. Those operated SE have lower k_{SVR}, particularly at the extreme low and high ranges of the audio band. This is primarily due to the resonance of the output ac coupling capacitor.

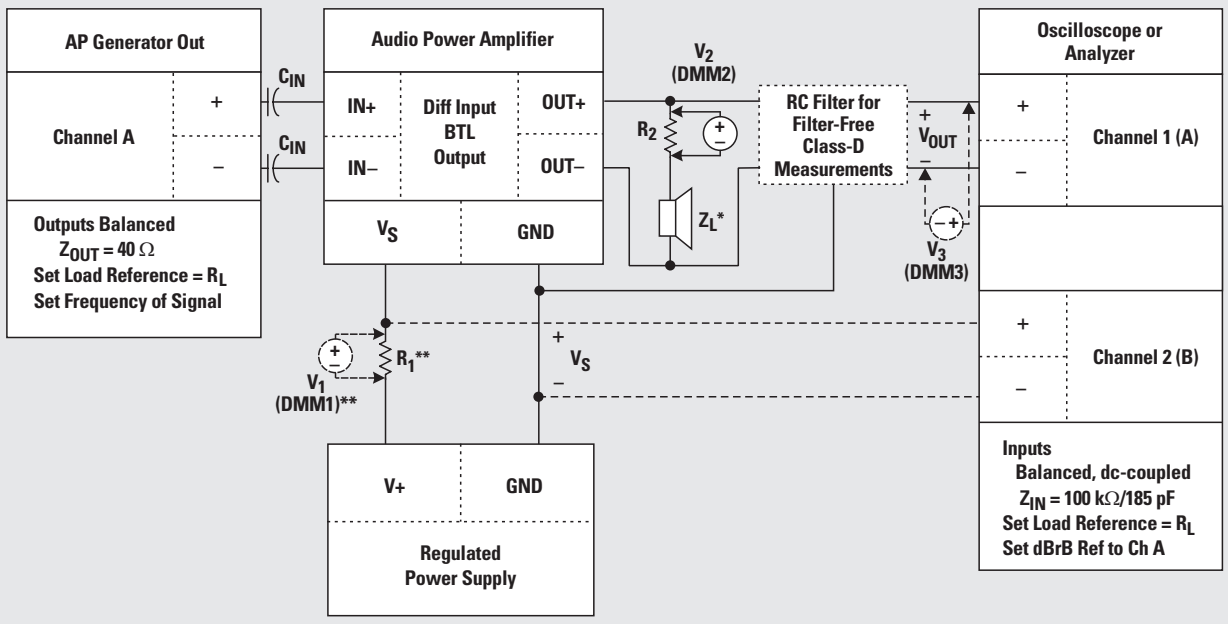
The k_{SVR} graphs of the TPA2001D1 and the TPA731 are shown in Figure 3. Both of these devices are differential input and BTL output. The TPA731 was measured with the inputs floating. Newer devices are typically measured with the inputs ac-grounded.

Efficiency measurements

Efficiency is the measure of the amount of power that is delivered to a load for a given input power provided by the supply. A class-AB APA acts like a variable resistor network between the power supply and the load, with the output transistors operating in the linear region. They dissipate quite a bit of power because of this mode of operation and are therefore inefficient. The output stage in class-D amplifiers acts as a switch that has a small resistance when operated in the saturation region, which provides a much higher efficiency.

A circuit for measuring the efficiency of a class-AB or class-D system is shown in Figure 4. The simplest setup occurs when the power supply voltage and current meters are accurate and have the resolution required. When the

Figure 4. Efficiency circuit, BTL



* Load Z_L is a speaker for class-D APAs and is a purely resistive load for class-AB APAs.

** DMM1 and Channel 2 of the AP/oscilloscope (or a third DMM) are used to measure the average power supply current and voltage when power supply meters are not accurate. Resistor R_1 can be removed when power supply meters are used.

supply current meter is not sufficient, R_1 is placed in the circuit. It should be a small value (0.1 Ω) and able to handle the power dissipated. The average voltage, V_1, across R_1 provides the average supply current ($I_S = V_1/R_1$) that is used to calculate the average power provided by the supply.

The true rms DMMs and the audio analyzer provide an rms value of both the voltage and the current, which, when multiplied together, provide the average power. When used, the power supply meters provide the average value of the supply voltage and current. The oscilloscope can measure the average or rms values of the power supply and output voltage. Some oscilloscopes even have current probes that can be used to measure the current through a wire, in which case R_1 is not needed.

The load measurement is different for class-AB and class-D APAs. Two elements are shown: one is the actual load, Z_L, and the other is resistor R_2. The Class-AB load is a non-inductive power resistor, $Z_L = R_L$. R_2 is not required for class-AB efficiency measurements since the load is purely resistive.

The filter-free class-D load is a speaker, so the impedance will vary with frequency. A speaker is used because it has the inductance that helps provide the high class-D efficiency. A purely resistive load is not a true indicator of the operating environment of the filter-free class-D, and will not provide accurate efficiency numbers. The power must be calculated independently of the speaker impedance since it varies with frequency. The small power resistor, R_2, provides a means of measuring the current that is used in the efficiency calculation ($I_{OUT} \approx V_2/R_2$).

Equation 7 provides the efficiency of the class-AB APA, and Equation 8 provides the efficiency of the class-D APA. The input power of both equations is just the average voltage applied to the power pin of the APA, multiplied by the average value of the power supply current. Average value is used for the power supply measurements, since the voltage and current have dc and ac components and are nonsinusoidal. The output power is also an average that results from the multiplication of two rms terms.

The RC measurement filter is used for making filter-free class-D output measurements when the analyzer or DMM cannot accurately process the switching waveform.[1, 2] The filter resistance must be large enough to minimize current flow through the filter; while the capacitance must be sized to achieve the desired cutoff frequency, which should be just above the audio band. If the filter resistor is not large enough, the filter current must be accounted for in the efficiency equation. The recommended values of R_{FILT} and C_{FILT} are 1 kΩ and 5.6 nF, respectively. This provides a filter cutoff frequency of ~28 kHz. This filter is not used with traditional class-D devices since they already have LC filters in the output circuit.

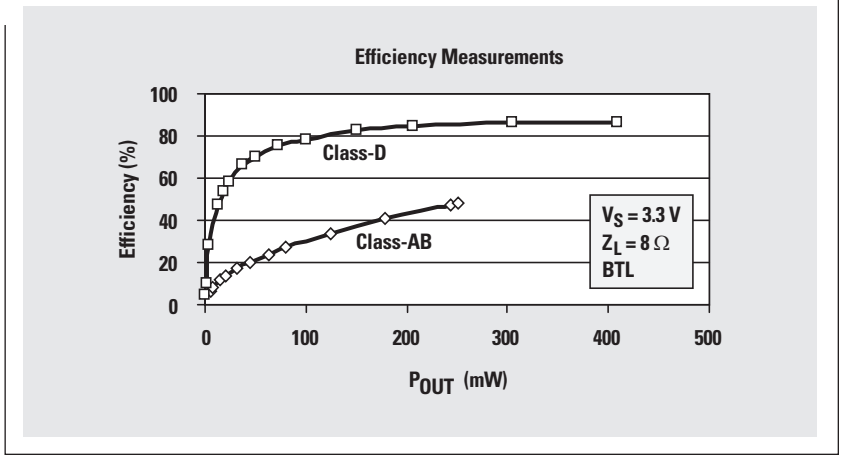
The efficiency was measured with a 3.3-V supply; the results are shown in Figure 5. Figure 5 provides the measured efficiency from the power supply meter and a Fluke 87III DMM measuring the voltage across the load.

Continued on next page

$$\eta_{Class-AB} = \frac{P_{OUT}}{P_S} = \frac{\left(\frac{V_{OUT(RMS)}^2}{R_L}\right)}{V_{S(AV)} \times I_{S(AV)}} \quad (7)$$

$$\eta_{Class-D} = \frac{P_{OUT}}{P_S} = \frac{V_{OUT(RMS)} \times I_{OUT(RMS)}}{V_{S(AV)} \times I_{S(AV)}} = \frac{V_{OUT(RMS)} \times \left(\frac{V_{R_2(RMS)}}{R_2}\right)}{V_{S(AV)} \times I_{S(AV)}} \quad (8)$$

Figure 5. Efficiency of the TPA731 class-AB APA and the TPA2001D1 class-D APA



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The DMM class-AB data was in close agreement with measurements made with the AP-II Analyzer or a TDS 754 oscilloscope. The class-D DMM and AP data were similar, but the oscilloscope measured 5–10% higher due to its averaging, which introduced a somewhat large margin of error, particularly at high power output. The DMM reading is more reliable, since it filters out the high-frequency harmonics of the switching waveform to provide a more stable, low-frequency value. Tables of measurement values for both amplifiers are available in Reference 2.

Power dissipated versus power to the load

The efficiency measurements provide the information required to calculate the amount of power dissipated, P_D, in the amplifier. P_D provides some insight into the supply currents and power that will be required. P_D is calculated by using Equation 9 and the measured values of supply and output power from the efficiency measurements. It is assumed that the power dissipated in the RC filter, used for the filter-free class-D APA measurements, is negligible; therefore it is not included in the calculation. When it is significant, it must be included as part of P_{OUT}.

$$P_D = P_S - P_{OUT} \quad \textbf{(9)}$$

Figure 6 shows graphs of dissipated power versus the output power calculated with Equation 9. The data was measured up to the maximum output power, which occurs just prior to clipping, and can easily be discerned from a graph of THD+N versus output power.[2] The designer can choose the percent distortion (level of clipping) that is acceptable for a system and test the device through that power level.

Crest factor and output power

The crest factor (CF) is the ratio of the peak output to the average output. It is typically graphed in terms of output power and is in units of dB. For example, the crest factor of a sine wave is 3 dB. Sine waves are used in the characterization of APA performance but do not give a clear idea of what the performance will be with music. The CF of music may vary between 6 dB and 24 dB and directly impacts the amount of heat dissipated in the device—the higher the crest factor, the lower the heat dissipated and the higher the ambient operating temperature may be. The P_D data discussed in the previous two paragraphs can be used to determine the CF of the device.

Equation 10 may be used to calculate CF. Since a sine wave was used for the measurements, the crest factor is 3 dB, and the average output power, $P_{OUT(AV)}$, is known. The peak output power, $P_{OUT(PK)}$, is calculated by manipulating Equation 10 into Equation 11, where $P_{OUT(PK)}$ and $P_{OUT(AV)}$ are expressed in watts and CF is expressed in dB.

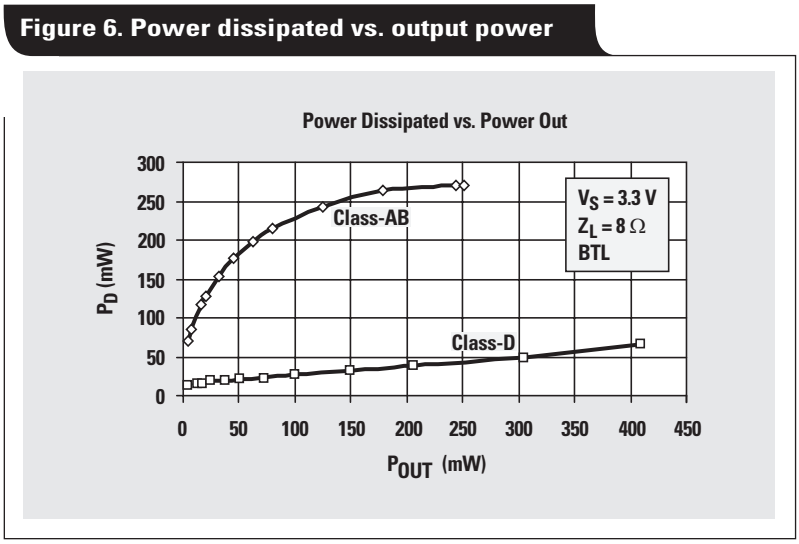
$$CF(dB) = 10\log\left(\frac{P_{OUT(PK)}}{P_{OUT(AV)}}\right) \quad \textbf{(10)}$$

$$P_{OUT(AV)} = \frac{P_{OUT(PK)}}{10^{\left(\frac{CF}{10}\right)}} \quad \textbf{(11)}$$

For example, the maximum peak output power is 500 mW for the TPA731. This is calculated by using 250 mW as $P_{OUT(AV)}$ and a CF of 3 dB for the output sinusoid. The peak will not change throughout the calculations, as it is the maximum output power possible and is independent of the output waveform. The CF is then increased in 3-dB steps up to 18 dB, and the corresponding $P_{OUT(AV)}$ is calculated for each step. The P_D in the device is measured for each value of $P_{OUT(AV)}$ with the efficiency measurement circuit.

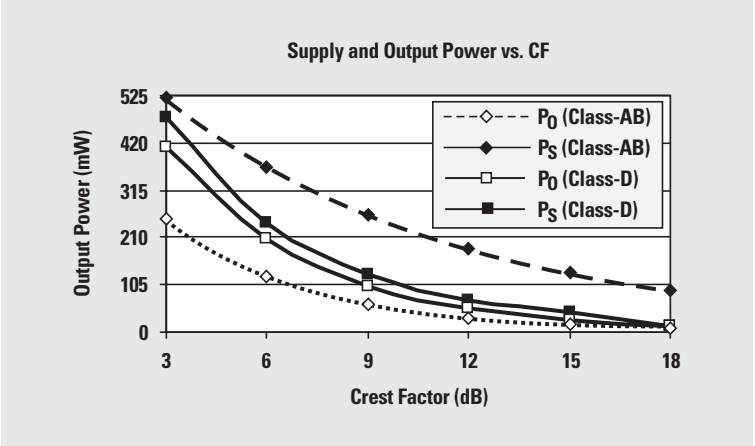
The efficiency data and CF calculations can help the designer approximate the power that must be provided by

Figure 6. Power dissipated vs. output power



the power supply. Figure 7 shows the graph of P_S and P_{OUT} versus crest factor. The graph allows easy comparison of the devices, and it is clear that the class-D APA provides more P_{OUT} with less power from the supply than the class-AB APA. The difference between P_S and P_{OUT} is the dissipated power, P_D.

Figure 7. Supply and output power vs. CF



Measurement pitfalls

The following is a list of common pitfalls, or mistakes, that can be encountered and will produce measurement errors.

- The signal generator should be balanced for differential inputs, unbalanced for SE inputs.
- Wires should be twisted together to minimize magnetic coupling into loops and ground loops.
- Use the RC measurement filter for the filter-free class-D outputs when using an analyzer or oscilloscope. The capacitor should be connected to either the power supply or the APA power ground.
- The leads of filter components should be kept short.
- The DMM must be "true rms" to get accurate measurements.
- The wires from the power supply and from the APA to the load should be at least 18 AWG for 2-W APAs.[2]

Supply rejection ratio measurements

- A 0.1-µF decoupling capacitor is required for class-D operation. All other capacitors should be removed. All decoupling capacitors should be removed for class-AB measurements.

Efficiency measurement

- The filter-free class-D RC measurement filter should have a high resistance for R_{FILT}, with a value of 1 kΩ recommended in conjunction with a 5.6-nF capacitor. The current through the filter must be considered when R_{FILT} is small.
- Check to make sure that the DMMs used at the load are set to measure ac volts and to measure dc volts at the power supply.

References

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Document Title	**TI Lit. #**
1. Richard Palmer, "Audio power amplifier measurements," *Analog Applications Journal* (July 2001), pp. 40-46.	slyt135
2. "Guidelines for Measuring Audio Power Amplifier Performance," Application Report . . .	sloa068

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www.ti.com/sc/docs/products/analog/tpa731.html
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Product Information Centers

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Europe, Middle East, and Africa

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Israel (English)	1800 949 0107
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Netherlands (English)	+31 (0) 546 87 95 45
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Japan

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	Domestic	0120-81-0036
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Asia

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International	+886-2-23786800	
Domestic	Local Access Code	TI Number
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