ADS809 analog-to-digital converter with large input pulse signal

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Introduction

The Texas Instruments (TI) ADS809 is a 12-bit, 80-MHz pipeline analog-to-digital converter (ADC). It has high speed, high resolution, high-input bandwidth, and a high signal dynamic range. Its many other good features include good signal-to-noise-ratio (SNR), good linearity, low jitter, flexible clocking, an over-range indicator (OVR), "data valid" output, three-state output, an internal or external reference, and a single-ended or differential input configuration. It can be used for broadband communications, test equipment, medical instrumentation, CCD imaging, and other fast-ADC applications.

In these applications the input analog signal applied to the ADS809 varies and may be a DC, AC, narrow band, wide band, or pulse signal with a large amplitude. The sampling clock used for these applications can be up to 80 MHz with a uniform or non-uniform clock phase. Different applications require different critical features of the ADS809. In some conventional sampling applications, the ADC input analog signal is smooth with a large amplitude, and the SNR and spurious-free dynamic range (SFDR) are critical; while in some small-signal sampling applications, the SFDR and full-scale (FS) step-acquisition time are not as critical. However, the FS step-acquisition time is critical in large-signal sampling applications, especially when the sampling clock has to be high-frequency with a non-uniform phase and the analog input pulse signal is large (for example, 2 V). In this case the input signal has a sharp edge with a large voltage amplitude, and the pulse edge could be very close to the sampling clock edge due to sampling clock phase variations. If the ADC does not have fast step response for the signal settling, the next ADC sample after the pulse edge will be unstable, which is undesirable. Therefore it is critical for the ADC to have a fast settling time when a large input pulse signal is sampled. Similarly, when the input pulse is over full-scale range (FSR), it is important for the ADC to have a fast over-range recovery time. This is tough for any ADC in applications where the input pulse signal is large and sampling speed is very high with a non-uniform clock phase. However, the ADS809 works well with this type of application. This article presents the results of recent lab tests that further prove the ADS809's fast step response with a large, FS input pulse. The test data also covers the ADS809's response to over-range conditions.

Over-FSR performance of the ADS809

The ADS809's over-voltage condition is defined as the input voltage in excess of its maximum linear conversion range. The voltage FSR of the ADS809 can be set as 2 V_{p-p}, 1.5 V_{p-p}, 1 V_{p-p}, or another range based on the internal or external voltage reference configuration. For single-ended input, the maximum voltage at the ADS809 input pin is +FS (½ FSR above 2.5-V common-mode voltage), and the minimum voltage at input is –FS (½ FSR below 2.5-V common-mode voltage). For differential input, +FS is ¼ FSR above 2.5-V common-mode voltage, and –FS is ¼ FSR below 2.5-V common-mode voltage. For the input voltage over FSR, the ADS809 has control features that include 12-bit data-code control and an OVR.

Figure 1. Output of ADS809 with input pulse over FSR at 66-MHz sampling clock
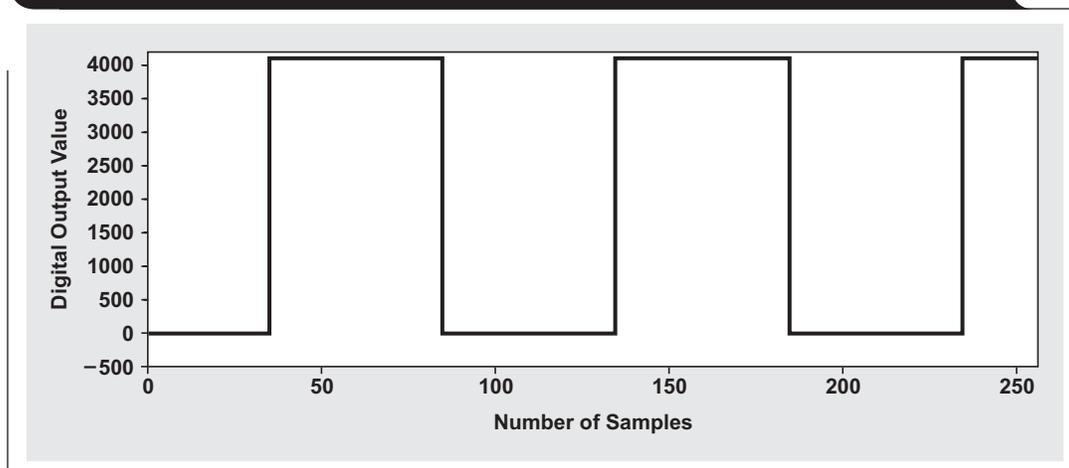
The digital output code of the ADS809 is straight offset binary or binary two's complement. In straight offset binary format, when the input voltage is maximum, the ADS809 outputs all 12 data bits as 1s (digital value = 4095); and when the input voltage is minimum, the ADS809 outputs all 0s. When the input voltage is 0 (at the middle of the FSR) or only the common-mode voltage, the ADS809 outputs 100000000000 (digital value = 2048). The ADS809 will output data from 0 to 4095 when the input voltage is from –FS to +FS – LSB. The ADS809 will output 4095 when the input voltage is above +FS, and will output 0 when the input voltage is below –FS.

The ADS809 output-code control was tested with the ADC sampling clock at 66 MHz and the input differential pulse amplitude at 2.8 V (0.8 V over FSR). The test result shows that the ADS809 has stable output-code control and quick over-range recovery from the input pulse signal. This is shown in Figure 1. The ADS809 samples 255 digital output samples at 66 MSPS from an over-FS input pulse. The data shows that all the bits are stable at 1 when the input pulse signal is over +FS, and stable at 0 when the input pulse signal is under –FS. The data also shows that when the input pulse signal goes from over FS to under FS or vice versa, the output of the ADS809 tracks the input step change and stays at 4095 or 0 without any miss code or bit flip.

Another over-FSR control feature of the ADS809 is an OVR output pin, which indicates over-range conditions. The OVR output is a function of the reference voltage and the output data bits, so it has the same pipeline delay as the output data bits. The OVR is logical low if the input signal is within the FSR, and logical high if the input signal is over +FS or under –FS. The OVR changes from logical low to high, or logical high to low, immediately following the change of the output data. When this happens, the input voltage changes from inside the FSR to outside the FSR or vice versa. When the input signal continues under or over FS, the OVR always remains high. When the input signal changes from under FS to over FS or vice versa, the OVR changes from high to low for ½ CLK period, then changes to high again. In other words, the OVR outputs a negative pulse at the transition of the input voltage from over FS to under FS or vice versa (see Figure 2). The output's most significant bit (MSB) pin is flipped based on the over-FS input pulse. It is high when the input pulse is over FS and low when the input pulse is under FS. The OVR pin outputs a negative pulse that appears half of the sampling clock period earlier than the transition at the MSB pin.

FS step response of ADS809 and measurement method

The FS step response or step-acquisition time of the ADS809 is defined as the time for the input signal to settle or for the internal sample-and-hold (S/H) circuit to track the input signal with a certain accuracy (for example, 0.1% FS) after the FS step signal is applied to the ADS809. The ADS809 settling time of a FS step signal is 5 ns, which is typically within 0.1% FS and is the minimum required interval between the input step edge and the next sampling clock edge.

The fast step response of the ADC is important in applications with a non-uniform sampling clock, because the variation of the sampling clock phase can cause a phase change between the input pulse and the sampling clock. This is shown in Figure 3, where the rising edge of the clock samples the input pulse signal; and the time, t_S, between the input step edge and the next rising edge of the sampling clock changes with the sampling clock phase change. When t_S is less than the ADC's minimum value, the ADC will take an unstable sample from the unsettled input signal, which is undesirable.

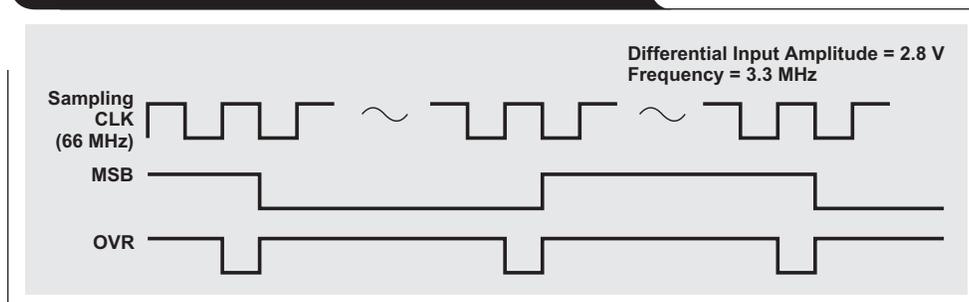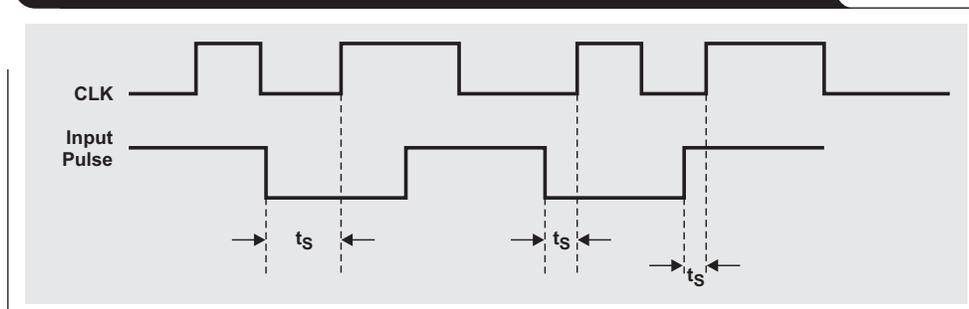### Figure 2. OVR of ADS809 with input pulse over FS

Differential Input Amplitude = 2.8 V
Frequency = 3.3 MHz

Sampling CLK (66 MHz)

MSB

OVR

Figure 3. The input step appears during the clock's tracking time because of clock phase variation
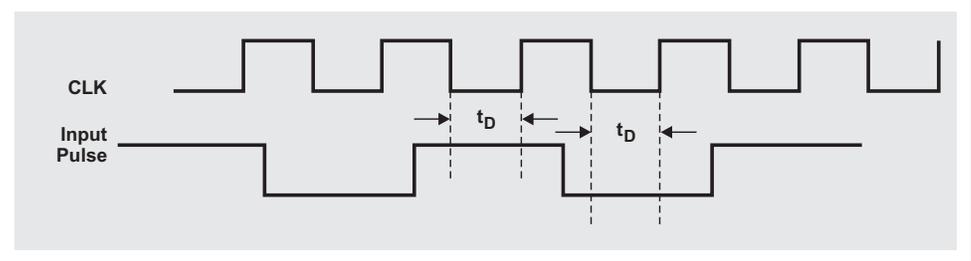

CLK

Input Pulse

t_S t_S t_S

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There are two ways to eval-
uate the step response. One is
measuring the time, t_S, shown
in Figure 3. Another is measur-
ing the relative tracking time,
t_D, of the sampling clock
shown in Figure 4.

Figure 4. The input step does not appear during the clock's tracking time

In the first method, the step
signal (pulse edge in this case)
is applied to the input of the
S/H circuit directly during the
tracking phase. By delaying
the input pulse or sampling clock, we can find the minimum
t_S, the first stable sample location after the pulse edge,
where the pulse signal level has been recovered with the
accuracy specified in the data sheet. This minimum t_S is
the step response of the ADC. In this method, highly accu-
rate measurement is needed. The signal input path of the
ADC should be clean. Large external input capacitance
from the board can cause signal step edge distortion, and
poor board layout with source impedance mismatch may
cause energy reflection or ringing. The probe capacitance
of the oscilloscope is also a concern. The shape of the step
edge and the detailed timing between the step signal and
the ADS809 sampling clock should be carefully measured,
including the ADS809 aperture time.

The second and simpler method of step-response evalu-
ation is to measure the clock's tracking time, t_D, shown in
Figure 4. In this method the clock's tracking edge appears
after the input signal step edge. The clock's tracking edge
triggers the ADS809 S/H circuit, changing the previous
voltage at the sampling capacitor to the current voltage of
the input pulse. The step-response time of the ADS809 S/H
circuit should be the same as in the first method (measur-
ing t_S) due to the same RC constant. If the tracking time
during t_D measurement is too short, the first sample after
the step signal will be unstable. The minimum tracking

time of the ADC should be less than or close to half of the
sampling clock cycle at the maximum speed specified.

Bench test of ADS809 step response

A real bench test was performed to determine the ADS809
step response with the method shown in Figure 3 (measur-
ing t_S). The basic test block diagram of the ADS809 is shown
in Figure 5. The ADS809 was configured with an internal
reference, a differential analog input with 2-V FSR, a differ-
ential clock input, and an external 2.5-V common-mode
voltage for the analog input, with no added load on the
common-mode (CM) pin except normal bypass capacitance.

The differential analog input of the ADS809 was a pulse
from the pulse generator with a frequency of 3.3 MHz and
an amplitude of 2.92 to 2.08 V (high to low) at each analog
input, near FSR. This input produced the digital output
values of 3770 and 300 (high and low), including a small
amount of DC offset. The input pulse's transition from high
to low was used as the step signal in the bench test. The
single-ended, 66-MHz sampling clock from the pulse genera-
tor was converted differentially through a differential trans-
lator. A Tektronix logic analyzer (TLA) was used to collect
the digital output of the ADS809 to determine whether the
sample was stable. After the input step signal, the digital
value of the first sample should be 300, within an accuracy

Figure 5. Basic test block diagram for ADS809 step response
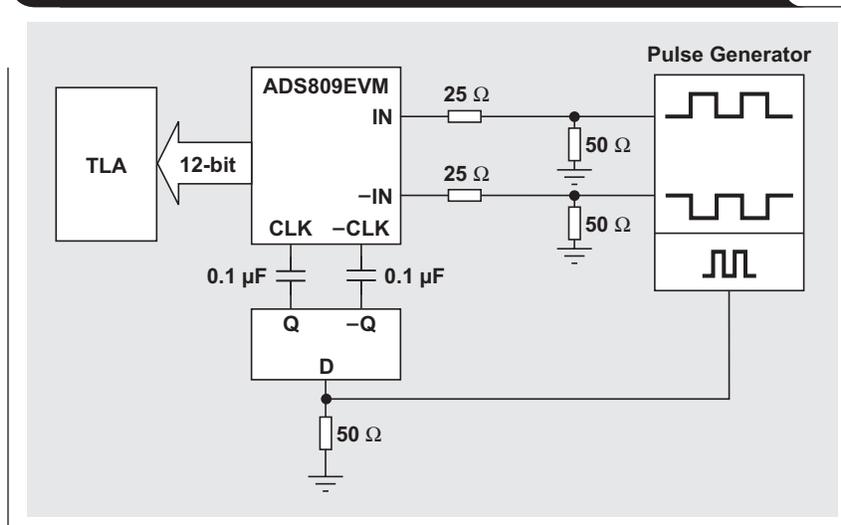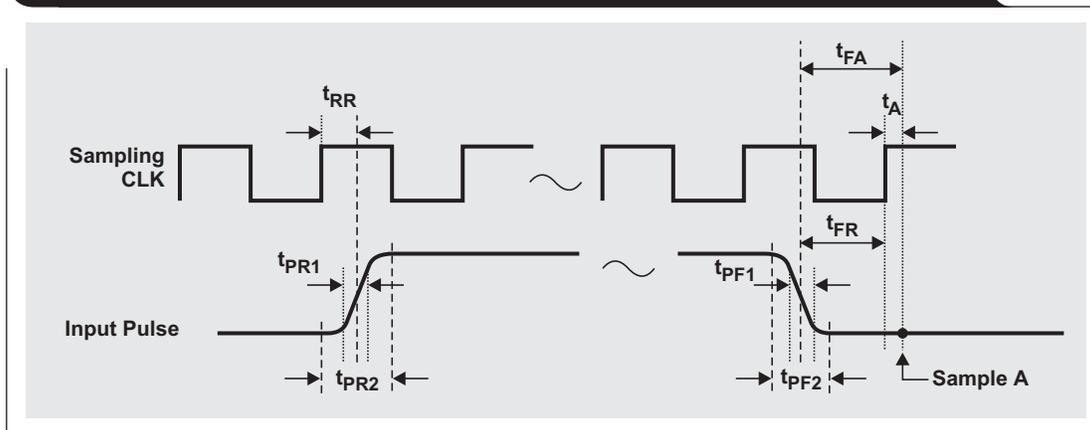
Figure 6. Timing measurement of sampling clock and input pulse at zero delay

of 0.1% FS, if the time interval between the step signal and the clock sampling edge is 5 ns or more as specified.

Three measurements were necessary in this bench test: aperture delay; input signal timing between the sampling clock and the input pulse; and the digital output of the ADS809 with input pulse delay.

The aperture delay, t_A, is the time from the rising edge of the sampling clock to the time when the sampling actually happens (see Figure 6). The data sheet provides only a typical value for t_A (3 ns). In the bench test the aperture delay was found by measuring the MSB and the time from the rising edge of the sampling clock to the falling edge of the pulse.

Figure 6 shows the measurement of the input signal timing between the sampling clock and the input pulse at zero delay. This measurement provides pulse edge information and a time reference for the input signal delay. The measurement was taken by Tektronix scope at the ADS809 input and clock input pins. The measurement data is shown in Table 1.

Table 1. Bench test measurement data

PARAMETER	MEASURED VALUE
Input pulse rising time (10% to 10%), t_{PR1}	1.1 ns at analog input pin IN
Input pulse falling time (10% to 10%), t_{PF1}	0.8 ns at analog input pin IN
Input pulse rising time (0.01% to 0.01%), t_{PR2}	2.7 ns at analog input pin IN
Input pulse falling time (0.01% to 0.01%), t_{PF2}	2.8 ns at analog input pin IN
Clock rising edge to pulse rising edge (50% to 50%), t_{RR}	8.5 ns at pins CLK and IN
Pulse falling edge to clock rising edge (50% to 50%), t_{FR}	6.59 ns at pins CLK and IN

After the input timing was measured, the input pulse delay, t_{Del}, was up to 12 ns in steps of 1 ns or less. When t_{Del} was 0, the time from the input pulse falling edge to the next rising edge of the sampling clock, t_{FR}, was 6.59 ns; and Sample A, the first sample after the high-to-low transition of the input pulse, was located at 9.59 ns ($t_{FR} + t_A = t_{FA}$) from the pulse falling edge (see Figure 6). With the increase of the input pulse delay, t_{FR} decreased and Sample A moved close to the falling edge of the input pulse. When the pulse delay was more than 9.5 ns, Sample A moved to the left side of the falling edge of the input pulse (see Figure 7).

Figure 7. Sample A moves with step signal delay

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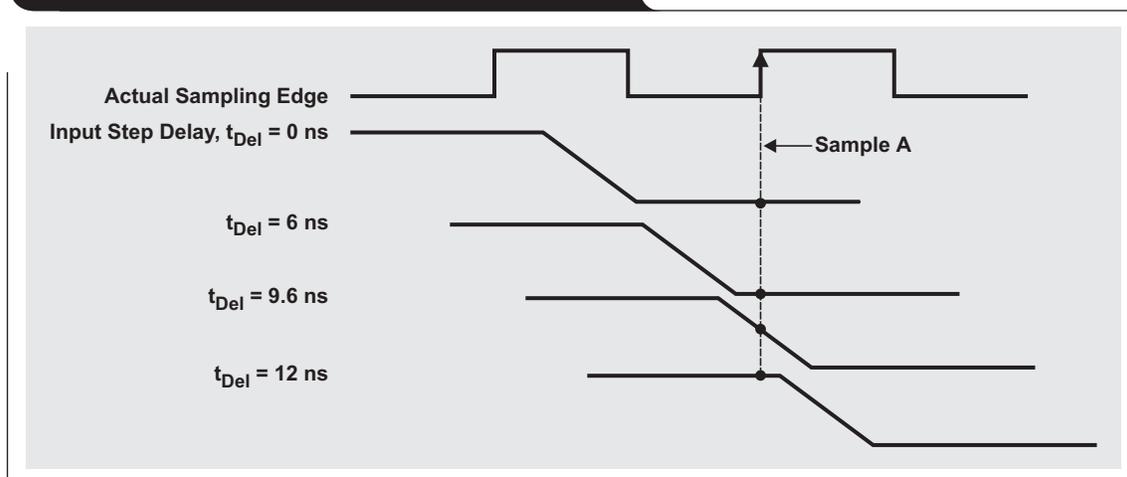
Sample A was collected by TLA, and its digital data is shown in Table 2. The Sample A output value of the ADS809 should be 300 (within an accuracy of ±0.1% FS) if t_{FR} is 2 ns or longer. In other words, Sample A is settled if the time t_{FA} ($t_{FR} + t_A$), from the falling edge of the input pulse to the actual sampling time of Sample A, is 5 ns or longer. For example, the digital value of Sample A is 299 when t_{FA} is 5.59 ns, and 300 when t_{FA} is about 9.59 ns, due to the input signal tracked by the ADS809 at these times. Sample A is unstable (the digital value is out of the range of 300 ± 0.1% FS) if t_{FA} is shorter than 5 ns. This is shown in Table 2 and Figure 8. For example, when t_{FA} is 3.59 ns, the digital value of Sample A is 358, which is significantly higher than 300, because the input signal has not recovered its low level after the high-to-low step of the input pulse. When t_{FA} is between 0.09 and –0.01 ns (see Table 2), Sample A hits the center of the falling edge or the middle scale of the ADS809. At this point t_{FR} reflects the aperture time of the ADS809. Continually delaying the input pulse eventually moves Sample A into the high level of the input pulse. When t_{FA} is less than –1.41 ns, the digital value of Sample A is about 3770 (see Figure 8). By this measurement, the step-acquisition time of the ADS809 is evaluated as 5 ns, within an accuracy of 0.1% FS, which matches the data sheet.

The test data introduced here includes a small error from the input timing measurement by the scope. There are actually many factors that can affect this type of measurement. The main one to point out here is that different input signal path conditions will have different digital values of Sample A at the same time space, t_{FA}. This could lead to a misinterpretation of the step-response time measurement. During the measurement, three different input signal path conditions were tested. In Condition 1, a 100-pF capacitor

Table 2. Digital value of Sample A versus input signal delay

t_{Del} (ns)	t_{FR} (ns)	t_{FA} (ns)	A (digital value)
0	6.59	9.59	300
1	5.59	8.59	299
2	4.59	7.59	301
3	3.59	6.59	296
4	2.59	5.59	299
5	1.59	4.59	315
6	0.59	3.59	358
7	–0.41	2.59	480
8	–1.41	1.59	739
9	–2.41	0.59	1277
9.5	–2.91	0.09	1902
9.6	–3.01	–0.01	2195
10	–3.41	–0.41	3334
11	–4.41	–1.41	3768
12	–5.41	–2.41	3767

was added at the input of the ADS809 on the EVM board. In Condition 2, this 100-pF capacitor was taken off the board. In Condition 3, the 100-pF capacitance was taken off the board and a 25-Ω damping resistor was added on the input path of the board. All three conditions ran with the sampling clock at 66 MHz, the input pulse at 3.3 MHz, the differential pulse amplitude at 1.68 V, and a zero delay to all input signals. The test data shows significant variation of the digital value of Sample A. Condition 1 produced the largest variation, mainly caused by edge distortion of the input pulse due to the external capacitor. Condition 3 produced the smallest variation, mainly caused by board layout and mismatch of the signal source impedance.

Figure 8. Step-response measurement data
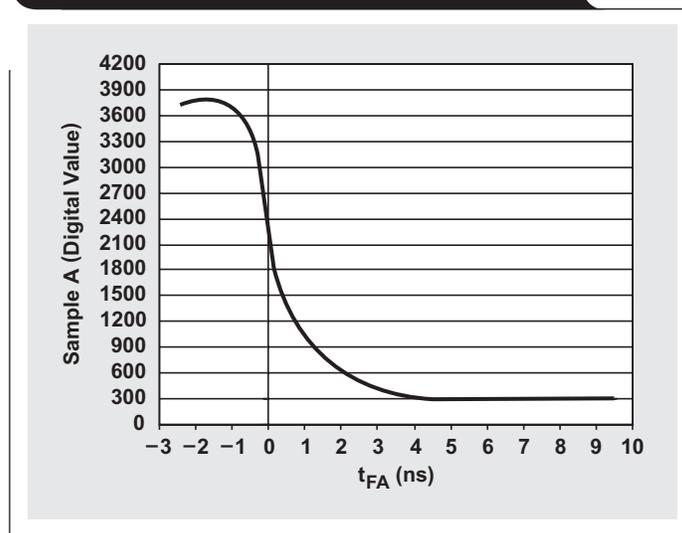
Conclusion

The ADS809, with 12-bit resolution and an 80-MSPS sampling speed, is used not only for conventional but also for nonconventional ADC sampling applications. An example of the latter is an ADC with a high-speed sampling clock with a non-uniform sampling phase that converts a large-amplitude input pulse signal. Such an application requires fast ADC settling time. This article has provided some test data based on the conditions of this type of application, including an over-FS control function and FS step-response measurement. The test data shows that the ADS809 has stable output-code control and stable OVR output when the input pulse signal is over 2-V FS. The ADS809 can convert a 2-V FS input pulse signal at an 80-MHz sampling rate and produce a stable output code. An actual bench test of the ADS809's FS step response was conducted; and the test method, procedure, and test results have been presented. The test data shows that the ADS809 has a FS step-acquisition time of 5 ns. It also indicates that the ADS809 has a large input dynamic range, a high-input bandwidth, and a fast, FS step response, making it suitable for large-signal sampling applications.

References

For more information related to this article, you can download an Acrobat Reader file at www-s.ti.com/sc/techlit/ *litnumber* and replace *"litnumber"* with the **TI Lit. #** for the materials listed below.

Document Title	TI Lit. #

1. "12-Bit, 80MHz Sampling Analog-to-Digital Converter," ADS809 Data Sheet sbas170
2. Mikael Gustavsson, J.J. Wikner, and N.N. Tan, *CMOS Data Converters for Communications* (Kluwer Academic Publishers, 2000).   —

Acknowledgments

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