Application Report
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AN-1238 Wide Bus Applications Using Parallel BLVDS SerDes Devices

ABSTRACT

Currently, BLVDS SerDes devices from National Semiconductor are available in 10-bit and 16-bit configurations. In cases where there are more parallel bits to transmit than a single SerDes can handle, multiple SerDes pairs can be used in parallel to perform the task provided certain constraints are met. The problem is clock to data skew. Not the skew between a deserializer's recovered clock (RCLK) and it's recovered data, but rather, between the RCLK of one deserializer and the data recovered by a second deserializer operating in parallel. For each SerDes pair the phase between the RCLK and the recovered data is relatively constant, but any difference in delay from one serial stream to another will result in skew between the RCLKs of the deserializers and hence the data of one deserializer and the RCLK of another. Since the client receive device must ultimately use only 1 RCLK, skew between the serial streams will affect the setup and hold times of the parallel data presented to it.

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This application note will show how to use the datasheet parameters t_{SD} (Serializer Delay) and t_{DD} (Deserializer Delay) to determine the timing constraints at the client receiver parallel interface when using SerDes in parallel.

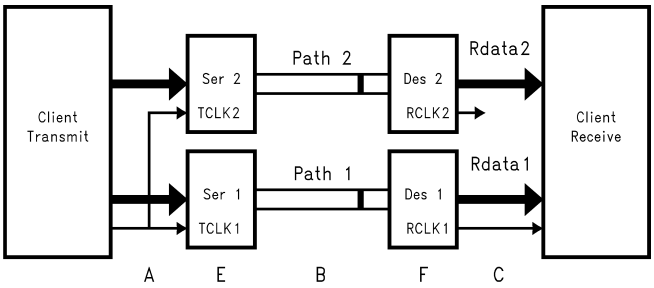

Figure 1. Parallel Serializers and Deserializers

1 SOURCES OF PATH SKEW

First let's look at the sources of phase offset (skew) in the paths. The diagram in Figure 1 shows two SerDes being used in parallel to transmit data from the client transmit device to the client receive device.

- **A** is the flight time between TCLK1 and TCLK2 from the Client Transmit.
- **E** is the serializer delay t_{SD}. The deserializer delay consists of a fractional number of clock cycles whose delay is proportional to the clock rate, and, a constant delay which is the result of propagation delays in the serializer.
- **B** is the flight time from serializer 2 to deserializer 2 or from serializer 1 to deserializer 1. This may be over PCB traces or through cables.
- **F** is the deserializer delay t_{DD}. The deserializer delay consists of a fractional number of clock cycles whose delay is proportional to the clock rate, and, a constant delay which is the result of propagation delays in the deserializer.
- **C** is the RCLK flight time from Deserializer 2 or Deserializer 1 to the client receive.

In this example the RCLK from deserializer 1 (RCLK1) is used to clock all of the recovered data from both deserializers into the client device. The recovered clock from deserializer two (RCLK2) is not connected. Since the recovered data (Rdata2) from deserializer 2 is in phase with RCLK2, the phase difference between RCLK 1 and RCLK 2 can be used to determine the timing constraints between data from deserializer 2 and the RCLK from deserializer 1.

The total time for data passing through path 1 is the sum of the flight times of PCB traces and other interconnections, and the delays of the serializer and deserializer.

Path 1 = $A_1 + B_1 + C_1 + E_1 + F_1$

The total time for data through path 2 is the sum of the flight times and the delays through those devices.

Path 2 = $A_2 + B_2 + C_2 + E_2 + F_2$

So the phase difference ($\Delta\varphi$) at the client receive is the difference of the overall delays in path 1 and path 2.

$\Delta\varphi = (A_1 + B_1 + C_1 + E_1 + F_1) – (A_2 + B_2 + C_2 + E_2 + F_2)$

With careful PCB layout, the flight times within the two paths can be made so that $A_1 = A_2$, $B_1 = B_2$, and $C_1 = C_2$ now the phase difference contributed by these segments will be negligible and any phase difference between the paths can be attributed solely to the serializer and deserializer delays t_{SD} and t_{DD} (E + F).

If $(A_1 + B_1 + C_1) = (A_2 + B_2 + C_2)$

then

$\Delta\varphi = (E_1 + F_1) - (E_2 + F_2)$

$\Delta\varphi = (t_{SD1} + t_{DD1}) - (t_{SD2} + t_{DD2})$

2 DETERMINING THE WORST CASE SKEW

The worst case phase difference will occur when the minimum delays are experienced in the serializer and deserializer in one path, the MIN path, and the maximum delays are experienced in the serializer and deserializer in the other path, the MAX path. These worst case delays are specified by t_{SDmin} and t_{SDmax} for the serializers and by t_{DDmin} and t_{DDmax} for the deserializers.

$\Delta\varphi = (t_{SDmax} + t_{DDmax}) - (t_{SDmin} + t_{DDmin})$

The maximum skew between serial streams in an otherwise skew controlled design can be determined using the maximum and minimum values of the Serializer Delay and Deserializer Delay parameters.

In Figure 1 RCLK1 (the recovered clock from deserializer 1) is selected as the reference clock for the client receive device. All data presented to the client receive device is referenced to RCLK1. Assume that Path 1 is the MIN path and has the SerDes pair with the minimum delay and that Path 2 is the MAX path; its SerDes pair has the maximum delay. This means that RCLK2 and Rdata2 will trail RCLK1 by Δφ. The setup time for Rdata2 will be degraded by as much as Δφ. See Figure 2.

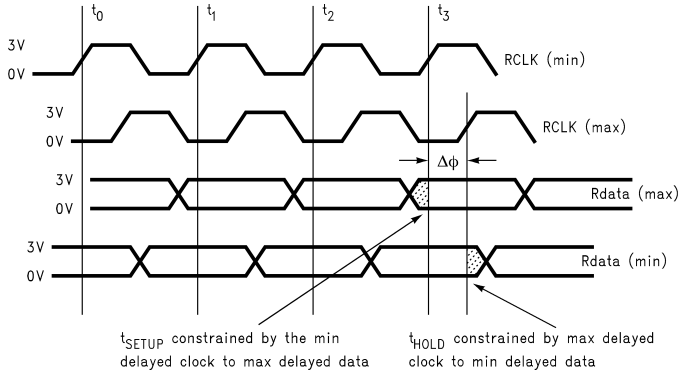

Figure 2. RCLK and Rdata Timing

The assumption that Path 1 is the MIN path and Path 2 is the MAX path could be wrong however. In fact, it could be that Path 1 is the MAX Path and Path 2 is the MIN path in which case RCLK1 will trail RCLK2 by Δφ. Now it is the hold time for Rdata2 that could be degraded by as much as Δφ. *(*Figure 2*).*

To be sure that either case is accounted for, both conditions must be considered. See Figure 2. If the MAX path is chosen as the reference then the clock and data from the MIN path will lead the clock and data from the MAX path by Δφ. The hold parameter of the MIN path data will be degraded by Δφ ns.

$t_{ROH'} = t_{ROH} - \Delta\varphi$

Conversely, if the MIN path clock is chosen as the reference, then the MAX path clock and data will trail the clock and data from the MIN path by Δφ. The setup parameter of the MAX path data will be degraded by Δφ ns.

$t_{ROS'} = t_{ROS} + \Delta\varphi$

NOTE: Since t_{ROS} is the data valid time before the reference clock it is specified as a negative number. Therefore Δφ is added to t_{ROS}.

Since the setup and hold parameters are specified in relation to the recovered clock period, it is convenient to use only the delay portion of the Serializer Delay and Deserializer Delay parameters. Both t_{SD} and t_{DD} are specified as a fractional number of clock cycles (xt_{CP} and yt_{CP}) plus a delay value (t_S and t_D).

$t_{SDmin} = xt_{CP} + t_{Smin}$, $t_{SDmax} = xt_{CP} + t_{Smax}$

$t_{DDmin} = yt_{CP} + t_{Dmin}$, $t_{DDmax} = yt_{CP} + t_{Dmax}$

So

$\Delta\varphi = [(xt_{CP} + t_{Smax}) + (yt_{CP} + t_{Dmax})] - [(xt_{CP} + t_{Smin}) + yt_{CP} + t_{Dmin})]$

Since the fractional clock cycle portion of the specs are proportional to the operating frequency they will be the same for all devices of that type regardless of the operating frequency. This means that part of the parameter value can be eliminated from the skew calculation. Rewriting the equation for the overall phase difference and substituting for E and F, we can see that the overall difference in phase will be due to the difference in delays through the serializers plus the difference in delays through the deserializers.

$\Delta\varphi = (E_1 + F_1) - (E_2 + F_2)$

$\Delta\varphi = (E_1 - E_2) + (F_1 - F_2)$

$\Delta\varphi = (t_{SD1} - t_{SD2}) + (t_{DD1} - t_{DD2})$

$\Delta\varphi = (t_{SDmax} - t_{SDmin}) + (t_{DDmax} - t_{DDmin})$

$\Delta\varphi = [(xt_{CP} + t_{Smax}) - [(xt_{CP} + t_{Smin})] + [(yt_{CP} + t_{Dmin}) - (yt_{CP} + t_{Dmin})]$

Since $xt_{CP1} = xt_{CP2}$ and $yt_{CP1} = yt_{CP2}$

$\Delta\varphi = (t_{Smax} - t_{Smin}) + (t_{Dmax} - t_{Dmin})$

So the maximum timing inpact on any number of serial paths can be calculated as follows:

$t_{ROH'} = t_{ROH} - \Delta\varphi = t_{ROH} - [(t_{Smax} - t_{Smin}) + (t_{Dmax} - t_{Dmin})]$

and

$t_{ROS'} = t_{ROS} + \Delta\varphi = t_{ROS} + [(t_{Smax} - t_{Smin}) + (t_{Dmax} - t_{Dmin})]$

Table 1 summarizes the setup and hold time calculations for the 10-bit SerDes products at various frequencies.

Table 1. Maximum Phase Difference and the Impact on Deserializer Output Timing[(1)]

Serializers	t_{SD} Range t_{SMIN}/t_{SMAX}	Deserializers	t_{DD} Range t_{DMIN}/t_{DMAX}	Δφ	16 MHz 62.5 ns	30 MHz 33.33 ns	40 MHz 25 ns	66 MHz 15.15 ns
DS92LV1021	0/5	DS92LV1212A	1.25/6.25	10	15	2.12	0.0	N/A
DS92LV1023	1/3	DS92LV1224	1.25/6.25	7	N/A	5.12	3.0	−1.24
	1/3		2.25/5.25	5	N/A	7.12	5.0	N/A
	1/3		2.75/4.75	4	N/A	N/A	N/A	1.76

(1) Within temperature specification for t_{SD} and t_{DD}. Much of the variation in deserializer delay is due to variation over temperature. The basic t_{DD} specification captures the entire range of variation. In application it is more likely that deserializers used in parallel will be located close together and therefore subject to the same temperature. The Within Temperature specification can be used under such conditions.

Example: Using the DS92LV1023 and DS92LV1224 SerDes chipsets in parallel with a 40 MHz clock.

To calculate the maximum phase difference (Δφ) between two '1023/'1224 serial links refer to the datasheet parameters t_{SD}, t_{DD}, t_{ROS}, t_{ROH}, and t_{RCP}.

$t_{SDMIN} = t_{TCP} + 1$ ns

$t_{SDMAX} = t_{TCP} + 3$ ns

$t_{DDMIN} = 1.75 * t_{RCP} + 1.25$ ns

$t_{DDMAX} = 1.75 * t_{RCP} + 6.25$ ns

$t_{RCP} = 1/40$ MHz = 25 ns

t_{ROS} = −0.4 * t_{RCP} = −0.4 * 25 ns = −10 ns

t_{ROH} = 0.4 * t_{RCP} = 0.4 * 25 ns = 10 ns

Plug the values into the equations for $t_{ROS'}$ and $t_{ROH'}$.

$\Delta\varphi = (t_{Smax} - t_{Smin}) + (t_{Dmax} - t_{Dmin})$

= (3 – 1) + (6.25 – 1.25) = 7 ns

$t_{ROH'} = t_{ROH} - \Delta\varphi$ = 10 – 7 = 3 ns

$t_{ROS'} = t_{ROS} + \Delta\varphi$ = (−10) + 7 = −3 ns

Therefore if the Client Receive ASIC supports a input set/hold of −3/+3 ns, then the timing is validated.

If the assumption that the SerDes pairs will all be at the same temperature is valid, then the Within Temperature specifications can be used to get wider setup and hold numbers.

$t_{SDMIN} = t_{TCP}$ + 1 ns

$t_{SDMAX} = t_{TCP}$ + 3 ns

t_{DDMIN} = 1.75 * t_{TCP} + 2.25 ns

t_{DDMAX} = 1.75 * t_{TCP} + 5.25 ns

$\Delta\varphi = (t_{Smax} - t_{Smin}) + (t_{Dmax} - t_{Dmin})$

= (3 – 1) + (5.25 – 2.25) = 5 ns

$t_{ROH'} = t_{ROH} - \Delta\varphi$ = 10 – 5 = 5 ns

$t_{ROS'} = t_{ROS} + \Delta\varphi$ = (−10) + 5 = −5 ns

Therefore if the client receive device supports a input set/hold of −5/+5 ns, then the timing is validated.

3 CONCLUSION

For any parallel arrangement of BLVDS SerDes pairs (where the flight times throughout the path have been controlled) the maximum phase difference between any deserializer output to another deserializer output will occur when the serializer and deserializer in one path both have a minimum delay while the serializer and deserializer in the other path both have the maximum delay. The parameters t_{SD} and t_{DD} specify the minimum and maximum delays for BLVDS SerDes devices. Some of the delay variation can be eliminated by using the Within Temperature specifications. Parallel arrangements are feasible and greatly depend upon the clock rate and the required set/hold time at the client receive device. In practice clock rates up to 50–60 MHz may be supported depending upon the system timing.

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