Low-Voltage Differential Signaling Yields Megatransfers per Second with Milliwatts of Power

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Low-Voltage Differential Signaling Yields Megatransfers per Second with Milliwatts of Power

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Today's high-speed data-transfer applications need hundreds of megatransfers per second, yet must consume only milliwatts of power. Older signal standards can achieve either—but not both—of these goals. New standards for low-voltage differential signaling let you overcome this roadblock.

Two new standards fill the need for a general-purpose, high-bandwidth interface standard for serial and parallel data requiring "megatransfers"—hundreds of millions of bits, bytes, or words per second. The standards are the Telecommunications Industry Association's (TIA's) TIA/EIA-644, Electrical Characteristics of Low Voltage Differential Signaling (LVDS) (Reference 1), and the IEEE's 1596.3-1996 LVDS for the Scalable Coherent Interface (SCI) (Reference 2). Both standards enable low-cost, standard-process ICs to communicate at gigabytes per second.

The standards are compatible, differing only in the intended use of the interface. The IEEE created the SCI standard for low-cost, low-power communication between SCI nodes at 500M transfers/sec. The TIA standard provides a general-purpose, application-independent interface for signaling rates as high as 655M transfers/sec.

Two innovative features of the TIA interface provide flexibility in its applications such as telecommunications, digital video, and multimedia. First, the standard's driver and receiver operate at a relatively low power, which allows integration of transceivers directly onto VLSI parts. Thus, you can use one chip to comprise the total data-transfer interface, or you can implement a discrete transceiver, which may be the more economical approach. The second innovative feature of the TIA interface is its low swing voltage, which lets your implementation achieve high speeds while using little power.

This technology enables low-cost parts for high-speed data transfers. These data streams can bypass the system bus by using a point-to-point architecture rather than the traditional multidrop-bus approach, which causes a bottleneck. Multidrop buses have inherent bandwidth limitations, such as reflections, slow signal flight due to capacitive loading, and stubs on transmission lines. These limitations limit the buses' practical switching frequencies to about 66 MHz. Wide buses can increase throughput but incur skew on parallel channels and require more board real estate. Further point-to-point standards developments and experience in implementing the SCI may eventually enable it to replace the multidrop buses in applications requiring high bandwidth.

LOW SWING VOLTAGE IS KEY

LVDS differs from previous signaling standards in that its developers' primary goal was high speed, and they incorporated a constant-current LVDS driver to help achieve that goal. The constant current allows power consumption to be relatively independent of frequency. Another speed-enhancing feature is the LVDS' ability to operate independently from the power-supply voltage, because the standard's interface voltage is low enough to operate from a 2V power supply. This situation means that future low-voltage parts will interoperate with current 5V parts. Also speeding performance are the standard's low-voltage swing and differential signals, which provide electromagnetic-compatibility (EMC) features that reduce high-speed signaling-system side effects.

Two single-ended signals create the differential signal's V_{OD} *(Figure 1)*. V_{OA} is the "true" signal, and V_{OB} is the "complement". You derive V_{OD} by subtracting the complement from the true signal, and receiver thresholds, V_{TH}s, are relevant only with respect to the differential signal. The LVDS receiver is concerned only about the difference between the true and complement signals.

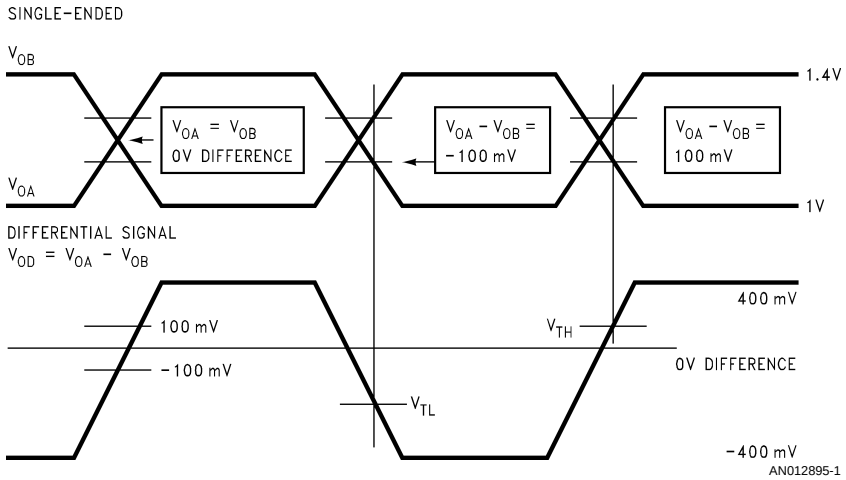

FIGURE 1. Differential Signaling has V_{OA} as the True and V_{OB} as the Complement Signal.

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Low swing is important for high-speed switching. The signals change a maximum of 400 mV and a minimum of 250 mV, centered at 1.2V with respect to the driver ground. The less a voltage level must change, the faster it can unambiguously achieve the desired state. LVDS typically switches only 325 mV on each single-ended line.

HOW FAST IS LVDS?

Transferring data involves more than just switching transceivers. You measure data transfer by bandwidth, and the effective data-transfer rate depends on protocol and system specifications, as well as on switching frequency. Consider a system that requires 1-Gbyte/sec bandwidth and a 2-byte-wide data-transfer interconnection. These requirements mean that the desired bit rate is 500 Mbps on each of the data lines. This situation provides a 2 ns bit width that must include signal-transition time, time for skew between parallel channels, and an interval at the stable voltage level for receiver setup-and-hold conditions.

To understand the capability and feasibility of high-speed switching, consider a scenario in which you allow 25% of the bit interval for transitions, leaving 500 ps for the voltage to change a maximum of 400 mV *(Figure 2)*. By designing for a 400 ps transition, you can achieve a slew rate (10% to 90% of 400 mV) of 0.8V/ns. This slew rate is too slow to cause EMI crosstalk. The low-swing voltage levels allow you to attain this slew rate in high-speed switching.

In this example, the skew between signal lines takes up about 35%, or 700 ps, of the bit width. Skew is the largest correctable factor inhibiting data-transmission speed within a system, and it can occur at many points in the data-transmission path. Skew first occurs in the signal path in the difference between driver circuit delays for each signal line. Packaging for both driver and receiver circuits, circuit-board traces, cables, connectors, and receiver-circuit delays also can cause skew.

LVDS standards are flexible enough to allow you to reduce skew and increase bandwidth. The IEEE standard makers assumed that automatic deskew circuits on the receiver would compensate for all the inequities in delays between channels up to the receiver. These circuits alone could increase the bit rate per channel by as much as 30%, leaving 40%, or 800 ps, of the bit width for the receiver to capture the data. Latches fabricated in submicron CMOS processes can operate at this speed. In this example, divide 800 ps between the setup-and-hold times the receiver circuit needs to latch the data.

LVDS ALSO SAVES POWER

The standards group set the driver-output offset for the differential signal at 1.2V; thus, power supplies can also be low-voltage. The group determined that this voltage level would suit CMOS designs and would not inhibit designs in other processes, including bipolar, BiCMOS, or GaAs. You can establish a symmetrical operating region between power rails as low as 2.4V. Use circuit-design techniques similar to those that EIA RS-485 uses to enable receivers to operate with an input voltage outside the power rails. Your design can then operate from a 2V power supply and still maintain a large receiver-input operating range.

The lower current and voltage levels for LVDS also result in lower on-chip power dissipation. The maximum constant driver-output current of 4 mA at an offset of 1.2V yields reduced power dissipation at the driver. Because the 4 mA then passes through a termination resistor at the receiver to give the differential voltage, the power dissipated at the terminating resistor is 1.6 mW or less.

The standard's constant-current driver requirement severs the connection between the power usage and the operating frequency. Voltage-mode interfaces that are implemented in CMOS have the undesirable feature, which the I_{CC}-vs-frequency curve illustrates, of suddenly increasing. Because the LVDS driver-output current remains constant, the driver-circuit design achieves a stable output current independent of the operating frequency. Driver power consumption remains almost constant as operating frequency increases.

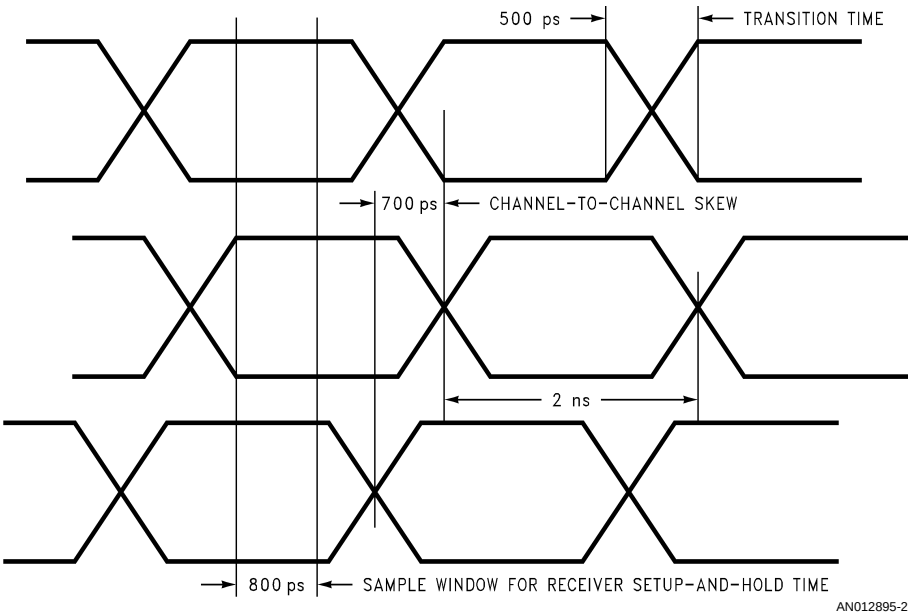


FIGURE 2. Three Parallel Differential Signals Show Allocation of Bit Width to Physical Signal Transition, Skew, and Receiver-Sample Parameters.

DIFFERENTIAL SIGNALS MAKE A DIFFERENCE

Differential signals, famous for their noise immunity, control the inevitable voltage uncertainty in many systems. Noise margin is a big concern, because noise on power supplies in high-clock-rate, dense-component, digital systems can be greater than 250 mV_{PP}, even if you use good decoupling techniques. Therefore, you must account for the impact of noise, typically by analyzing noise margins.

The minimum 250 mV differential signal and the apparent lack of noise margin alarm some designers. However, you needn't worry. Divide the noise in a system into common-mode and single-ended noise. Further divide common-mode noise into noise on the power supply, which every component in the system sees, and EMI.

Properly routed single-ended signals for differential performance having parallel, equal-length traces incur little EMI noise, because it interferes with all signals that are referenced to a given voltage that is supposedly stable. This "stable" voltage moves with power-supply and EM-induced variations. With differential signals, the true and the complement signals move with these variations. The noise is seen as common not as a differential signal. A properly designed system's differential signal is immune to power-supply and EMI noise. Proper design means that each single-ended signal must simultaneously encounter the same common-mode voltages.

You usually think of noise-margin analysis in terms of single-ended signals, in which you define the noise-margin high (NMH) as the difference between the minimum driver high-output voltage, $V_{OH(MIN)}$, and the maximum receiver-sensitivity input-high voltage, $V_{IH(MAX)}$, as follows *(Figure 3)*:

$$NMH = V_{OH(MIN)} - V_{IH(MAX)} \quad (1)$$

The maximum driver-output low and the minimum receiver-input high threshold define the NML:

$$NML = V_{IL(MIN)} - V_{OL(MAX)} \quad (2)$$

With differential signals, you do not define noise margin with respect to the true and complement single-ended signals. *Equations (1), (2)*, therefore, use the terms in *Figure 4* to arrive at the noise margin — 150 mV when you calculate it in the same way as the single-ended signal. However, because the differential signal is immune to the common-mode noise, the only noise source is the single-ended noise. Single-ended noise comes from transmission-line phenomena, such as reflections and crosstalk. You can control these phenomena using proper transmission-line design (see Appendix, Deal with Transmission-Line Noise).

Designers often worry that using differential signals can double the pin count. Conventional wisdom says that pins are expensive due to package size, manufacturing, and reliability. However, because the LVDS provides higher frequency, the datapath can be narrower and still achieve the same bandwidth, meaning that you can use fewer pins overall. National Semiconductor's Flat-Panel Display Link (FPD-Link) devices let you narrow a 28-bit, single-ended parallel bus to five differential pairs on the data-transfer path. Both ports to the chip handle the same bandwidth. This fact means that the 28-signal-pin TTL bus achieves the same bandwidth as the 10-pin LVDS port. Bus width reductions of greater than 50% are possible even with the addition of a couple of signal common references on the data-transfer path. This saves cable and connector cost, reduces the connecter physical sizes, and requires less EMI shielding for box-to-box connections (Reference 3).

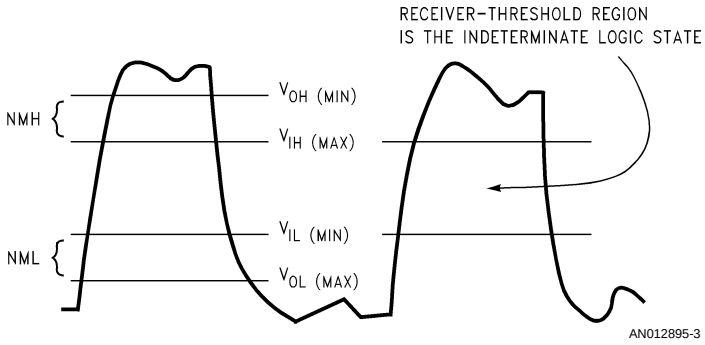
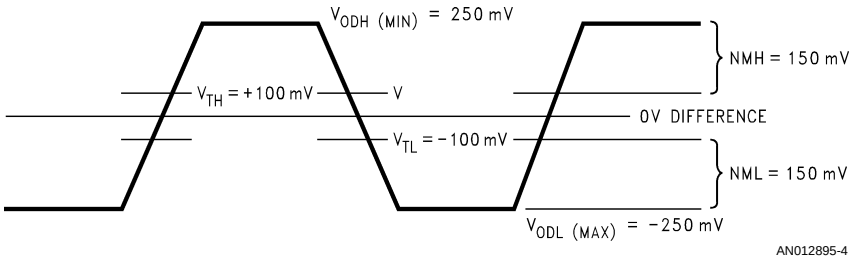


FIGURE 3. Noise Margin for Single-Ended Signals are Determined by the Receiver's Threshold



Notes:
Differential Noise-Margin High = 250 mV − (100 mV) = 150 mV.
Differential Noise-Margin Low = −100 mV − (−250 mV) = 150 mV.

FIGURE 4. You Determine Differential Noise Margins for LVDS with Respect to a Zero-Difference Reference Level.

Another factor about pin usage for high-frequency signaling is that, because the single-ended signals are always referenced to a common voltage between the driver and receiver, this common voltage must remain stable. Otherwise, noise margin can suffer. When the frequency becomes very high for a signal with large voltage swings and switching current, the noise, or ground bounce, also increases. Maintain the common voltage at a steady level to ensure adequate noise margin. The best way to achieve this goal is to use more ground pins per signal in the interconnect and package. This approach ensures that the switching currents have a low inductive return path. Such standards as Futurebus+ (IEEE 896.2) recommend a ratio of two signals per ground-bounce connection for single-ended signals switching at frequencies of 20 MHz to 40 MHz in a bused environment. Higher frequency signals require a 1-to-1 ratio. The disadvantage of having two pins per signal is still better than having twice as many pins.

System operating voltages are now often 3.3V and 2.5V and will eventually go as low as 2V. Any new signaling standard that wants to enjoy a long life should be able to operate from these voltages. The LVDS standard is independent of power-supply voltage as low as 2V, because the differential signals center at 1.2V.

You can use any of the copper transmission-media options as interconnects for LVDS, because neither standard specifies a transmission medium. Each application has its own set of requirements, and you must specify the media within those requirements. Consider distance, bit rate, protocol and coding schemes, mechanical specifications for connectors, and media and EMC when choosing the LVDS carrier.

The LVDS standard assumes the use of a 100Ω, differential-impedance transmission medium to transport the signal from the driver to the receiver. You must also place a 100Ω termination at the end of the transmission line to create a difference voltage to the constant current from the driver output. The TIA/EIA standard lets you use either an external package or integrated termination resistance. Because the IEEE targeted its standard at a specific application, it specifies only an integrated termination.

You should follow two general guidelines. First, the transmission path should have a controlled differential impedance of 100Ω, ±10%. Second, you must control skew.

You have some flexibility beyond the scope of the standard in implementing the interconnect and termination. Because the driver output is constant-current, you can sometimes use a higher value resistor for the termination. For instance, you could use 150Ω to terminate a 150Ω transmission line, which would result in the difference voltage being a maximum 600 mV rather than the 400 mV for a 100Ω termination. This approach would not yield as much of a low-swing-voltage signal, but it would provide more margin for signal attenuation and noise to meet a system-implementation requirement. To minimize reflections, you should select a termination impedance that matches the differential impedance of the media ($R_T = Z_{OD}$).

In skew control, you must match the electrical length of both signal paths within a differential pair and parallel datapaths. You must establish manufacturing tolerances for eliminating skew in cables. As these tolerances decrease, the cost of manufacturing usually increases. However, because this skew control becomes more critical as the signaling frequency increases, eliminating the interconnect skew is important in high-frequency-system design.

Certain types of media work best in specific applications. For interconnecting ICs on one pc board, you usually use microstrip and strip-line copper traces, through-hole vias, and chip-pin solder pads. These interconnections are usually less than 50 cm long.

A second application is connecting circuit boards within the same chassis or crate. In this case, you probably would use a board connector and unshielded cabling. The cabling could be anything from simple ribbon cable to impedance- controlled, high-frequency flex circuit. These connections can measure from a few centimeters for an adapter-card-to-adapter-card connection to 1m for a shelf-to-shelf connection.

You can also use connectors and shielded cables to connect circuit boards in different chassis. Such interconnections range from 30 cm to hundreds of meters long. For practical purposes, copper interconnects for LVDS at frequencies higher than 100 MHz probably cannot exceed 50m. The shielded cables can be inexpensive twisted-pair, parallel-pair or high-tech coaxial cable using the latest in high performance dielectrics. The variety of options for carrying LVDS signals can be confusing, but your clear understanding of some trade-offs will ease your decisions.

For transmission of LVDS signals over any type of copper interconnect, consider the DC and AC characteristics and the length of the interconnect. With low-frequency transmissions, DC characteristics and IR drop are key factors. You calculate how far the signal can travel before the voltage drop due to resistance per unit length attenuates the signal so much that the signal has no margin.

However, the length-limiting factor at high frequency is the AC performance of a cable. How much does the cable's length slow signal transitions? The answer lies in the capacitance per unit length of the cable. The cable acts as a low-pass filter. As the signal propagates, it filters out high-frequency components in the transitioning edges. Therefore, the transition stretches as the signal travels through more and more cable. A transition that takes more than 50% of the bit period causes clipping of the signal amplitude.

The lowpass-filter cable effect depends on the cable's dielectric quality and construction. The combination of impedance, skin effect, dielectrics, and shielding of the filter can attenuate the LVDS. By carefully trading off these parameters, cable manufacturers can construct high-performance, though expensive, cables. Several cable manufacturers have been working with LVDS to see how their cables and connectors perform *(Figure 5)*. For example, you can use inexpensive unshielded twisted pair (UTP) Category 3 cable at low frequency and short distance. You need carefully constructed premium cable at higher frequencies and longer distances.

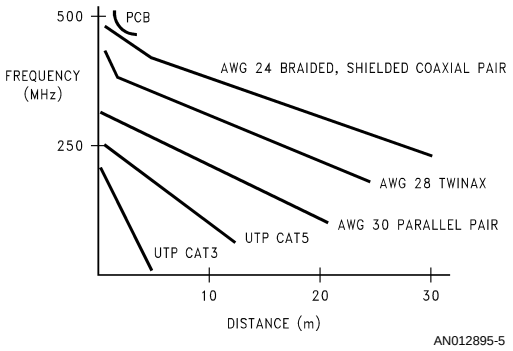


FIGURE 5. You Can Use Inexpensive Unshielded Twisted-Pair (UTP) Category 3 Cable at Low Frequency and Short Distance. You Need Carefully Constructed Premium Cable at Higher Frequencies and Longer Distances.

High-frequency LVDS inhibits generation of electromagnetic fields by reducing the voltage swing and limiting transition times. These electromagnetic fields are the same as those that cause the results in *Equations (3), (4)* (see Appendix, Deal with Transmission-Line Noise). However, LVDS does not eliminate the problem. The switching signals and, therefore, interference still produce fields. LVDS reduces but does not eliminate EMI. You must specify cable shielding to control the EMI outside the box.

You can control EMI using board layout, shielding, and proper grounding techniques. Differential-signal pairs are close to each other, so that the equal and opposite transitions on each line create equal and opposite electromagnetic fields, which cancel each other out. Shielding in the cable is the best way for you to control EMI, once the signal leaves the Faraday shield that a good chassis provides.

Grounding reduces ground-loop area, because propagating signal currents create equal and opposing return currents in whatever path is available *(Figure 6)*. You can minimize the fields this ground loop creates by ensuring that the return path is low-impedance and closely related to the signal path. Therefore, you should pay attention to the ground path for each signal pair. Each pair of premium cables, such as parallel-pair and twinaxial, has a “drain” wire. This wire provides the unambiguous ground-return path for each signal wire. Putting ground wires and pins into the connectors is another way to control the fields the signals generates.

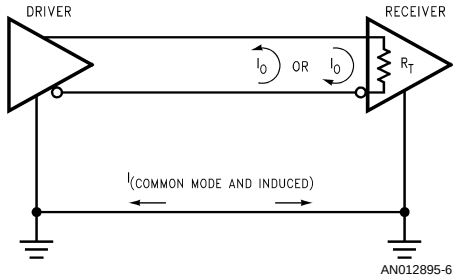


FIGURE 6. Good Ground Connections to Carry Common-Mode and Induced Currents are Critical to Final Performance.

APPENDIX

Deal with Transmission-Line Noise

Transmission lines use termination to absorb energy from propagating signals, thereby stopping the energy from reflecting off a discontinuity at the end of the terminated media. In the multidrop-bus environment, discontinuities exist at every drop line off the bus. Termination can lower reflections, or noise, but they are always on the line due to the mid drops. You can minimize reflections by using a point-to-point transmission path. Because no discontinuities exist on the path, you can perfectly match the transmission-path differential impedance with termination at the receiver input.

Electromagnetic-field energy originating from propagating signals causes crosstalk. Simplified equations provide an understanding of the signal characteristics critical to crosstalk. *Equation (3)* describes the backward-coupled voltage; *Equation (4)*, the forward-coupled voltage to the signal path that the field is influencing.

$$V_{bkwd} = (V_A/T_R)\ (½\ t_L)\ (C_C\ Z + L_C/Z) \qquad (3)$$

and

$$V_{frwd} = (V_A/T_R)\ (½)\ (C_C\ Z - L_C/Z) \qquad (4)$$

where V_A is the aggressor-signal amplitude, T_R is the aggressor-signal transition time, L is the line length, T_L is the line delay, Z is the line impedance, C_C is the capacitive coupling, and L_C is the inductive coupling.

Both types of crosstalk are directly proportional to the amplitude and inversely proportional to the transition times of the aggressor signal. The capacitive and inductive coupling affect both types of crosstalk. In backward crosstalk, the aggressor amplitude adds the two types of coupling and then multiplies them to give a same-polarity pulse to the victim. In forward crosstalk, the aggressor amplitude multiplies $C_C\ Z - L_C/Z$ to give a pulse of either polarity, depending on the relative size of the coupled reactance.

This calculation shows that aggressor amplitude and transition times are dominant factors in causing crosstalk. The LVDS standard minimizes the signal amplitude and controls the transition times to reduce single-ended noise due to crosstalk.

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