SD395EVK
LMH0395 Evaluation Board User Guide

National Semiconductor
EVK User Manual

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Overview

The SD395 Evaluation Kit (EVK) enables evaluation of the LMH0395 3G/HD/SD SDI Dual Output Adaptive Cable Equalizer.

Evaluation Kit Contents

The EVK contains the following parts:

- SD395EVK board assembly with the LMH0395 cable equalizer
- SD395EVK User Guide

Evaluation Board Description

Figure 1 shows the SD395 evaluation board and highlights some of its features.

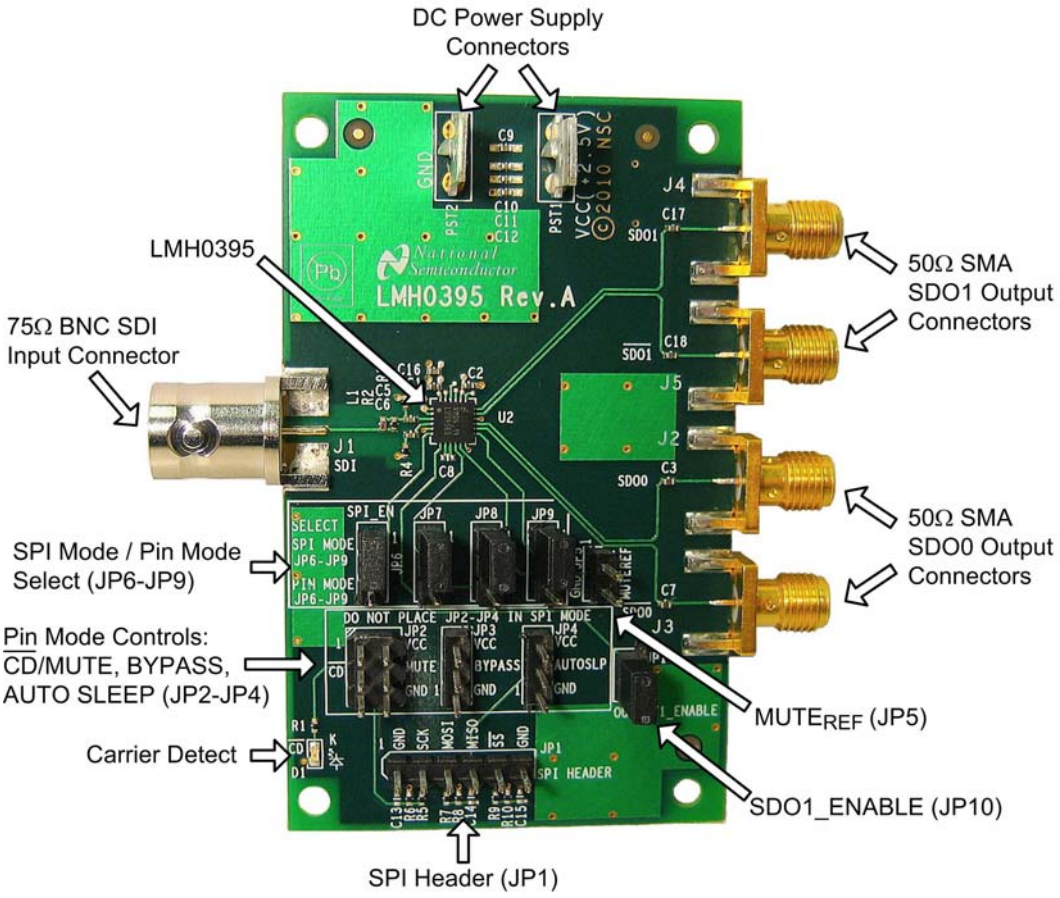

FIGURE 1. SD395 Evaluation Board

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SDI Input and SDO Output

The SDI input connector (J1) is a 75Ω BNC connector. The SDI input should conform to the SMPTE 424M, SMPTE 292M, or SMPTE 259M standards.

The SDO0 and SDO1 output connectors (J2, J3, J4, and J5) are 50Ω SMA connectors. The SDO0 and SDO1 output connectors have onboard 4.7uF AC coupling capacitors (C3, C7, C17, and C18). When using only one side of an output pair, the other side should be terminated with a 50Ω SMA termination. For example, when only using the SDO0 output, $\overline{SDO0}$ should be terminated with a 50Ω SMA termination.

DC Power Connectors

The VCC and GND power connectors, PS1 and PS2 respectively, should be powered with a DC input voltage of 2.5V ± 5%.

SPI Mode / Pin Mode Select (JP6 – JP9)

JP6, JP7, JP8, and JP9 are used to select between SPI Mode or Pin Mode. To select Pin Mode, set these jumpers in the down position as shown in Figure 2. To select SPI Mode, set these jumpers in the up position as shown in Figure 3. For proper operation, either Pin Mode or SPI Mode must be selected. **Do not leave JP6-JP9 open.**

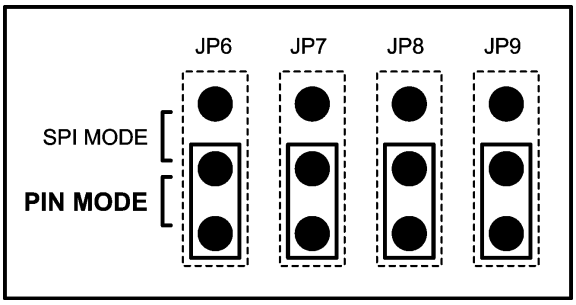

FIGURE 2. Pin Mode Select

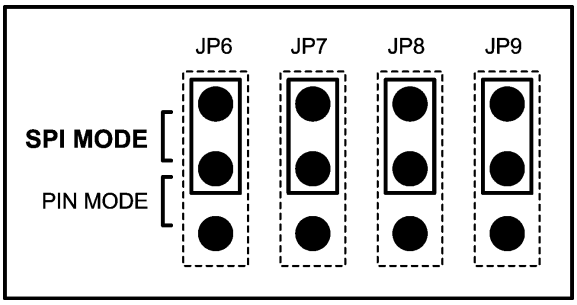

FIGURE 3. SPI Mode Select

$MUTE_{REF}$ (JP5)

JP5 allows control of the $MUTE_{REF}$ function and may be used in either Pin Mode or SPI Mode. $MUTE_{REF}$ is an input voltage used to set the threshold for $\overline{CD}$. The $MUTE_{REF}$ DC input voltage should be between 0V and 2.5V. Refer to the LMH0395 datasheet for details. Leave JP5 unconnected for normal operation.

SDO1_ENABLE (JP10)

JP10 allows control of the SDO1_DISABLE function and may be used in either Pin Mode or SPI Mode. When this jumper is set, the SDO1 output is enabled. When this jumper is removed, the SDO1 output is disabled (high impedance).

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Pin Mode Controls (JP2 – JP4)

JP2, JP3, and JP4 are used to control the $\overline{CD}$ and Mute, Bypass, and Auto Sleep functions while the device is configured in Pin Mode. **Do not place jumpers on JP2, JP3, or JP4 while the device is configured for SPI Mode.**

$\overline{CD}$ and MUTE (JP2)

JP2 allows Carrier Detect ($\overline{CD}$) monitoring and MUTE control. $\overline{CD}$ is high when no input signal is present. MUTE may be used to force the outputs on or off, or tied to $\overline{CD}$ to allow automatic mute operation if the SDI signal is not present. To activate mute and force the outputs into a muted condition, set the jumper to pull MUTE to VCC. To turn off mute so that the outputs will never mute, set the jumper to tie MUTE to GND. For normal operation, set the jumper to tie $\overline{CD}$ to MUTE for automatic mute control. The MUTE pin has an internal pulldown (to disable mute), so JP2 may be left unconnected and the device will never mute.

BYPASS (JP3)

JP3 allows control of the equalization BYPASS function. To put the device into bypass mode, set the jumper to pull BYPASS to VCC. To turn off bypass (for normal operation) set the jumper to pull BYPASS to GND. The BYPASS pin has an internal pulldown (to disable bypass), so JP2 may be left unconnected for normal operation.

AUTO SLEEP (JP4)

JP4 allows control of the AUTO SLEEP function. To put the device into auto sleep mode in which it will power down when no input is detected, set the jumper to pull AUTO SLEEP to VCC. To turn off auto sleep and prevent the LMH0395 from automatically powering down, set the jumper to pull AUTO SLEEP to GND. The AUTO SLEEP pin has an internal pullup (to enable auto sleep), so JP4 may be left unconnected to enable auto sleep mode.

SPI Header (JP1)

JP1 is the SPI (Serial Peripheral Interface) header. It allows access to the SPI pins ($\overline{SS}$, MISO, MOSI, and SCK) while the LMH0395 is in SPI mode. These pins may be connected to a standard SPI controller to access the LMH0395 SPI registers. Refer to the LMH0395 datasheet for details.

Carrier Detect LED (D1)

D1 shows the status of Carrier Detect. This LED is GREEN when an input signal has been detected, and OFF when no input is detected. D1 shows the status of Carrier Detect while in Pin Mode or SPI Mode.

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Typical Performance

Equalizer Output

Figures 4, 5, and 6 show output waveforms for the SD395 with various Belden 1694A cable lengths. The input signal is a 2.97 Gbps PRBS10, and the output signal is measured on the Agilent DCA-J 86100C oscilloscope.

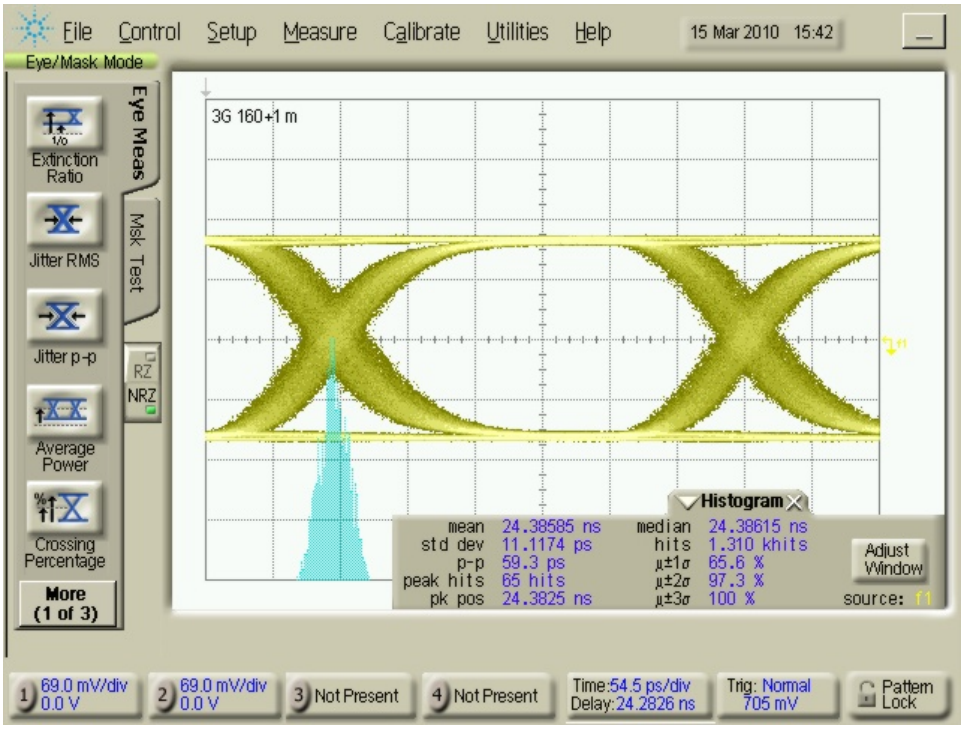

FIGURE 4. SD395 Output Waveform at 2.97 Gbps with 160m Belden 1694A Cable

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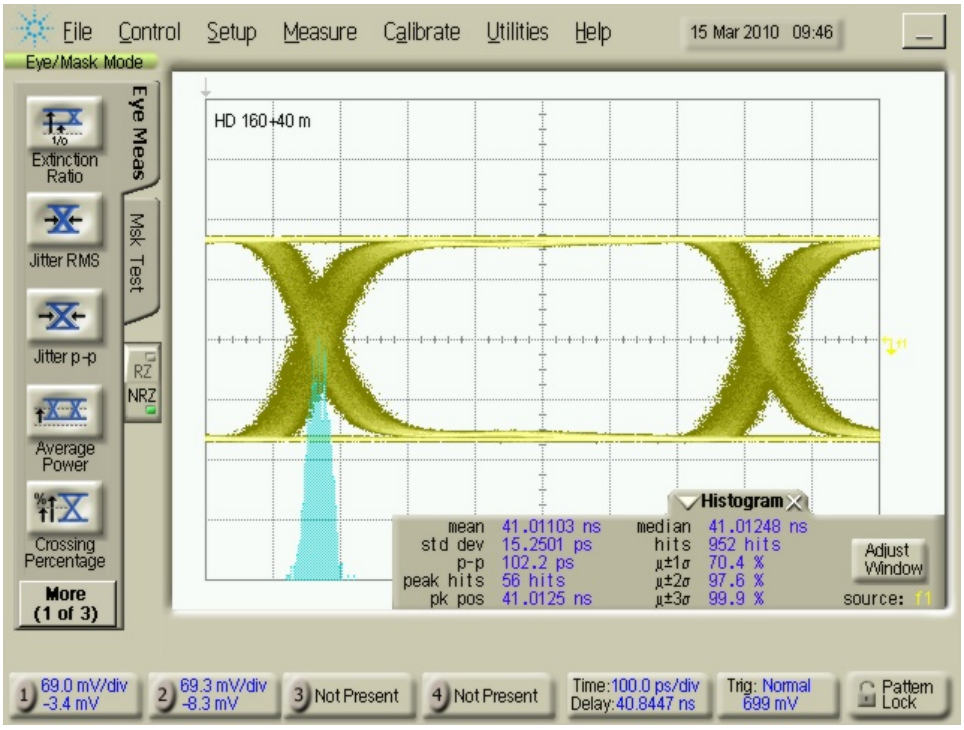

FIGURE 5. SD395 Output Waveform at 1.485 Gbps with 200m Belden 1694A Cable

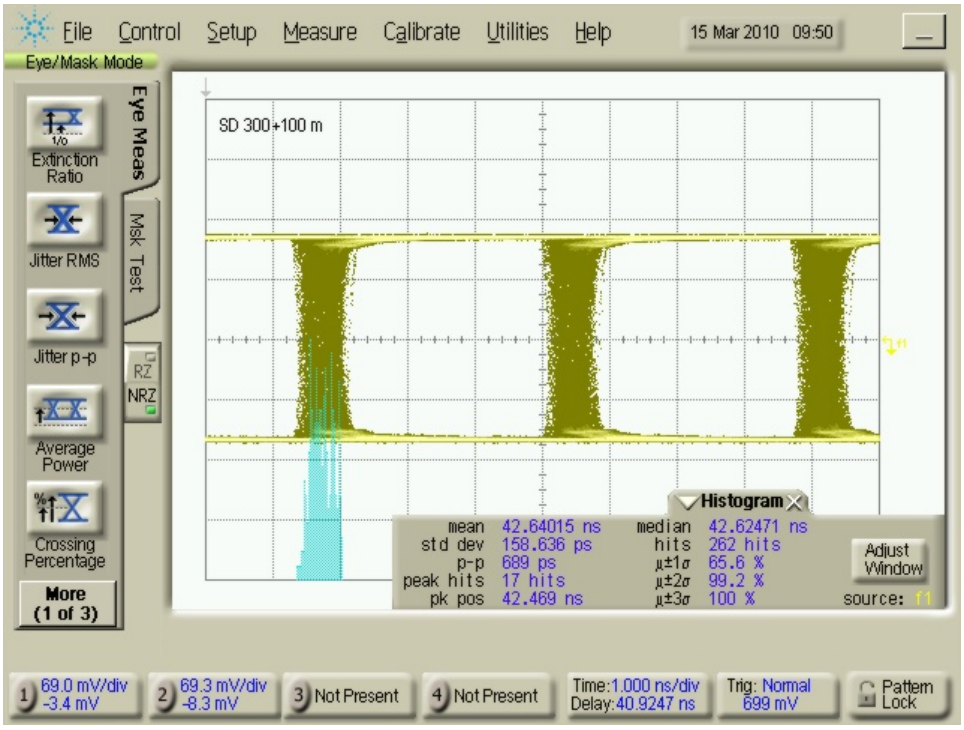

FIGURE 6. SD395 Output Waveform at 270 Mbps with 400m Belden 1694A Cable

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Input Return Loss

Figure 7 shows input return loss of the LMH0395 as measured at the BNC on the SD395. The return loss is measured using the Agilent 8722ES VNA with a 75Ω BNC to 75Ω Type N connector on the input. Note that return loss is layout dependent.

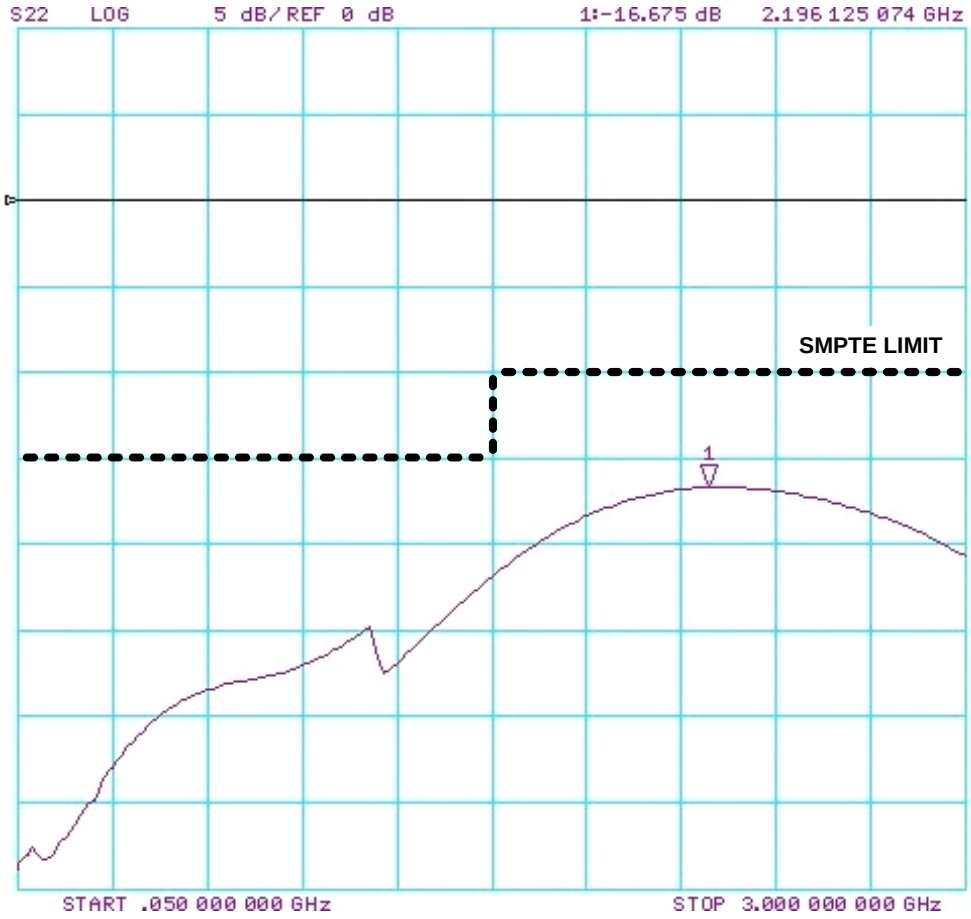

FIGURE 7. SD395 Input Return Loss

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SD395 Bill of Materials

Reference Designator	Qty	Description	Manufacturer	Manufacturer Part No.
C1, C2, C12	3	Capacitor, 0.01uF, 25V, X7R, 0402	Kemet	C0402C103J3RACTU
C3, C7, C9, C16, C17, C18	6	Capacitor, 4.7uF, 6.3V, X5R, 0402	Panasonic - ECG	ECJ-0EB0J475M
C5, C6	2	Capacitor, 1uF, 6.3V, X5R, 0402	Panasonic - ECG	ECJ-0EB0J105M
C10, C11	2	Capacitor, 0.1uF, 16V, X7R, 0402	Kemet	C0402C104K9RACTU
D1	1	LED, Green, 0603	Lite-On	LTST-C190GKT
J1	1	BNC, 75-ohm, Amphenol, edge launch	Amphenol	031-6009
J2, J3, J4, J5	4	SMA, 50-ohm, edge launch	Johnson Components	142-0701-851
JP1	1	Header, 6x1, 0.1"	3M/ESD	929647-01-06-I
JP2	1	Header, 3x2, 0.1"	3M/ESD	929665-01-03-I
JP3, JP4, JP6, JP7, JP8, JP9	6	Header, 3x1, 0.1"	3M/ESD	929647-01-36-I
JP5, JP10	2	Header, 2x1, 0.1"	3M/ESD	929647-01-02-I
L1	1	Inductor, 5.6nH, 0402	Murata	LQP15MN5N6B02D
PST1, PST2	2	Power Supply Terminal	Keystone	1287-ST
R1	1	Resistor, 300-ohm, 1/10W, 5%, 0603	Panasonic - ECG	ERJ-3GEYJ301V
R2, R3	2	Resistor, 75-ohm, 1/16W, 1%, 0402	Yageo America	RC0402FR-0775RL
R4	1	Resistor, 37.4-ohm, 1/16W, 1%, 0402	Vishay/Dale	CRCW040237R4FKED
R5, R7, R9	3	Resistor, 3.16k-ohm, 1/10W, 1%, 0402	Panasonic - ECG	ERJ-2RKF3161X
R6, R8, R10	3	Resistor, 9.76k-ohm, 1/10W, 1%, 0402	Panasonic - ECG	ERJ-2RKF9761X
U2	1	LMH0395 Cable Equalizer, LLP-24	National Semiconductor	LMH0395SQ

Schematic (next page)

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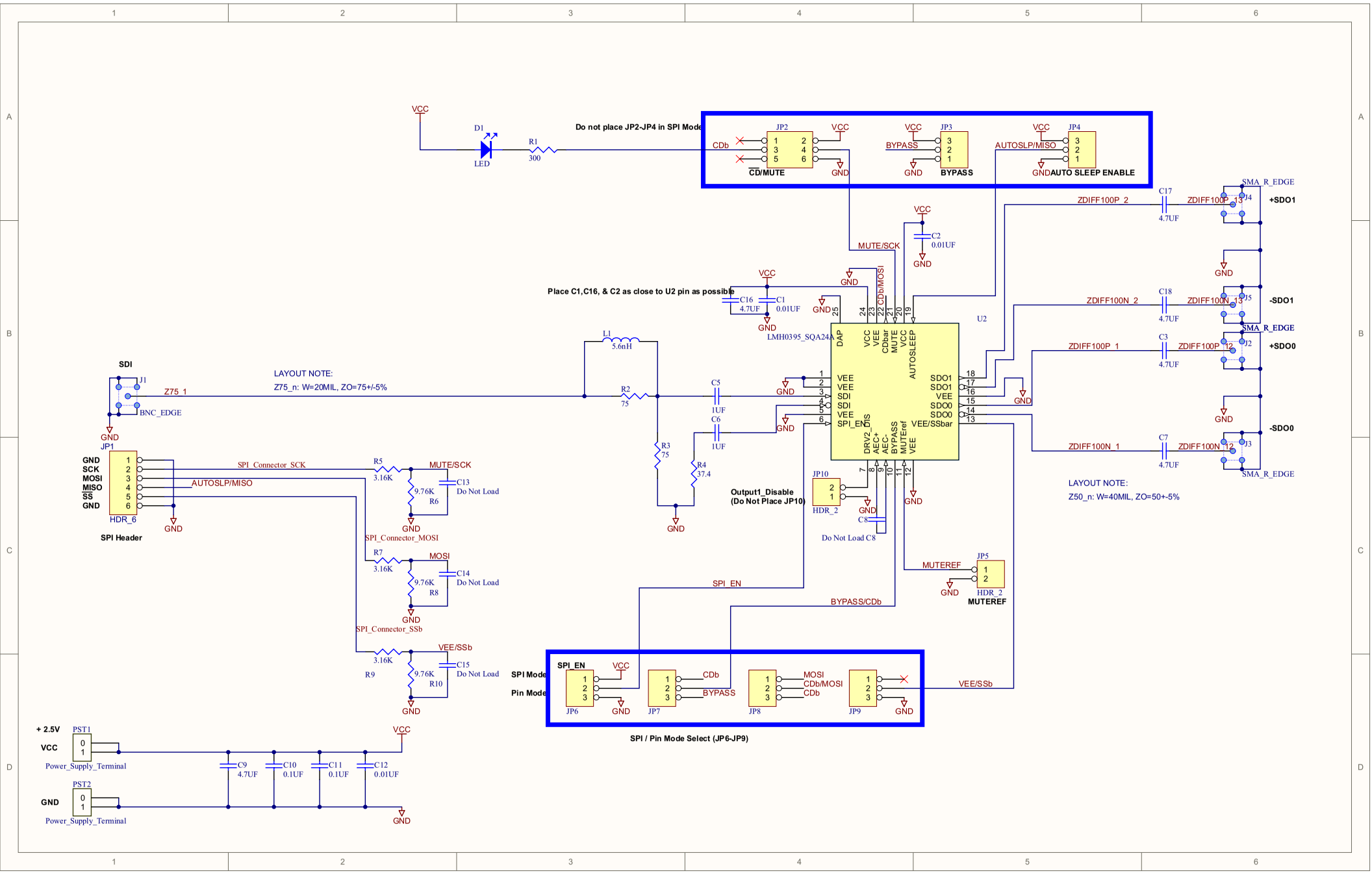
VCC
D1
LED
R1
300
Do not place JP2-JP4 in SPI Mode
JP2
CDb
CD/MUTE
GND
JP3
BYPASS
JP4
AUTOSLP/MISO
AUTO SLEEP ENABLE
C2
0.01UF
MUTE/SCK
Place C1,C16, & C2 as close to U2 pin as possible
C16
4.7UF
C1
0.01UF
LMH0395_SQA24A
U2
DAP
VCC
VEE
CDbar
MUTE
AUTOSLEEP
CDb/MOSI
SDO1
SDO0
VEE/SSbar
SPI_EN
DRV2_DIS
AEC+
AEC-
BYPASS
MUTEref
L1
5.6nH
R2
75
C5
1UF
C6
1UF
R3
75
R4
37.4
SDI
J1
BNC_EDGE
Z75_1
LAYOUT NOTE:
Z75_n: W=20MIL, ZO=75+/-5%
JP1
GND
SCK
MOSI
MISO
SS
HDR_6
SPI Header
SPI_Connector_SCK
AUTOSLP/MISO
R5
3.16K
MUTE/SCK
9.76K
R6
C13
Do Not Load
SPI_Connector_MOSI
R7
3.16K
MOSI
9.76K
R8
C14
Do Not Load
SPI_Connector_SSb
R9
3.16K
VEE/SSb
9.76K
R10
C15
Do Not Load
Output1_Disable
(Do Not Place JP10)
JP10
HDR_2
C8
Do Not Load C8
JP5
MUTEREF
HDR_2
SPI_EN
BYPASS/CDb
SPI Mode
Pin Mode
JP6
JP7
JP8
JP9
SPI / Pin Mode Select (JP6-JP9)
ZDIFF100P_2
ZDIFF100N_2
ZDIFF100P_1
ZDIFF100N_1
C17
C18
C3
C7
4.7UF
SMA_R_EDGE
J4
J5
J2
J3
+SDO1
-SDO1
+SDO0
-SDO0
LAYOUT NOTE:
Z50_n: W=40MIL, ZO=50+-5%
+ 2.5V
VCC
PST1
Power_Supply_Terminal
GND
PST2
C9
4.7UF
C10
0.1UF
C11
0.1UF
C12
0.01UF

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