Application Report
SNOA454–May 2004

AN-1311 MPL PHY Layer Overview

ABSTRACT

No existing interconnect standard meets the severe constraints for use within small handheld electronic devices. Existing interface technology such as LVDS, RSDS, and CMADS did save power, wiring and EMI in Notebook PCs a generation ago, but tomorrow's cellular handsets and PDA demand still lower power, lower number of wires and lower EMI. Mobile Pixel Link (MPL) provides an optimized interface between video ports on sources and targets. Its three main attributes are: Few wires (2 active lines), Low Power, and Very Low EMI.

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1 *Why MPL (Mobile Pixel Link)?*

No existing interconnect standard meets the severe constraints for use within small handheld electronic devices. Existing interface technology such as LVDS, RSDS, and CMADS did save power, wiring and EMI in Notebook PCs a generation ago, but tomorrow's cellular handsets and PDA demand still lower power, lower number of wires and lower EMI. Mobile Pixel Link (MPL) provides an optimized interface between video ports on sources and targets. Its three main attributes are: Few wires (2 active lines), Low Power, and Very Low EMI.

2 The MPL Link

To gain its system benefits of low power and low EMI, MPL uses small-magnitude current signaling transmission. The two logic states are determined by the magnitude of the current that is sourced from the receiver to the transmitter. The two currents can be thought of as an AC current riding on a DC bias current. Typically the two currents are 150 µA and 450 µA and considered to be ±150 µA riding on a constant 300 µA.

MPL defines the high current (i.e. 450 µA) as a Logic LOW and the low current (150 µA) as the Logic HIGH. The current is sunk by the driver and returned to the receiver via the MG (VSSA) pin. The MPL Ground should have a nearby, low impedance path back to its origination at the receiver. Also, by keeping the ground near by the signal line the resulting ring area is minimized and EMI is less due to the current-mode switching, low current magnitudes, and small ring area.

In comparison to other signaling standards, MPL switches current an order of magnitude less than LVDS (3.5 mA vs. 300 µA) and also has a voltage swing that is also smaller (20 mV vs. 350 mV). This lowers the power dissipation and also noise generation. When the link powers up, the Slave is initialized to the current magnitude that the driver is pulling. This optimizes signal quality and maximizes noise margins for the link in both directions.

MPL uses National's WhisperBus™ technology as a basis of its physical layer. Variations of WhisperBus technology have been employed in large format TFT-LCD displays for the same reasons it is being applied to the portable handheld applications. MPL adopts the basics of the WhisperBus PHY and adds a power saving (sleep) mode, bi-directional data transmission capability, and its own mobile optimized protocol (*currently in definition, CY2004*). A basic MPL link is shown in Figure 1. The Master resides next to the host (BBP, µP, or Imager) and the Slave resides next to the Display or target device.

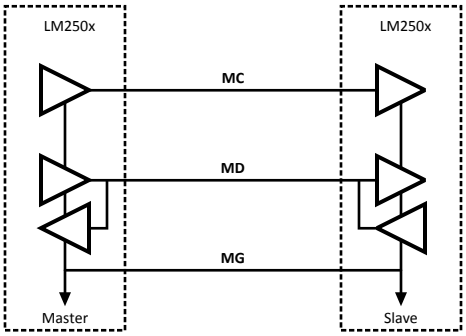

Figure 1. MPL Link Bus Configuration

3 The MPL Line Driver

The MPL Line Driver features a two-state current sink. The magnitude of the current is determined by the input state (LVCMOS). The Line Driver does not set the voltage on the line as this is set by the receiver on the link. The Line Driver is able to accommodate a wide range of receiver voltages. This allows for the Line Driver and Receiver devices to be powered from different supply rails if desired. The current sources in the receiver may also be turned off, reducing line current to zero and providing a very low power sleep or MPL off state. A simplified Line Driver is shown in Figure 2. When the DEnable* (internal signal) is LOW, the Idata switch is connect to the MPL signal line and a current of magnitude (Idata) is sunk by the driver. When the Din internal signal is Low the 2Idata is also switched in, thus 3xIdata is sunk by the driver. When the Din is High, the 2xIdata switch is open and the other state (Idata) is obtained. If both are open (DEnable* = High), the driver is off, and no current is sunk by the driver. Logically, MPL defines a Logic Low as the higher current magnitude (3 X Idata) and a Logic High as the lower current magnitude (1 X Idata). Idata may be set from 100 µA to 200 µA on the initial MPL Test device (LM2500 -test chip). The design of the driver is compatible with core rails that are extremely low down to a few hundred milliVolts. Also the return path for the current is directly via the MG (MPL Ground) pin. From a driver implementation, the MC (Clock) and the MD (Data) outputs are the same.

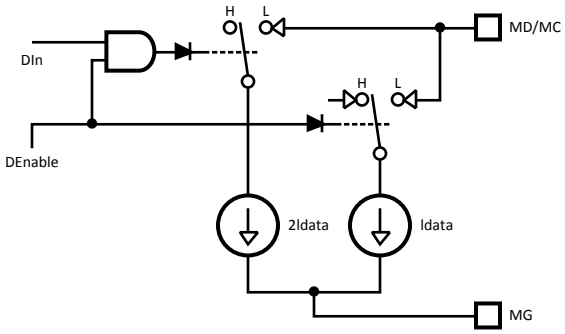

Figure 2. MPL Line Driver

4 The MPL Receiver

The MPL receiver detects the current state on the bus, converts it to a voltage, and amplifies that to standard logic levels and whether current is present or not. The receiver also provides line termination, eliminating the need of an external termination resistor simplifying system design and saving PCB real estate. A current sense circuit is also included in the receiver that informs a Slave device to power up or down when a signal is sensed. The Master device monitors the current flow in the MD line when the link is off as this indicates a service request from the Slave.

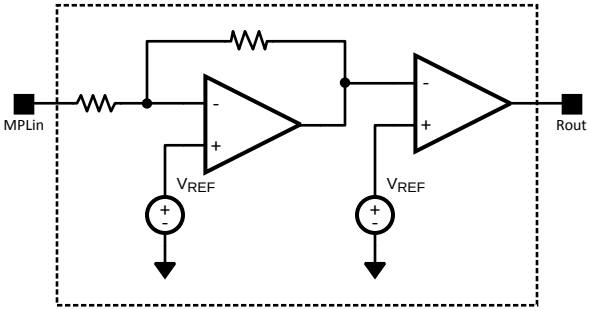

Figure 3. MPL Receiver

5 The MPL Transceiver

A transceiver may be constructed by combining a Line Driver and a Receiver circuit. For the Master device, the default for MD is a Line Driver and the Receiver block may be powered off to reduce current demand. During a Read_Data transaction, the Master's MD line driver may be switch off the bus or powered down during the reverse data flow of a Read transaction. For a Slave device the default for MD is a receiver with the MD line driver powered off (again for power saving reasons). When a Read_Command transaction is received, the TA′ (Turn Around) phase is long enough to allow the Slave's MD Line Driver to power up and its MD receiver may be switched off the line or powered off.

6 MPL Bus Configuration

The basic MPL link is comprised of two active signal lines and a signal ground return (MG). The clock (MC) is single direction and is always sourced by the Master device. The data signal (MD) is synchronous to the clock in the Master to Slave direction utilizing both clock edges. This aids in keeping clock rates lower for power, noise, and EMI reasons. The MD data signal is a half-duplex bi-directional line. To support a Data In (Read) transaction, the direction of the data signal may be turned around. In the normal configuration, Data Out (Write) the Master's MD Receiver and the Slave's MD Line Driver are powered off to conserve power. Time is provided in the Turn Around (TA) periods to power them up and down when they are required.

MPL acknowledges that the video paths are unique and generally point-to-point in today's systems. Being point-to-point allows optimization of the electrical properties of the link. As it has internal termination, an optimal transmission line is more easily constructed, without the worry and impact of stubs for example. In addition, the location of the devices (display, camera, etc) it serves are generally physically separated, and thus a serial point-to-point link serves them better than routing a multi-drop or multi-point link. Finally, as the MPL link has only two active wires, the overhead of multiple MPL interfaces is low cost and space/pin count efficiency compared to parallel buses.

7 MPL Data Signaling Rates

The basic data rate for the LM2500/1/2 Transceivers are up to 160 Mbps in the Master-to-Slave direction. In this mode the maximum transmission rate is 160 Mbps (6.25 ns unit interval), and the clock is 80 MHz since both edges of the clock are used. Using both edges allows for a low frequency clock signal (vs. 160 MHz single-edge), which aids in reducing EMI. For the back channel, (Data flow from Slave-to-Master) only the rising edge of the clock is used by the Slave to gate the data, allowing more time for data sampling in the Slave-to-Master direction based on the Master supplied clock. By maintaining the 80 MHz clock, an 80 Mbps back channel transmission rate is supported.

The current basic transmission rate is ≤160 Mbps with extensions to 200 Mbps and 400 Mbps. It is foreseen in the future that the physical layer is capable of operating into the Gigabit per second range. These higher data rates are under study now.

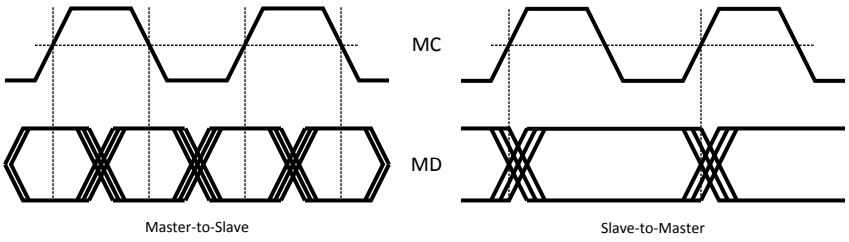

Figure 4. MPL Serial Bus Timing—Dual and Single Edge Timing

8 MPL Bus Phases

There are four bus phases on the MPL serial bus. These are determined by the state of the MC and MD lines. Two of the bus phases have options. The MPL bus phases are shown in Table 1.

Table 1. MPL Link Phases[(1)]

Name	MC State	MD State	Phase Description	Pre-Phase	Post-Phase
Link-Off (O)	0	0	Link is Off, no current flow or transmission	A, I or LU	LU
Idle (I)	A	L	Data is static (Low)	A or LU	A or O

(1) Notes on MC/MD Line State:
0 = no line current (off)
L = Logic Low—The higher level of current on the MC and MD lines
H = Logic High—The lower level of current on the MC and MD lines
X = Low or High
A = active clock

Table 1. MPL Link Phases[(1)] (continued)

Name		MC State	MD State	Phase Description	Pre-Phase	Post-Phase
Active (A)	Command (C)	A	X	Command information	LU, A, I	A, I, or O
	Turn Around (TA', TA")	A	L/0/L	Turn Around—MD line is OFF to turn around the direction		
	Data In (DI)	A	X	Data In (Read)—includes Command, TA', TA" sub phases		
	Data Out (DO)	A	X	Data Out (Write)—includes Command, Data Out phases		
Link-Up (LU)	Master (M)	LHL	00L	Master initiated Link-Up	O	A, I, or O
	Slave (S)	LHL	L0L	Slave requested Link-Up		
	Dual (D)	LHL	L0L	Dual requested Link-Up		

9 Power Up/Down

In the Power-Save mode (OFF), both MD and MC drivers and are turned off with zero line current flowing. The Master may inform the Slave to LINK-UP by driving the MC line Low for 12 clocks (t1)—Point A. Next it drives the MC line High for 12 clocks (t2). On the Low-to-High transition—Point B, the Slave's current sources are optimized to maximize noise margins. Finally the Master drives both MC and MD to a stable Low state for 12 clocks (t3). The LINK-UP phase requires 36 cycles to complete. The Master may now send data (active), idle the bus or return to Link-Off.

In the Figure 5 example, an IDLE bus phase is shown with duration of time t4 after which the bus is active and the "High" start bit on MD initiates the transfer of information—Point C.

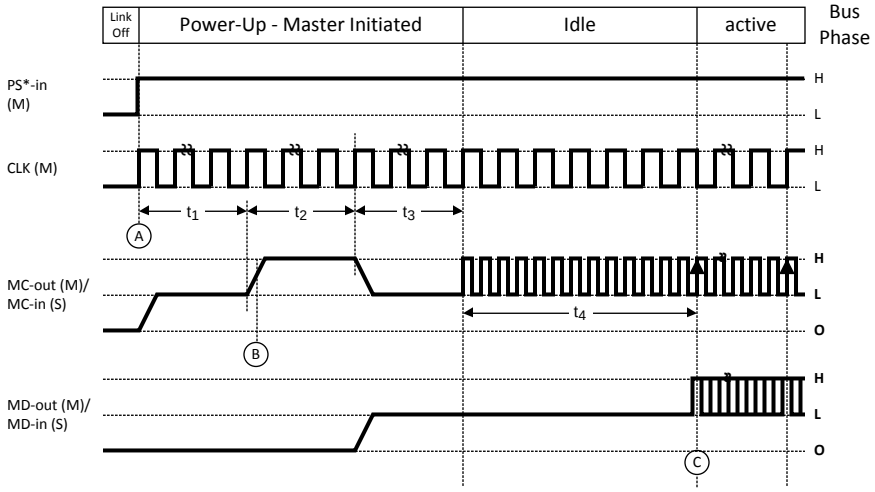

Figure 5. MPL Link-Up Request—Master Initiated

Note that the Master is in Power_Save mode, as the Link is off, and the Master's PLL is running and locked to its source (application dependant—not required if host provides a high speed clock).

The Slave has the capability to inform the Master to power-up also. This is accomplished by the Slave driving the MD line to a logic Low until the Master responds with the MC signal driven Low also. The Master detects the presence of current flowing in the MD line and generates an INTR signal that informs the local host of the Slave's Link-up request. The host clears the INTR by de-asserting the PS* pin and then the Master drives the MC line Low also for a minimum of 12 clock cycles. The Slave detects the Low MC state and then turns off its MD Driver before the MC High-to-Low transition. The Master sensing the MD line is off then drives the MD lines to a static Low. After another duration of 12 clock cycles, the bus phase is now in an IDLE state and may remain in IDLE, power back off (Link Off), or become active as shown in Figure 6. Note that t3 depends upon system (host) response time.

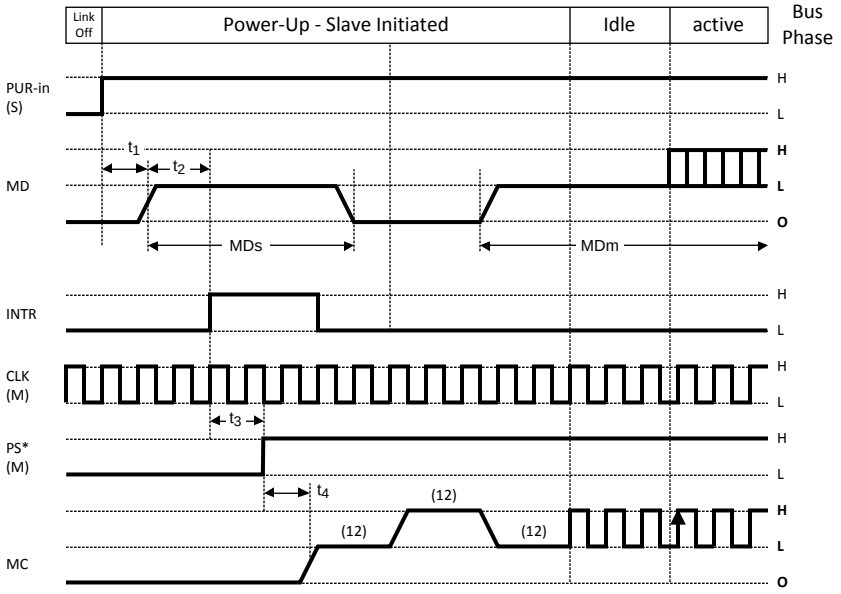

Figure 6. MPL Link-Up Request—Slave Initiated

Figure 7 illustrates the timing when both the Slave and Master initiate a link-up request at about the same time. Due to flight times the timing may overlap. Thus this sequence is available to link-up the MPL bus for this situation. The bus has zero current flowing in both lines (MC and MD) in the Link-Off phase. If both the Master and the Slave initiate a power-up sequence at approximately the same time (both MC and MD are driven Low) the Slave then detects that the Master is driving the MC line and then disables its MD driver (see MDs). The Master detects the MC Low and then initiates a standard Master initiated power up sequence as shown in Figure 5. After this, the bus phase is now in an IDLE state (or may become active) and may remain in IDLE, power back off, or become active as shown in Figure 7. Note that in Figure 7, control signals are not shown.

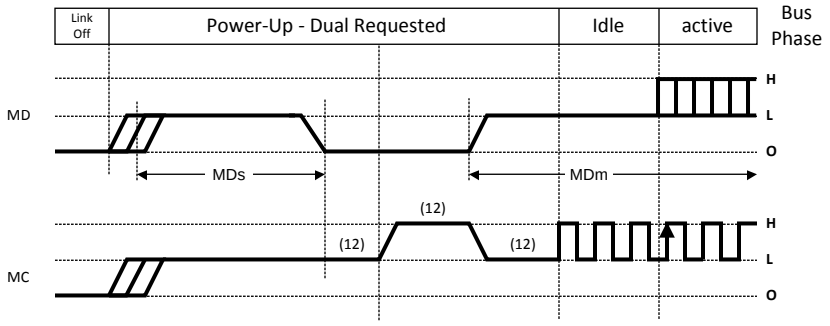

Figure 7. MPL Link-Up—Dual Requested

10 Interconnect Media

PCB traces, flex cables, or short cables can be used for interconnects. The exact type and configuration depends upon actual system requirements. These include length of the interconnect, mechanical restrictions, and EMC requirements. Flex interconnects provide an economical interconnect and are commonly used in small applications. Single sided flex interconnects are the lowest cost, but tend to be higher in impedance and offer limited shielding. These are normally sufficient for slower data rates and in low noise applications. Microstrip (double sided flex) provides a more controlled impedance path and 50Ω lines are easily obtainable with common dimensions. An additional benefit is the ground layer shielding and optional ground guard traces. At a minimum, three signal lines could be used. Two for the MD and MC line and a shared ground return. The MG ground should have a ground connection at both ends of the link to minimize ground loops. Examples of single and double sided cross sections are shown in Figure 8.

Connector details are also application dependant. However, Plug or ZIF connectors are commonly used as they are only used on one side (not on flex side) and are offered in small footprints and are economical compared to pin and socket type connectors.

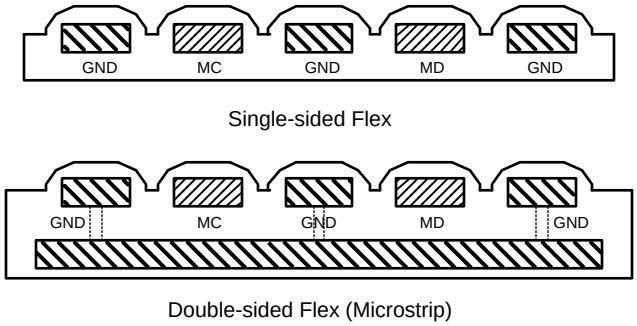

Figure 8. Flex Media Cross Sections

11 How Far/How fast?

Initial MPL applications are initially targeted up to 40, 80, and 160 Mbps in the forward direction. This is determined mainly by the Camera array size and clock rate or by the display's resolution. A doubling of data rate is planned to 320 Mbps and simulations predict that Gigabit rates are entirely feasible. Data signaling rate is also a factor of drive current and line length and media quality and impedance control. Most display applications are single direction or have lite back channel needs. Thus to simplify implementation, the clock is always sourced from the Master to the Slave. To maximize timing margins, a half rate back channel with single edge clocking is supported—see Figure 4.

The target applications for MPL are small portable equipment such as cell phones and PDAs. Inside these, interconnects of 5-10-15 cm (2-4-6 inch) are common. MPL interfaces tend to be less than 30 cm in total length. As discussed above, length is also related to media quality, data rate, and drive current (Idata) setting.

12 MPL Power Dissipation

MPL saves power in many ways. First, a low current-mode signaling scheme is used for data transmission. The magnitude of current is in the low 100's of µA for systems capable of several hundred megabits per second. The low current and current sources tend to limit switching spikes, noise, and generates only a small delta voltage on the line. With the small voltage on the line, power is saved in not having to charge/discharge the line/load capacitance as much compared to a larger swing signaling transmission scheme. The chipset also has a power-save (Link Off) feature that shuts off the interface current when it is not needed to save even more system power. Lastly, by sending data and clock separately, the receiver and possibly the transmitter (if a high speed clock is already available) does not require a power consuming PLL block or encoders.

13 EMI–

MPL is expected to generate very small amounts of EMI due to:

a) 10 mV transition (small dV/dT)

b) 150/450 µA signaling states

c) current-mode transmission with soft edges

d) small current loop between the signal line and MPL ground

e) at frequency clock

f) dedicated current return path/small ring antenna

Also, WhisperBus has been shown to greatly reduce EMI in flat panels when compared to 3V single ended transmission. National has received reports of less EMI for WhisperBus™ interfaces than TFT panels that employ RSDS (Reduced LVDS signaling of 200 mV) from Notebook Display Customers.

14 EMS/RFI–

While MPL uses a small swing and low current, it is still robust. This is related to the fact that it uses a low impedance termination to ground and low impedance lines (50Ω) which both help to minimize noise pick up.

On RFI tolerance, National plans tests soon, to date we have done some preliminary tests on a large flat panel that used WB for the data lines and RSDS (LVDS) for the clock line. For these tests, cell phone antennas were placed on the targeted traces along with a 5W CB Radio (49 MHz) while transmitting voice. Under the testing the WB lines showed no errors based on the column driver error rate pin in test mode. The RSDS/LVDS line was found to fail first! This is believed to be related to the transmission scheme and termination. LVDS tends to be 100Ω terminated with high common-mode impedance, thus a noise signal can couple on and create common-mode modulations that eventually breaks the receiver detection circuitry and corrupts the differential signal. On the other had, WB (MPL) is terminated to an AC ground point with a low impedance, thus a stronger signal is needed to generate a voltage to upset the data! Also, MPL is a 50Ω impedance to ground vs. LVDS which depending upon design may be many kΩ or even greater to ground. (Cell phones used: 2 different Samsung Sprint PCS phones and a Nokia 5190). Other factors that impact system RFI tolerance include system grounding, shielding and interconnect design.

15 MPL Standard

The physical (MPL-0) and link layers for MPL is currently under study by leading edge system manufacturers, silicon providers, and other interested parties.

16 Summary

MPL that sets it apart from other Interfaces is its focus on Video applications for portable applications. Notable features are:

- Few Wires
- Low Power
- Low EMI

- Simple Protocol/Low Gate Count
- Video Focused
- Bi-directional Point-to-Point link
- Open Standard/Multiple Sources
- Megapixels @ milliwatts!

17 References

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