ADC1210

AN-245 Applications of the ADC1210 CMOS A/D Converter

Literature Number: SNOA636

Application of the ADC1210 CMOS A/D Converter

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INTRODUCTION

The ADC1210 is the answer to a need for analog to digital conversion in applications requiring low power, medium speed, or medium to high accuracy for low cost. The versatile input configurations allow many different input scale ranges and output logic formats.

The wide supply voltage range of 5V to 15V readily adapts the device to many applications. The very low power dissipation yields remarkable conversion linearity over the full operating temperature range. Table I below summarizes the typical performance of the ADC1210.

TABLE I. ADC1210 Performance Characteristics

Resolution	12 bits
Linearity Error, $T_A = 25°C$	$\pm 0.0183\%$ FS MAX
Over Temperature	$\pm 0.0366\%$ FS MAX
Full Scale Error, $T_A = 25°C$	0.2% FS MAX
Zero Scale Error, $T_A = 25°C$	0.2% FS MAX
Quantization Error	$\pm \frac{1}{2}$ LSB MAX
Conversion Time	200 μs MAX

This note expands the scope of application configurations and techniques beyond those shown in the data sheet. The first section discusses the theory of operation. The remaining sections are devoted to applications that extract the optimum potential from the ADC1210.

THEORY OF OPERATION

Like most successive approximation A to D's, the ADC1210 consists of a successive approximation register (SAR), a D to A converter, and a comparator to test the SAR's output against the unknown analog input. In the case of the ADC1210, these elements are connected to allow unusual versatility in matching performance to the user's applications.

The SAR is a specialized shift register programmed such that a start pulse applies a logical low to the most significant bit (MSB) and logical highs to all other bits, thus applying a half scale digital signal to the DAC. If the comparator finds that the unknown analog input is below half scale, the low is shifted to the second bit to test for quarter scale. If, on the other hand, the comparator finds that the analog input is above half scale, the ''low'' state is not only shifted to the second bit, but also retained in the MSB, thus forming the digital code for three quarters scale. Upon completing the quarter (or three-quarter) sacle test, the next clock pulse sets the SAR to test either $\frac{1}{8}$, $\frac{3}{8}$, $\frac{5}{8}$, or $\frac{7}{8}$ full scale, depending on the input and the previous decisions. This successive half-the-previous-scale approximation sequence continues for the remaining lower order bits. The thirteenth clock pulse shifts the test bit off the end of the working register and into the conversion complete output. *Figure 1* shows the schematic diagram of the device.

OPERATING CONFIGURATIONS

Figures 2 through *5* show four operating configurations in addition to those presented in the data sheet.

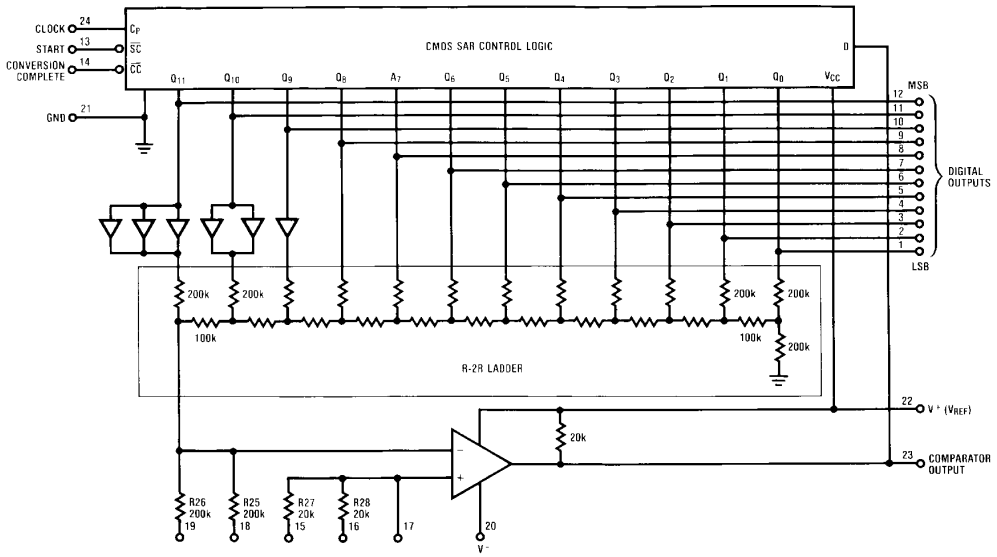

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FIGURE 1. Schematic Drawing

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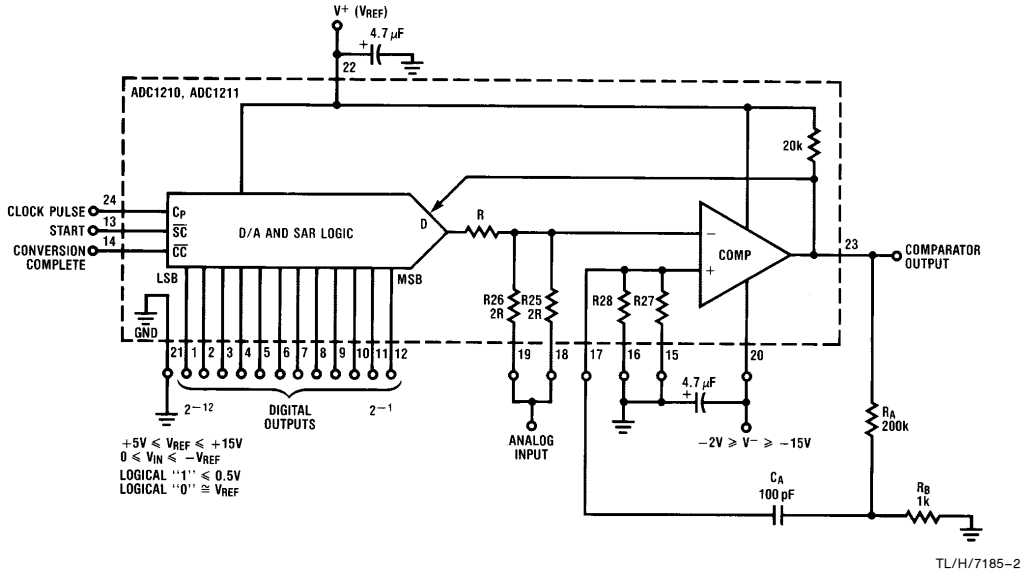

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FIGURE 2. Complementary Logic, 0V to $-V_{REF}$ Input

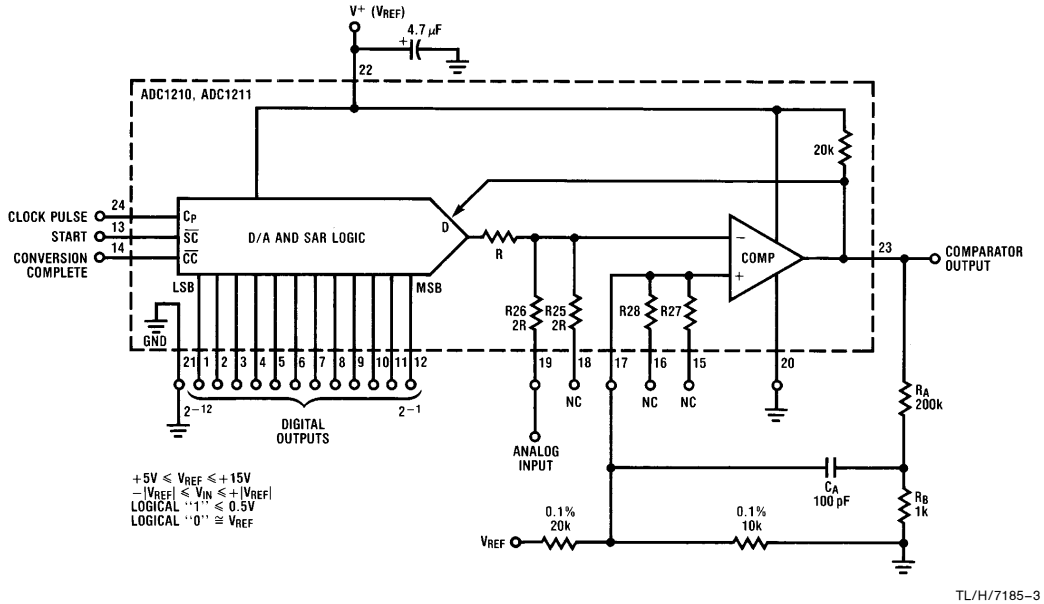

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FIGURE 3. Complementary Logic, Bipolar $-V_{REF}$ to $+V_{REF}$ Input

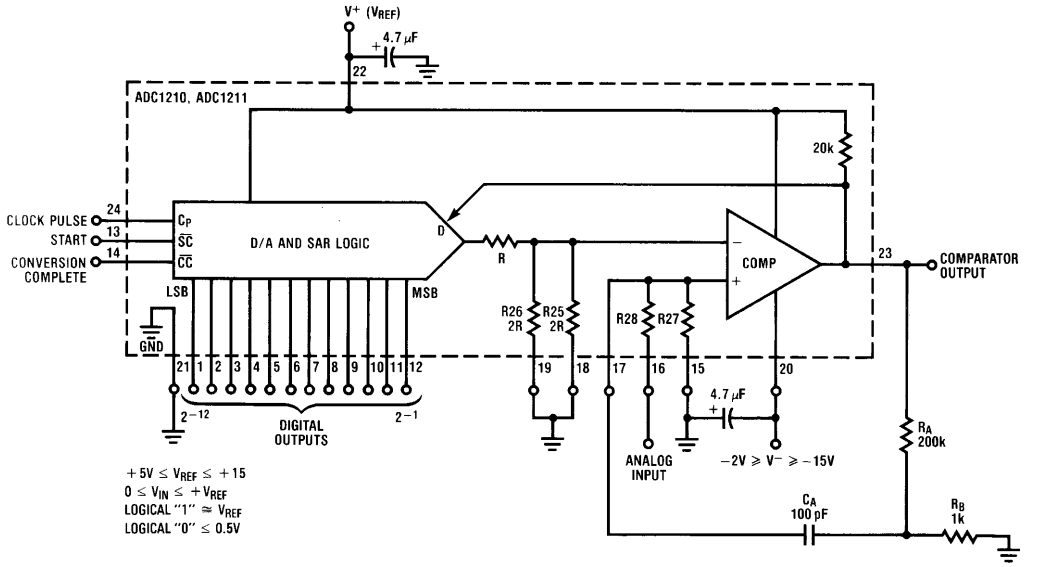

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FIGURE 4. Positive True Logic, 0V to $+V_{REF}$ Input

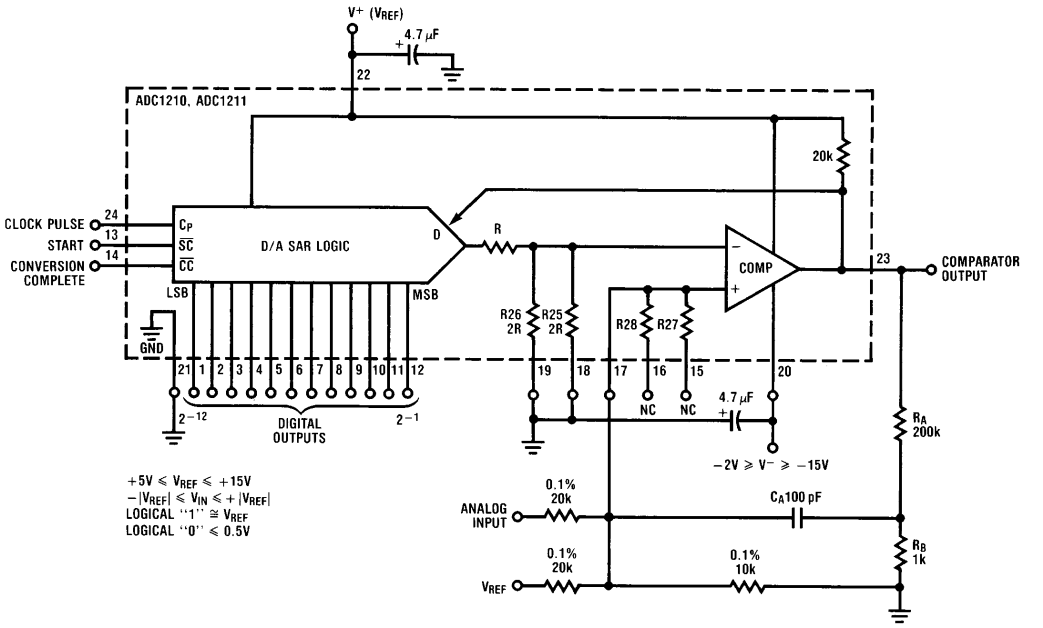

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FIGURE 5. Positive True Logic, Bipolar $-V_{REF}$ to $+V_{REF}$ Input

DESIGN CONSIDERATIONS

To Complement, or Not to Complement

Of the two recommended logic configurations, the complementary version is preferred. It provides greater accuracy than the straight binary version. The reason for that is that with the complementary logic configuration, a reference voltage is fixed at the non-inverting input of the comparator. Consequently, the comparator operates at this fixed threshold independent of the input voltage. For the straight binary configuration, the analog input drives the non-inverting input of the comparator so that the common mode voltage on the comparator input varies with the analog input. This adds a non-linear offset voltage of less than ¼ LSB.

Regardless which configuration is used, the comparator input common mode range must not be exceeded. In fact, the voltage at either comparator input must be no less than 0.5 volts from the negative supply and 2.0 volts from the positive supply. Therefore, for applications requiring common mode range to ground, simply connect a negative supply (−2V to −15V) to pin 20.

Layout Considerations

High resolution D/A and A/D converter circuits may have their entire error budget blown if any digital noise is allowed to enter the analog circuit.

Exercising care in the layout is certain to minimize frustrations. Single point analog grounding is a good place to start. All analog ground connections and supply bypassing should be returned to this point. In fact, in critical applications, the ADC1210 GND pin should be made "the" reference node. Furthermore, one should separate the analog ground from the digital ground. Any excursion of switching spikes generated in the digital circuit is, to some degree, decoupled from the analog circuitry. *Figure 6* illustrates this. Of course, these two points are eventually tied together at the power supply/chassis common.

In addition to a good ground system, it is a good idea to keep digital signal traces as far apart from the analog input as is practical in order to avoid signal cross coupling.

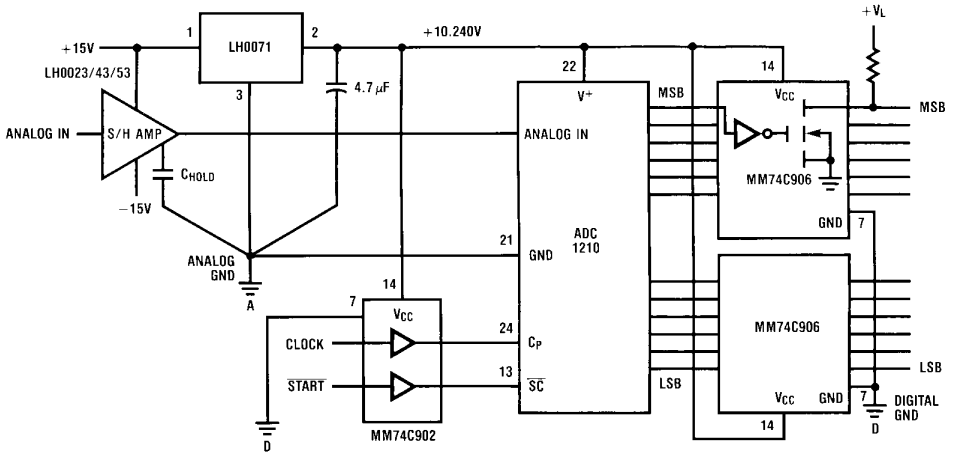

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FIGURE 6. Grounding Considerations of Interface Circuits

Power Supply Bypassing

The supply input only provides power to the digital logic, it is also a reference voltage to the resistor ladder network of the ADC1210. This voltage must be a very stable source. A precision reference device such as the LH0070 or LH0071 is ideal for the ADC1210. However, the internal CMOS Successive Approximation Register (SAR) invariably generates current spikes (10–20 mA peak) in the supply pin as the logic circuit switches past the linear region. Consequently, if a reference device such as the LH0070 is used, the current spike tends to cause excursions in the reference voltage, thus threatening conversion accuracy. To preserve the 12-bit accuracy, bypass the supply pin with a 4.7 μF tantalum capacitor. In high noise environments, a 22 μF capacitor shunted by a 0.1 μF ceramic disc capacitor is desirable.

If pin 20 is connected to a negative supply, it too should be bypassed to prevent voltage fluctuations from affecting the comparator operation.

Output Drive Capability

The digital outputs of the ADC1210 and the outputs of the SAR, through which the resistor ladder is referenced, are one and the same. Any excessive load current on the digital output lines will degrade conversion accuracy. For this reason, the ADC1210 must interface with CMOS logic. However, the three most significant bits (pins 10, 11, and 12) are buffered from the R-2R ladder and are capable of driving light loads without degrading linearity. This could prove useful in 2's complement applications where an inverter is necessary in the MSB; one might construct this inverter with a discrete NPN transistor and two resistors. The bit most sensitive to output loading is the fourth most significant (pin 9). An error voltage at this pin gets divided down by a factor of 16 before being applied to the comparator, so if we wish to limit the error due to output loading to say, ½ LSB, or 1.25 mV at the comparator, we can tolerate 20 mV at pin 9. If all lower bits will have the same output load, the error must be limited to 10 mV. Since all of the digital outputs have a maximum ON resistance of 350Ω at 10V V_{REF} in both high and low states, the maximum allowable load current is 10 mV/350Ω = 29 μA. This current requirement is easily satisfied with an MM74C914 or MM74C901 thru MM74C902 level translators for interface with logic levels different than V_{REF}.

Comparator Hysteresis

Even an ideal comparator can be expected to oscillate due to stray capacitive feedback if biased in the linear region. It is the normal operation of the SAR feedback loop to do just that . . . at least at or toward the end of the conversion cycle. For most applications, this oscillation is only a minor bother, as the SAR register would have locked out the converted data from further changes at the end of conversion. If that is still undesirable, the Conversion Complete ($\overline{CC}$) Signal may be used to drive an open-collector gate (such as the MM74C906) with the output wire-ORed to the comparator output. In this way, the comparator is always clamped to the low state at the end of conversion. Normal operation resumes upon restart of a new conversion cycle.

In normal operation, however, if we want to preserve 12-bit accuracy, the comparator oscillation should be suppressed. The recommended technique is to apply a slight amount of AC hysteresis (50 mV) at the beginning of the decision cycle, but let it decay away to an acceptable accuracy before the decision is actually recorded in the SAR. The approximate decay time is (5) $\times$ (10k + 1k) $\times$ (100 pF), or 5.5 μs (see *Figure 2*).

For those applications using supply voltage other than 10V, say 5V, and if 50 mV initial hysteresis is to be maintained, the 200 kΩ (R_A) resistor in *Figure 2* should be changed to 100 kΩ based on the relationship:

$$\frac{R_B}{R_A + R_B} V_{REF} = 50 \text{ mV}$$

Where: R_B = 1 kΩ

High Speed Conversion Technique

By using one IC, one discrete NPN transistor, and a resistor, the ADC1210 can be made to run at up to 500 kHz clock frequency, or 12-bit conversion time of 26 μs. The circuit is shown in *Figure 7*. The idea is to clamp the comparator output low until the SAR is ready to strobe in the data at the rising edge of the conversion clock. Comparator oscillation is suppressed and kept from influencing the conversion decisions. This technique eliminates the need for the AC hysteresis circuit.

To implement the idea, a complementary phased clock is required. The positive phase is used to clock the converter SAR as is normally the case. The inverted clock, generated from the same clock signal, is inverted by the transistor. The open collector is wire-ORed to the output of the comparator. During the first half of the clock cycle (50% duty cycle), the comparator output is clamped and disabled, though its internal operation is still in working order. During the last half cycle, the comparator output is unclamped. Thus, the output is permitted to slew to the final logic state just before the decision is logged into the SAR. The MM74C906 buffer (or with two inverting buffers) provides adequate propagation delay such that the comparator output data is held long enough to resolve any internal logic set-up time requirements.

The 500 kHz clock implies that the absolute minimum amount of time required for the comparator output to be unclamped is 1 μs. Therefore, for applications with clock signal other than 50% duty cycle, this 1 μs period must be observed.

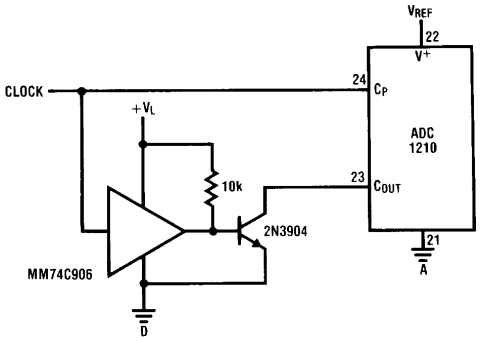

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FIGURE 7. High Speed Conversion Circuit

Testing has demonstrated reliable performance from this circuit beyond the recommended device operating frequency of 65 kHz. However, the AC hysteresis circuit is still a very reliable technique below this clock frequency and, therefore, should be used. Only in applications where the required clock frequency is above 65 kHz should the above-mentioned technique be adopted.

Synchronizing Conversion Start Signal

It is recommended that the $\overline{\text{START CONVERT}}$ input be synchronized to the CLOCK input. This avoids the possibility of the comparator making an error on the first (MSB) decision when the analog input is near ½ scale. There is a chance that energy can be coupled to the comparator from the rising edge of the $\overline{\text{START}}$ signal. If this occurs just before the rising edge of the clock, a wrong MSB decision can be made if time is not allowed for the charge to dissipate. The synchronization circuit in *Figure 8* effectively prevents this from occurring.

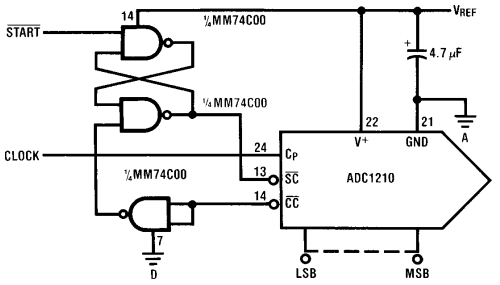

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FIGURE 8. Synchronizing START CONVERT Signal

The circuit operates as follows: initially the latch is in the RESET state and the converter is in the end-of-conversion state ($\overline{\text{CC}}$ output at logic low). The $\overline{\text{START}}$ signal sets the latch and, on the next positive clock transition, initializes all internal registers in the converter. The $\overline{\text{CC}}$ output is set to logic high, presetting the external latch. The latch is held in the "RESET" state during the entire conversion period, effectively preventing a new $\overline{\text{START}}$ signal from interrupting the conversion.

Serial Output

The comparator output does contain the stream of serially converted data with the most significant bit first. However, recognizing the danger of comparator oscillation, there is a potential for the external serial data register to latch a data bit different from that recorded in the SAR due to different logic set-up time requirements. If the ADC1210 accepts an error in any one data bit, the subsequent lower order bits tend to correct for it. On the other hand, an external serial register has no provision for error correction. All subsequent bits following a bit in error will not be valid data.

The 12 bits of information can be shifted out serially by using an MM74C150 digital multiplexer. The circuit is shown in *Figure 9*. This scheme permits valid data to be available at the serial output port as fast as half a clock cycle after the most current decision. The data are thus synchronized to the converter clock (here the serial data are synchronized at the falling edge of the system CLOCK, to avoid clock skew). Obviously, a number of variations can be made to this basic circuit for use with different handshake protocols.

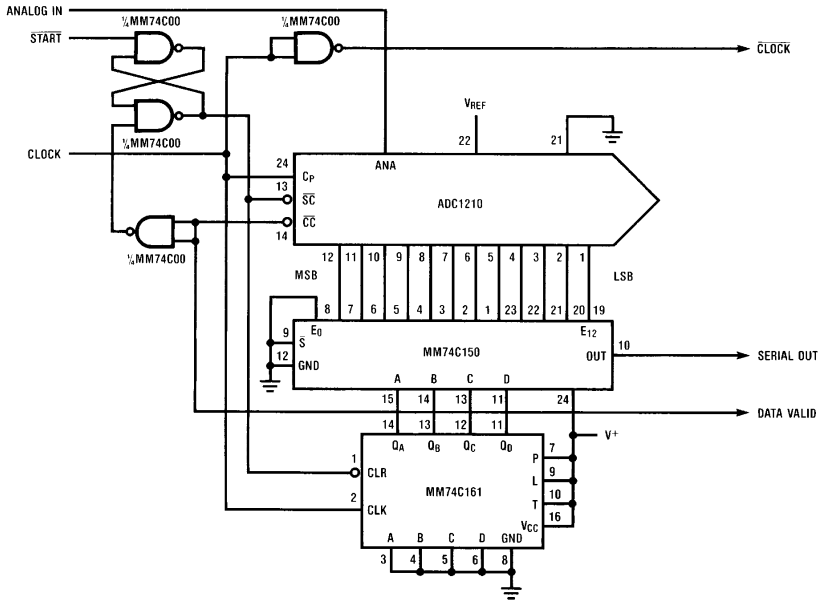

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FIGURE 9. 12-Bit A/D Converter with Serial Output

APPLICATIONS

Long Time Sample and Hold

The circuit in *Figure 10* is a particularly simple realization of an infinite sample and hold. This scheme requires two low-cost analog sample-and-hold amplifiers to complete the circuit.

The idea is to utilize the digital-loop feedback mechanism of the ADC1210 which, in the normal conversion mode, replicates the analog input voltage at the output of the SAR/D-to-A converter.

The operation of the circuit may be described as follows: During the normal ''hold'' mode, the replicated analog voltage is buffered straight through the S/H amplifier to the output. Upon an issuance of a $\overline{\text{SAMPLE}}$ signal, this S/H amplifier is placed in the hold mode, holding the voltage until the new analog voltage is valid. The same $\overline{\text{SAMPLE}}$ signal triggers an update to the input sample-and-hold amplifier. The most current analog voltage is captured and held for conversion. This way, the previously determined voltage is held stable at the output during the conversion cycle while the SAR/D-to-A continuously adjust to replicate the new input voltage. At the end of the conversion, the output sample-and-hold amplifier is once again placed in the track mode. The new analog voltage is then regenerated.

An Auto-Ranging Gain-Programmed A/D Converter

The circuit in *Figure 11* shows one possible circuit of an auto-ranging A/D converter. The circuit has a total of 8 gain ranges, with the ranging done in the LH0086 Programmable Gain Amplifier (for differential input, use the LH0084 with ranges of 1, 2, 5, 10 digitally programmed, or pin strap programmed for multiplying factors of 1, 4, and 10). The gain ranges are: 1, 2, 5, 10, 20, 50, 100, and 200. It effectively improves the A/D *resolution* from 12 bits to an equivalent of 19 bits, a dynamic range of better than 100 dB.

The circuit has relatively high speed ranging due to the very fast settling time of the LH0086, typically 5 μs for 10V swing, well within the 15 μs converter clock period. Thus, the ranging circuit is designed to work off the same clock.

The circuit is designed such that the auto-ranging function is transparent to the user. All command signals into and out of the system are identical to those of an ADC1210 operating alone. The only exception is that the system requires one and one-half clock cycle (mandatory auto range cycle), plus however many ranges it has to scale to (each scale requires one clock period, 7 possible range switching in all) in addition to the basic 13 conversion cycle required by the ADC1210. Therefore, in the best case where no ranging is necessary, the circuit adds 22.5 μs to the conversion time; and in the worst case, an additional 128 μs.

In the quiescent state where the ADC1210 is in the non-conversion mode, the auto-ranging circuit is free to function normally. Upon an issuance of a $\overline{\text{START}}$ signal, the next clock rising edge puts the circuit in the final auto range cycle before conversion begins. If the need for up-range or down-range is detected, the circuit remains in the auto range mode until all necessary scaling is completed. The control circuit then issues a start conversion signal to the ADC1210. Half a clock cycle later, the ADC1210 begins conversion and suspends the auto-ranging operation until the conversion is completed. At which time the 12-bit converter data plus the 3-bit range data are valid for further processing.

This design is suitable for applications in data-acquisition systems or portable instruments, particularly where low power is an important consideration. Other variations from this basic scheme can be realized depending on the user's requirements.

SUMMARY

The ADC1210 is a low-cost, medium-speed CMOS analog-to-digital converter with 12-bit resolution and linearity. It has wide supply range and flexible configuration to allow varied applications such as field instruments and sampled data systems.

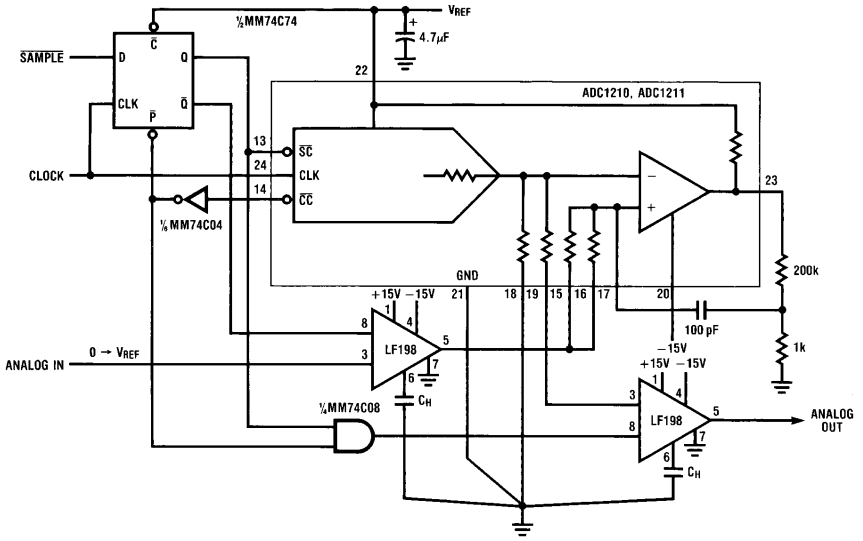

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FIGURE 10. Infinite Sample and Hold Amplifier

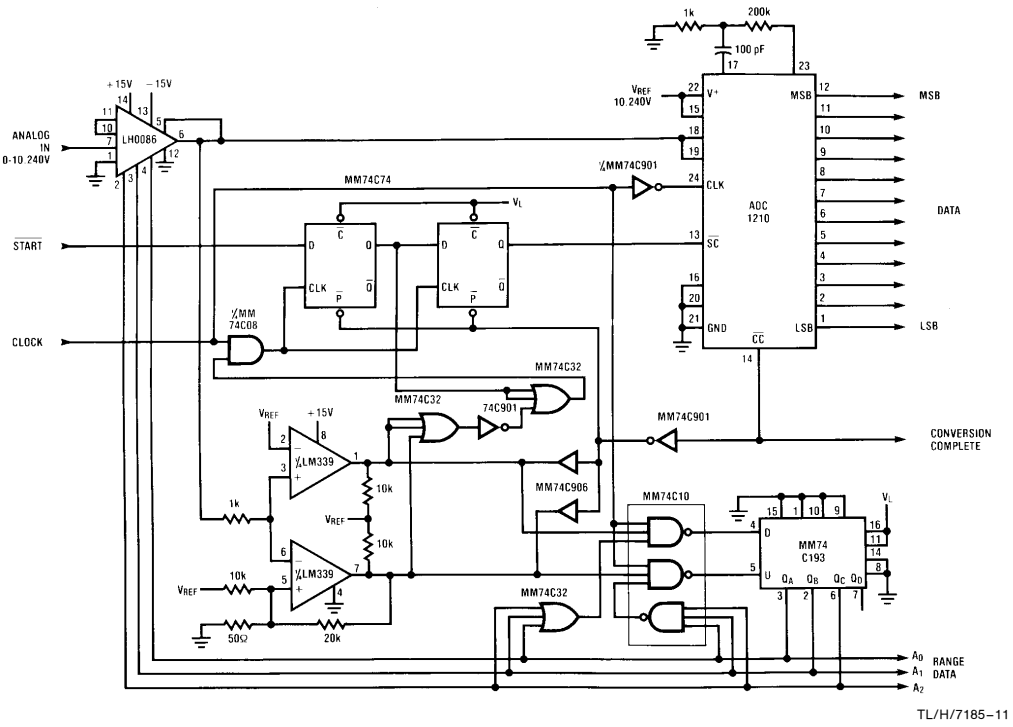

FIGURE 11. Auto Gain Ranging A/D Converter

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