Configuring Digital I/Os of the TMS320F240 DSP Controller

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Abstract

This document describes how to configure the digital I/Os of the Texas Instruments (TI™) TMS320F240. The TMS320F240 DSP controller has 28 digital I/O pins. All 28 digital I/Os are multiplexed with other functions. These I/Os are in addition to the 64k of addressable I/O space associated with the address and data pins. Since the I/O pins are shared with functions from several different peripheral modules, the user must be aware of several configuration registers described in this document.

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Design Problem

How do I configure the digital I/Os of the TMS320F240?

Solution

The Texas Instruments (TI™) TMS320F240 DSP controller has 28 digital I/O pins. All 28 digital I/Os are multiplexed with other functions. These I/Os are in addition to the 64k of addressable I/O space associated with the address and data pins. Since the I/O pins are shared with functions from several different peripheral modules, the user must be aware of several configuration registers. Table 1 shows the configuration registers that are used for the GPIO.

Table 1. Registers Used for GPIO Configuration

Register	Address	Name	Affected Pins
SCIPC2	705Eh	SCI Port Control Reg 2	43-4
SPIPC1	7040h	SPI Port Control Reg 1	45, 48
SPIPC2	704Eh	SPI Port Control Reg 2	49, 51
XINT2CR	7078h	Ext Int 2 Control Reg	54
XINT3CR	707Ah	Ext Int 3 Control Reg	55
OCRA	7090h	I/O Mux Control Reg A	72-3, 90-1, 100-2, 105-9
OCRB	7092h	I/O Mux Control Reg B	65-70
PADATDIR	7098h	I/O Port A Data/Dir Reg	72-3, 90-1
PBDATDIR	709Ah	I/O Port B Data/Dir Reg	100-2, 105-9
PCDATDIR	709Ch	I/O Port B Data/Dir Reg	63-70

Configuration details for each pin are listed in Table 2. Note that Pin 64 is a useful pin for debugging purposes. In addition to the CPUCLK, the WDCLK and the SYSCLK can be output from this pin. Also, the XINT2 and XINT3 pins are configured as GPIO when these interrupts are disabled. The user should be careful not to inadvertently drive these outputs by configuring these pins as inputs.

Table 2. Configuration Details for Each Shared I/O Pin

Pin #	Shared Function	After RESET	Make Pin GPIO	Configure as Input	Read Data from	Configure as Output	Write Data to
43	SCIRXD	GPI	SCIPC2.1=0	SCIPC2.0=0	SCIPC2.3	SCIPC2.0=1	SCIPC2.2
44	SCITXD	GPI	SCIPC2.5=0	SCIPC2.4=0	SCIPC2.7	SCIPC2.4=1	SCIPC2.6
45	SPISIMO	GPI	SPIPC2.5=0	SPIPC2.4=0	SPIPC2.7	SPIPC2.4=1	SPIPC2.6
48	SPISOMI	GPI	SPIPC2.1=0	SPIPC2.0=0	SPIPC2.3	SPIPC2.0=0	SPIPC2.2
49	SPICLK	GPI	SPIPC1.1=0	SPIPC1.0=0	SPIPC1.3	SPIPC1.0=0	SPIPC1.2
51	SPISTE[1]	GPI	SPIPC1.5=0	SPIPC1.4=0	SPIPC1.7	SPIPC1.4=1	SPIPC1.6
54	XINT2	GPI	XINT2CR.0=0	XINT2CR.4=0	XINT2CR.6	XINT2CR.4=1	XINT2CR.3
55	XINT3	GPI	XINT3CR.0=0	XINT3CR.4=0	XINT3CR.6	XINT3CR.4=1	XINT3CR.3
63	ADCSOC	GPI	OCRB.0=0	PCDATDIR.8=0	PCDATDIR.0	PCDATDIR.8=1	PCDATDIR.0
64	CPUCLK	CPUCLK	SYSCR.6,7=00	PCDATDIR.9=0	PCDATDIR.1	PCDATDIR.9=1	PCDATDIR.1
65	XF	GPO-low	OCRB.2=1	PCDATDIR.10=0	PCDATDIR.2	PCDATDIR.10=1	PCDATDIR.1
66	BIO	GPO-low	OCRB.3=1	PCDATDIR.11=0	PCDATDIR.3	PCDATDIR.11=1	PCDATDIR.3
67	CAP1/QEP1	GPI	OCRB.4=0	PCDATDIR.12=0	PCDATDIR.4	PCDATDIR.12=1	PCDATDIR.4
68	CAP2/QEP2	GPI	OCRB.5=0	PCDATDIR.13=0	PCDATDIR.5	PCDATDIR.13=1	PCDATDIR.5
69	CAP3	GPI	OCRB.6=0	PCDATDIR.14=0	PCDATDIR.6	PCDATDIR.14=1	PCDATDIR.6
70	CAP4	GPI	OCRB.7=0	PCDATDIR.15=0	PCDATDIR.7	PCDATDIR.15=1	PCDATDIR.7
72	ADCIN0	GPI	OCRA.0=0	PADATDIR.8=0	PADATDIR.0	PADATDIR.8=1	PADATDIR.0
73	ADCIN1	GPI	OCRA.1=0	PADATDIR.9=0	PADATDIR.1	PADATDIR.9=1	PADATDIR.1
90	ADCIN9	GPI	OCRA.2=0	PADATDIR.10=0	PADATDIR.2	PADATDIR.10=1	PADATDIR.2
91	ADCIN8	GPI	OCRA.3=0	PADATDIR.11=0	PADATDIR.3	PADATDIR.11=1	PADATDIR.3
100	PWM7/CMP7	GPI	OCRA.8=0	PBDATDIR.8=0	PBDATDIR.0	PBDATDIR.8=1	PBDATDIR.0
101	PWM8/CMP8	GPI	OCRA.9=0	PBDATDIR.9=0	PBDATDIR.1	PBDATDIR.9=1	PBDATDIR.0
102	PWM9/CMP9	GPI	OCRA.10=0	PBDATDIR.10=0	PBDATDIR.2	PBDATDIR.10=1	PBDATDIR.2
105	T1PWM/T1CMP	GPI	OCRA.11=0	PBDATDIR.11=0	PBDATDIR.3	PBDATDIR.11=1	PBDATDIR.3
106	T2PWM/T2CMP	GPI	OCRA.12=0	PBDATDIR.12=0	PBDATDIR.4	PBDATDIR.12=1	PBDATDIR.4
107	T3PWM/T3CMP	GPI	OCRA.13=0	PBDATDIR.13=0	PBDATDIR.5	PBDATDIR.13=1	PBDATDIR.5
108	TMRDIR	GPI	OCRA.14=0	PBDATDIR.14=0	PBDATDIR.6	PBDATDIR.14=1	PBDATDIR.6
109	TMRCLK	GPI	OCRA.15=0	PBDATDIR.15=0	PBDATDIR.7	PBDATDIR.15=1	PBDATDIR.7

The code in Example 1 shows how to configure the pins connected to OCRA (I/O Mux Control Reg A) as general-purpose inputs (Pins 72-3, 90-1, 100-2, 105-9). After the pins are set as GPIO in the OCRA register, PADATDIR (I/O Port A Data/Dir Reg) and PBDATDIR (I/O Port B Data/Dir Reg) are configured to set the pins as inputs.

Example 1. Code to Configure I/O that Uses the OCR and PxDATDIR Rregisters

```
OCRA        .set  7090h
PADATDIR    .set  7098h
PBDATDIR    .set  709Ah
LDP         #0E1H     ;Point to appropriate data page,
LACC        #0h       ;pins IOPA0~IOPA3 and IOPB0~IOPB7
SACL        OCRA      ;are configured as I/Os pins.
SACL        PADATDIR  ;IOPA0~IOPA3 are configured as inputs.
LACC        #00F0h    ;Pins IOPB7~IOPB4 are configured as inputs.
SACL        PBDATDIR  ;Pins IOPB3~IOPB0 are configured as outputs.
LACC        PBDATDIR  ;Reading input states IOPB7~IOPB4.
AND         #F000h    ;ACC = input status.
```

[1] SPISTE automatically becomes a GPIO when the SPI is in Master mode.

The code in Example 2 shows how to configure Pin 43 (SCIRXD) as digital input and Pin 44 (SCITXD)as digital output-low. Register SCIPC2 (port control register) needs to be configured to setup Pins 43 and 44.

Example 2. Code to Configure I/O Using Individual Peripheral Control Registers

```
SCIPC2          .set  705Eh
LDP             #0E0h         ;Point to the appropriate data page
SPLK            #0010h, SCIPC2;Configure SCITXD as output-low and
LACC            SCIPC2        ;SCIRXD as input.
OR              #040h         ;Set SCITXD as output-high, without
SACL            SCIPC2        ;changing other configuration bits.
```

The Pin 64 (IOPC1) is associated with the System Control Register. Pin 64 can be configured as an I/O by resetting (putting zero) bits 7 and 6 of the System Control Register (SYSCR @ 7018h). Configuring the PCDATDIR register as shown in Example 1 can set the direction and data of Pin 64. The code in Example 3 shows how to configure Pin 64 as a digital input. As previously noted, Pin 64 is a useful pin for debugging and should be reserved for this purpose.

Example 3. Code to Configure Pin 64 as an Input

```
PCDATDIR        .set  709Ch
SYSCR           .set  7018h
LDP             #0E0h
LACC            SYSCR
AND             #0FF3Fh
SACL            SYSCR
LDP             #0E1
LACC            #0h
SACL            PCDATDIR
```