TMS320C6000 and TMS320C5000 McBSP Features Summary

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ABSTRACT

The multichannel buffered serial ports (McBSP) implemented on the Texas Instruments TMS320C6000™ and TMS320C5000™ digital signal processors (DSPs) are very similar. This document provides a summary of the McBSPs used in each of the C6000™ and C5000™ devices. It provides quick reference information on the specific McBSP features in each DSP. The full functional description of each McBSP is beyond the scope of this document. Refer to the documents listed in the Reference section for such details.

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1   Overview

The TMS320C6000 and TMS320C5000 devices share similar multichannel buffered serial ports (McBSP). The highly flexible McBSPs in the C6000 and C5000 devices provide full duplex, bidirectional communication with external serial devices such as codecs, analog interface chips (AICs), and A/D and D/A converters. The McBSP can also be used for interprocessor communication in multiprocessing applications. Since the C6000 and C5000 digital signal processors (DSP) have different target applications, the McBSPs in these devices are slightly different. In addition, new features and enhancements have been added to the newer McBSPs in the C6000 and C5000 devices. This application report lists the McBSP differences in the following C6000 and C5000 devices: TMS320C5401, TMS320C5402, TMS320C5403, TMS320C5406, TMS320C5409, TMS320C5409A, TMS320C5410, TMS320C5410A, TMS320C5416, TMS320C5420, TMS320C5421, TMS320C5509, TMS320C5510, TMS320C6201 (Rev 3.x), TMS320C6202, TMS320C6203, TMS320C6204, TMS320C6205, TMS320C6211, TMS320C6701, TMS320C6711, TMS320C6414, TMS320C6415, and TMS320C6416.

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2 C6000 and C5000 McBSP Differences

Table 1 shows the different features and enhancements between the McBSP on the C6000 and C5000 devices. Table 2 explains these features. For details on these features, refer to the documents listed in the Reference section.

Table 1. Different Features on the C6000 and C5000 McBSPs

McBSP Features	C6000 Devices										
	C6201-GJC/GJL (Rev 3.x)	C6202	C6203	C6204	C6205	C6211	C6701	CC6711	C6414	C6415	C6416
16-bit registers											
32-bit registers	√	√	√	√	√	√	√	√	√	√	√
Sub-bank addressing											
ABIS mode support											
DX Enabler (DXENA)						√		√	√	√	√
FREE/SOFT Emulation control bits						√		√	√	√	√
IDLE mode power conservation											
CLKS pin available	√	√	√	√	√	√	√	√	√	√	√
SRG clock sources: CPU only											
SRG clock sources: CPU, CLKS	√	√	√	√	√	√	√	√	√	√	√
SRG clock sources: CPU, CLKS, CLKR, CLKX											
R/XWDREVRS 32-bit data reversal						√		√	√	√	√
Independent 128-channel selection capability									√	√	√

McBSP Features	C5000 Devices													
	C5401	C5402	C5409	C5410 PGE	C5410 GGW	C5403	C5406	C5409A	C5410A	C5416	C5420	C5421	C5509	C5510
16-bit registers	√	√	√	√	√	√	√	√	√	√	√	√	√	√
32-bit registers														
Sub-bank addressing	√	√	√	√	√	√	√	√	√	√	√			
ABIS mode support				√	√	√	√	√	√	√		√		
DX Enabler (DXENA)				√	√	√	√	√	√	√	√	√	√	√
FREE/SOFT Emulation control bits	√	√	√	√	√	√	√	√	√	√	√	√	√	√
IDLE mode power conservation				√	√	√	√	√	√	√		√	√	√
CLKS pin as SRG clock source					√						√			√
CPU clock as SRG clock source	√	√	√	√	√	√	√	√	√	√	√	√	√	√
CLKR pin as SRG clock source	√				√	√	√	√	√	√		√	√	√
CLKX pin as SRG clock source	√				√	√	√	√	√	√		√	√	√
R/XWDREVRS 32-bit data reversal						√	√	√	√	√		√		
Independent 128-channel selection capability						√	√	√	√	√		√	√	√

Table 2. Description of McBSP Features on C6000 and C5000 Devices

Feature	Description
16-bit registers	McBSP register size is 16 bits
32-bit registers	McBSP register size is 32 bits
Sub-bank addressing	Sub-bank addressing is used for the TMS320CC54x™ McBSP control registers, due to limitations on the C54x™ data page 0 memory map.
ABIS mode support	ABIS mode provides the capability to implement a PCM link of up to 1024 bits.
DX Enabler (DXENA)	The DXENA bit (SPCR1[7] in C5000 McBSP, SPCR[7] in C6000 McBSP) provides additional delay before the DX line is driven (relative to the clock edge) to provide additional margin against bus contention in systems where multiple McBSPs are sharing the bus (multichannel implementations).
FREE/SOFT Emulation control bits	Provides control of the behavior of the McBSP on emulation stop.
IDLE mode power conservation	The McBSP peripheral is only clocked when active to conserve power.
CLKS pin available	CLKS pin is used as an external clock source to the clock and frame sync generator.
SRG clock sources: CPU only	Since some C5000 devices do not have the CLKS pin available, the only clock source to the sample rate generator is CPU clock.
SRG clock sources: CPU, CLKS only	Either the CPU clock or the external clock source CLKS can be used as an input to the sample rate generator.
SRG clock sources: CPU, CLKS, CLKR, CLKX	The SCLKME bit (PCR[7]) selects the CLKS, CLKR, CLKX, or CPU clock as a clock input to the sample rate generator. Since the CLKS pin does not exist on some of these devices, only the CLKR, CLKX, or CPU clock can be input to the sample rate generator in effect.
R/XWDREVRS 32-bit data reversal	The R/XWDREVRS bit (R/XCR[4]) controls the bit ordering of the 32-bit elements.
Independent 128 channel selection capability	The RMCME (MCR1[9]) and XMCME (MCR2[9]) bits, along with 6 additional receive/transmit channel enable registers, allow 128 channel enable selection.

3   Errata

For all errata regarding the C6000 and C5000 devices, please visit the TI web site at www.ti.com

4   References

1. *TMS320C6000 Peripherals Reference Guide (*SPRU190).
2. *TMS320C54x DSP Enhanced Peripherals Reference Guide (*SPRU302).
3. *TMS320C55x DSP Peripherals Reference Guide* (SPRU317).

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