

# LM6132/LM6134 Dual and Quad Low Power 10 MHz Rail-to-Rail I/O Operational Amplifiers

## 1 Features

- (For 5V Supply, Typ Unless Noted)
- Rail-to-Rail Input CMVR  $-0.25\text{ V}$  to  $5.25\text{ V}$
- Rail-to-Rail Output Swing  $0.01\text{ V}$  to  $4.99\text{ V}$
- High Gain-Bandwidth,  $10\text{ MHz}$  at  $20\text{ kHz}$
- Slew Rate  $12\text{ V}/\mu\text{s}$
- Low Supply Current  $360\text{ }\mu\text{A}/\text{Amp}$
- Wide Supply Range  $2.7\text{ V}$  to over  $24\text{ V}$
- CMRR  $100\text{ dB}$
- Gain  $100\text{ dB}$  with  $R_L = 10\text{ k}$
- PSRR  $82\text{ dB}$

## 2 Applications

- Battery Operated Instrumentation
- Instrumentation Amplifiers
- Portable Scanners
- Wireless Communications
- Flat Panel Display Driver

## 3 Description

The LM6132/34 provides new levels of speed vs. power performance in applications where low voltage supplies or power limitations previously made compromise necessary. With only  $360\text{ }\mu\text{A}/\text{amp}$  supply current, the  $10\text{ MHz}$  gain-bandwidth of this device supports new portable applications where higher power devices unacceptably drain battery life.

The LM6132/34 can be driven by voltages that exceed both power supply rails, thus eliminating concerns over exceeding the common-mode voltage range. The rail-to-rail output swing capability provides the maximum possible dynamic range at the output. This is particularly important when operating on low supply voltages. The LM6132/34 can also drive large capacitive loads without oscillating.

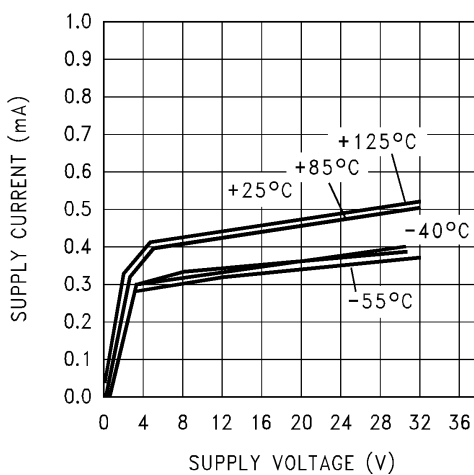
Operating on supplies from  $2.7\text{ V}$  to over  $24\text{ V}$ , the LM6132/34 is excellent for a very wide range of applications, from battery operated systems with large bandwidth requirements to high speed instrumentation.

### Device Information<sup>(1)</sup>

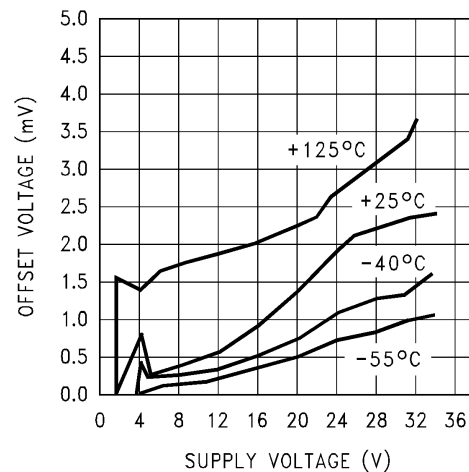
PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM6132	SOIC (8)	4.90 mm x 3.91 mm
LM6132	PDIP (8)	9.81 mm x 6.35 mm
LM6134	SOIC (14)	8.65 mm x 3.91 mm
LM6134	PDIP (14)	19.177 mm x 6.35 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

**Supply Current vs. Supply Voltage**



**Offset Voltage vs. Supply Voltage**



## Table of Contents

<b>1 Features</b> ..... 1 <b>2 Applications</b> ..... 1 <b>3 Description</b> ..... 1 <b>4 Revision History</b> ..... 2 <b>5 Pin Configuration and Functions</b> ..... 3 <b>6 Specifications</b> ..... 4 6.1 Absolute Maximum Ratings ..... 4 6.2 Handling Ratings ..... 4 6.3 Recommended Operating Conditions <sup>(1)</sup> ..... 4 6.4 Thermal Information, 8-Pin ..... 4 6.5 Thermal Information, 14-Pin ..... 4 6.6 5.0V DC Electrical Characteristics ..... 5 6.7 5.0V AC Electrical Characteristics ..... 6 6.8 2.7V DC Electrical Characteristics ..... 6	6.9 2.7V AC Electrical Characteristics ..... 6 6.10 24V DC Electrical Characteristics ..... 7 6.11 24V AC Electrical Characteristics ..... 7 6.12 Typical Performance Characteristics ..... 8 <b>7 Application and Implementation</b> ..... 13 7.1 Application Information ..... 13 7.2 Enhanced Slew Rate ..... 13 7.3 Typical Applications ..... 17 <b>8 Device and Documentation Support</b> ..... 18 8.1 Related Links ..... 18 8.2 Trademarks ..... 18 8.3 Electrostatic Discharge Caution ..... 18 8.4 Glossary ..... 18 <b>9 Mechanical, Packaging, and Orderable Information</b> ..... 18
--	--

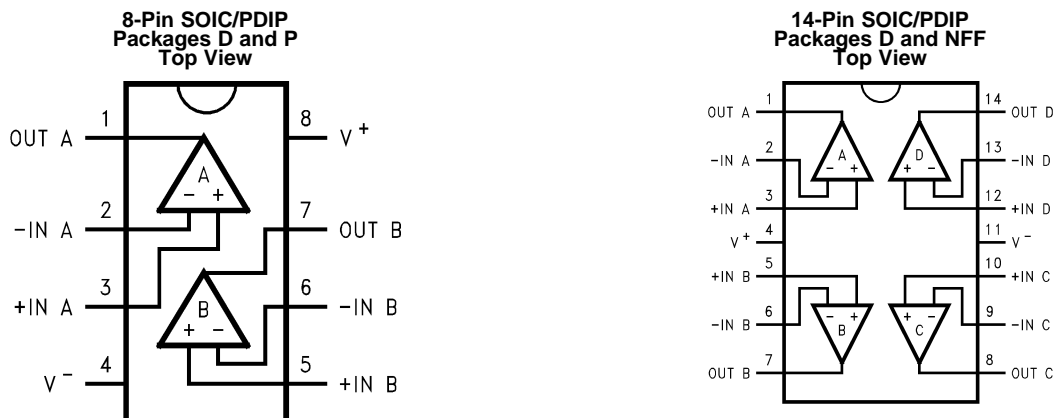
## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision D (February 2013) to Revision E</b>	<b>Page</b>
• Changed "Junction Temperature Range" to "Operating Temperature Range" and deleted "T <sub>J</sub> ".	4
• Deleted T <sub>J</sub> = 25°C for Electrical Characteristics tables.	5

<b>Changes from Revision C (February 2013) to Revision D</b>	<b>Page</b>
• Changed layout of National Data Sheet to TI format	17

## 5 Pin Configuration and Functions



### Pin Functions

NAME	PIN		I/O	DESCRIPTION
	LM6132 D/P	LM6134 D/NFF0014 A		
-IN A	2	2	I	ChA Inverting Input
+IN A	3	3	I	ChA Non-inverting Input
-IN B	6	6	I	ChB Inverting Input
+IN B	5	5	I	ChB Non-inverting Input
-IN C		9	I	ChC Inverting Input
+IN C		10	I	ChC Non-inverting Input
-IN D		13	I	ChD Inverting Input
+IN D		12	I	ChD Non-inverting Input
OUT A	1	1	O	ChA Output
OUT B	7	7	O	ChB Output
OUT C		8	O	ChC Output
OUT D		14	O	ChD Output
V-	4	11	I	Negative Supply
V+	8	4	I	Positive Supply

## 6 Specifications

### 6.1 Absolute Maximum Ratings<sup>(1)(2)</sup>

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Differential Input Voltage		±15	V
Voltage at Input/Output Pin		(V <sup>+</sup> )+0.3 (V <sup>-</sup> )-0.3	V
Supply Voltage (V <sup>+</sup> -V <sup>-</sup> )		35	V
Current at Input Pin		±10	mA
Current at Output Pin <sup>(3)</sup>		±25	mA
Current at Power Supply Pin		50	mA
Lead Temp. (soldering, 10 sec.)		260	°C
Junction Temperature <sup>(4)</sup>		150	°C

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical characteristics.
- (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
- (3) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.
- (4) The maximum power dissipation is a function of T<sub>J(MAX)</sub>, R<sub>θJA</sub>, and T<sub>A</sub>. The maximum allowable power dissipation at any ambient temperature is P<sub>D</sub> = (T<sub>J(MAX)</sub> - T<sub>A</sub>)/R<sub>θJA</sub>. All numbers apply for packages soldered directly into a PC board.

### 6.2 Handling Ratings

	MIN	MAX	UNIT
T <sub>stg</sub> Storage temperature range	-65	+150	°C
V <sub>(ESD)</sub> Electrostatic discharge Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>		2500	V

- (1) Human Body Model, 1.5 kΩ in series with 100 pF. JEDEC document JEP155 states that 2500-V HBM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Supply Voltage		1.8 ≤ V <sup>+</sup> ≤ 24	V
Operating Temperature Range: LM6132, LM6134	-40	+85	°C

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical characteristics.

### 6.4 Thermal Information, 8-Pin

THERMAL METRIC <sup>(1)</sup>	D (SOIC)	P (PDIP)	UNIT
	8 PINS	8 PINS	
R <sub>θJA</sub> Junction-to-ambient thermal resistance	193	115	°C/W

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

### 6.5 Thermal Information, 14-Pin

THERMAL METRIC <sup>(1)</sup>	D (SOIC)	NFF (PDIP)	UNIT
	14 PINS	14 PINS	
R <sub>θJA</sub> Junction-to-ambient thermal resistance	126	81	°C/W

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

## 6.6 5.0V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for  $V^+ = 5.0V$ ,  $V^- = 0V$ ,  $V_{CM} = V_O = V^+/2$  and  $R_L > 1\text{ M}\Omega$  to  $V^+/2$ . **Boldface** limits apply at the temperature extremes

PARAMETER	TEST CONDITIONS	TYP <sup>(1)</sup>	LM6134AI LM6132AI LIMIT <sup>(2)</sup>	LM6134BI LM6132BI LIMIT <sup>(2)</sup>	UNIT	
$V_{OS}$	Input Offset Voltage	0.25	2 4	6 8	mV max	
$TCV_{OS}$	Input Offset Voltage Average Drift	5			$\mu\text{V}/\text{C}$	
$I_B$	Input Bias Current	110	140 300	180 350	nA max	
$I_{OS}$	Input Offset Current	3.4	30 50	30 50	nA max	
$R_{IN}$	Input Resistance, CM	104			$\text{M}\Omega$	
CMRR	Common Mode Rejection Ratio	100	75 70	75 70	dB min	
			80	60 55		60 55
PSRR	Power Supply Rejection Ratio	82	78 75	78 75	dB min	
$V_{CM}$	Input Common-Mode Voltage Range	-0.25 5.25	0 5.0	0 5.0	V	
$A_V$	Large Signal Voltage Gain	100	25 8	15 6	V/mV min	
$V_O$	Output Swing	100k Load	4.992	4.98 4.93	4.98 4.93	V min
			0.007	0.017 0.019	0.017 0.019	V max
	10k Load	4.952	4.94 4.85	4.94 4.85	V min	
		0.032	0.07 0.09	0.07 0.09	V max	
	5k Load	4.923	4.90 4.85	4.90 4.85	V min	
		0.051	0.095 0.12	0.095 0.12	V max	
$I_{SC}$	Output Short Circuit Current LM6132	Sourcing	4	2 2	2 1	mA min
		Sinking	3.5	1.8 1.8	1.8 1	mA min
$I_{SC}$	Output Short Circuit Current LM6134	Sourcing	3	2 1.6	2 1	mA min
		Sinking	3.5	1.8 1.3	1.8 1	mA min
$I_S$	Supply Current	360	400 450	400 450	$\mu\text{A}$ max	

(1) Typical Values represent the most likely parametric normal.

(2) All limits are guaranteed by testing or statistical analysis.

## 6.7 5.0V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for  $V^+ = 5.0V$ ,  $V^- = 0V$ ,  $V_{CM} = V_O = V^+/2$  and  $R_L > 1\text{ M}\Omega$  to  $V^+/2$ . **Boldface** limits apply at the temperature extremes

PARAMETER		TEST CONDITIONS	TYP <sup>(1)</sup>	LM6134AI LM6132AI LIMIT <sup>(2)</sup>	LM6134BI LM6132BI LIMIT <sup>(2)</sup>	UNIT
SR	Slew Rate	$\pm 4V$ @ $V_S = \pm 6V$ $R_S < 1\text{ k}\Omega$	14	8 <b>7</b>	8 <b>7</b>	V/ $\mu$ s min
GBW	Gain-Bandwidth Product	$f = 20\text{ kHz}$	10	7.4 <b>7</b>	7.4 <b>7</b>	MHz min
$\theta_m$	Phase Margin	$R_L = 10k$	33			deg
$G_m$	Gain Margin	$R_L = 10k$	10			dB
$e_n$	Input Referred Voltage Noise	$f = 1\text{ kHz}$	27			nV/ $\sqrt{\text{Hz}}$
$i_n$	Input Referred Current Noise	$f = 1\text{ kHz}$	0.18			pA/ $\sqrt{\text{Hz}}$

(1) Typical Values represent the most likely parametric normal.

(2) All limits are guaranteed by testing or statistical analysis.

## 6.8 2.7V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for  $V^+ = 2.7V$ ,  $V^- = 0V$ ,  $V_{CM} = V_O = V^+/2$  and  $R_L > 1\text{ M}\Omega$  to  $V^+/2$ . **Boldface** limits apply at the temperature extreme

PARAMETER		TEST CONDITIONS	TYP <sup>(1)</sup>	LM6134AI LM6132AI LIMIT <sup>(2)</sup>	LM6134BI LM6132BI LIMIT <sup>(2)</sup>	UNIT
$V_{OS}$	Input Offset Voltage		0.12	2 <b>8</b>	6 <b>12</b>	mV max
$I_B$	Input Bias Current	$0V \leq V_{CM} \leq 2.7V$	90			nA
$I_{OS}$	Input Offset Current		2.8			nA
$R_{IN}$	Input Resistance		134			M $\Omega$
CMRR	Common Mode Rejection Ratio	$0V \leq V_{CM} \leq 2.7V$	82			dB
PSRR	Power Supply Rejection Ratio	$\pm 1.35V \leq V^+ \leq \pm 12V$	80			dB
$V_{CM}$	Input Common-Mode Voltage Range			2.7 0	2.7 0	V
$A_V$	Large Signal Voltage Gain	$R_L = 10k$	100			V/mV
$V_O$	Output Swing	$R_L = 100k$	0.03	0.08 <b>0.112</b>	0.08 <b>0.112</b>	V max
			2.66	2.65 <b>2.25</b>	2.65 <b>2.25</b>	V min
$I_S$	Supply Current	Per Amplifier	330			$\mu$ A

(1) Typical Values represent the most likely parametric normal.

(2) All limits are guaranteed by testing or statistical analysis.

## 6.9 2.7V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for  $V^+ = 2.7V$ ,  $V^- = 0V$ ,  $V_{CM} = V_O = V^+/2$  and  $R_L > 1\text{ M}\Omega$  to  $V^+/2$ .

PARAMETER		TEST CONDITIONS	TYP <sup>(1)</sup>	LM6134AI LM6132AI LIMIT <sup>(2)</sup>	LM6134BI LM6132BI LIMIT <sup>(2)</sup>	UNIT
GBW	Gain-Bandwidth Product	$R_L = 10k$ , $f = 20\text{ kHz}$	7			MHz
$\theta_m$	Phase Margin	$R_L = 10k$	23			deg
$G_m$	Gain Margin		12			dB

(1) Typical Values represent the most likely parametric normal.

(2) All limits are guaranteed by testing or statistical analysis.

## 6.10 24V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for  $V^+ = 24V$ ,  $V^- = 0V$ ,  $V_{CM} = V_O = V^+/2$  and  $R_L > 1\text{ M}\Omega$  to  $V^+/2$ . **Boldface** limits apply at the temperature extreme

PARAMETER		TEST CONDITIONS	TYP <sup>(1)</sup>	LM6134AI LM6132AI LIMIT <sup>(2)</sup>	LM6134BI LM6132BI LIMIT <sup>(2)</sup>	UNIT
$V_{OS}$	Input Offset Voltage		1.7	3 <b>5</b>	7 <b>9</b>	mV max
$I_B$	Input Bias Current	$0V \leq V_{CM} \leq 24V$	125			nA
$I_{OS}$	Input Offset Current		4.8			nA
$R_{IN}$	Input Resistance		210			M $\Omega$
CMRR	Common Mode Rejection Ratio	$0V \leq V_{CM} \leq 24V$	80			dB
PSRR	Power Supply Rejection Ratio	$2.7V \leq V^+ \leq 24V$	82			dB
$V_{CM}$	Input Common-Mode Voltage Range		-0.25 24.25	0 24	0 24	V min V max
$A_V$	Large Signal Voltage Gain	$R_L = 10k$	102			V/mV
$V_O$	Output Swing	$R_L = 10k$	0.075 23.86	0.15 23.8	0.15 23.8	V max V min
$I_S$	Supply Current	Per Amplifier	390	450 <b>490</b>	450 <b>490</b>	$\mu$ A max

(1) Typical Values represent the most likely parametric normal.

(2) All limits are guaranteed by testing or statistical analysis.

## 6.11 24V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for  $V^+ = 24V$ ,  $V^- = 0V$ ,  $V_{CM} = V_O = V^+/2$  and  $R_L > 1\text{ M}\Omega$  to  $V^+/2$ .

PARAMETER		TEST CONDITIONS	TYP <sup>(1)</sup>	LM6134AI LM6132AI LIMIT <sup>(2)</sup>	LM6134BI LM6132BI LIMIT <sup>(2)</sup>	UNIT
GBW	Gain-Bandwidth Product	$R_L = 10k$ , $f = 20\text{ kHz}$	11			MHz
$\theta_m$	Phase Margin	$R_L = 10k$	23			deg
$G_m$	Gain Margin	$R_L = 10k$	12			dB
THD + N	Total Harmonic Distortion and Noise	$A_V = +1$ , $V_O = 20V_{P-P}$ $f = 10\text{ kHz}$	0.0015%			

(1) Typical Values represent the most likely parametric normal.

(2) All limits are guaranteed by testing or statistical analysis.

## 6.12 Typical Performance Characteristics

$T_A = 25^\circ\text{C}$ ,  $R_L = 10\text{ k}\Omega$  unless otherwise specified

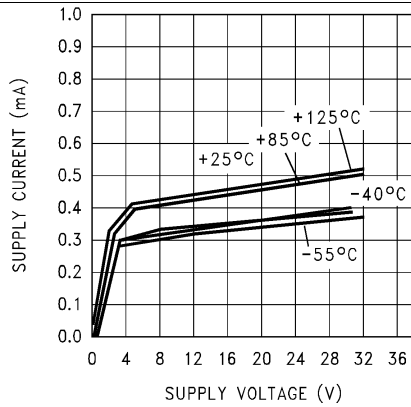


Figure 1. Supply Current vs. Supply Voltage

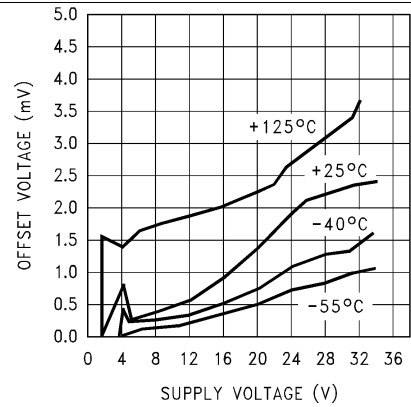


Figure 2. Offset Voltage vs. Supply Voltage

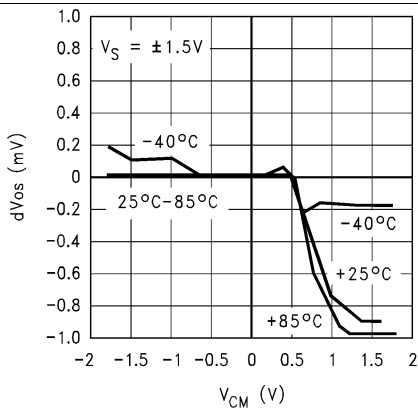


Figure 3.  $dV_{OS}$  vs.  $V_{CM}$

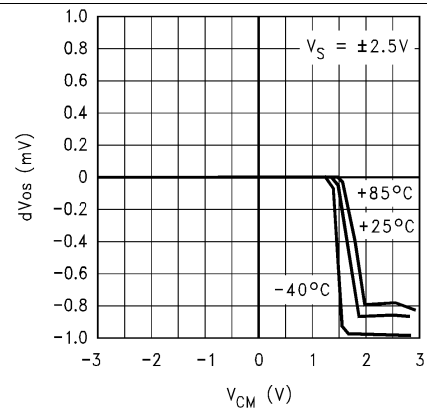


Figure 4.  $dV_{OS}$  vs.  $V_{CM}$

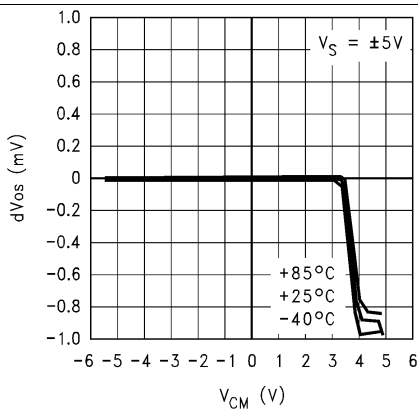


Figure 5.  $dV_{OS}$  vs.  $V_{CM}$

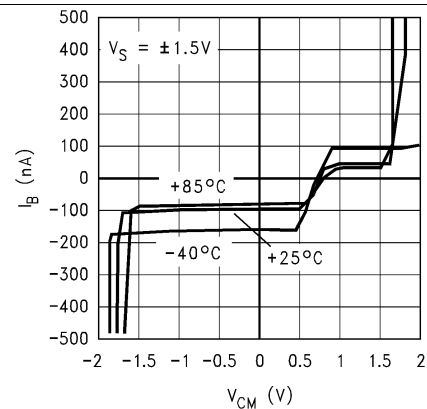


Figure 6.  $I_{BIAS}$  vs.  $V_{CM}$



Typical Performance Characteristics (continued)

$T_A = 25^\circ\text{C}$ ,  $R_L = 10\text{ k}\Omega$  unless otherwise specified

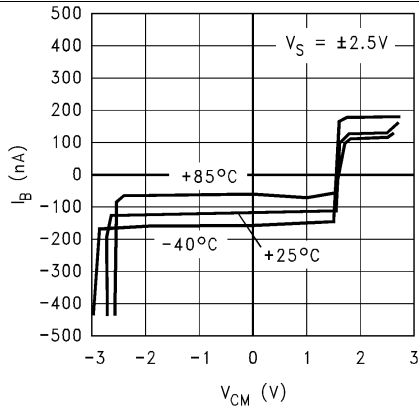


Figure 7.  $I_{BIAS}$  vs.  $V_{CM}$

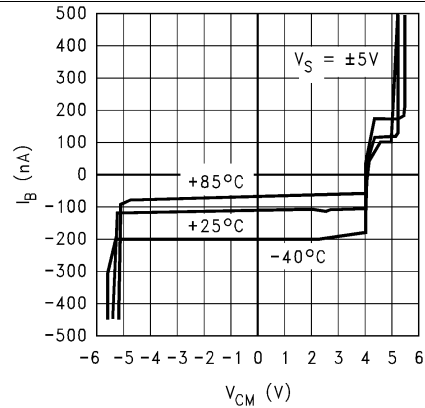


Figure 8.  $I_{BIAS}$  vs.  $V_{CM}$

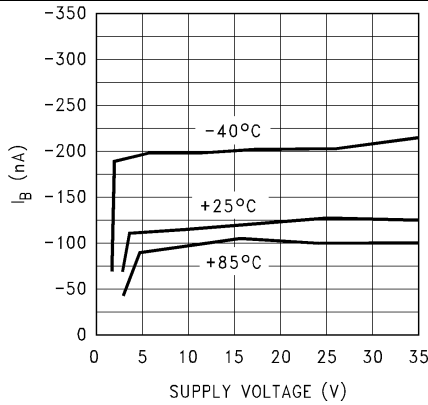


Figure 9. Input Bias Current vs. Supply Voltage

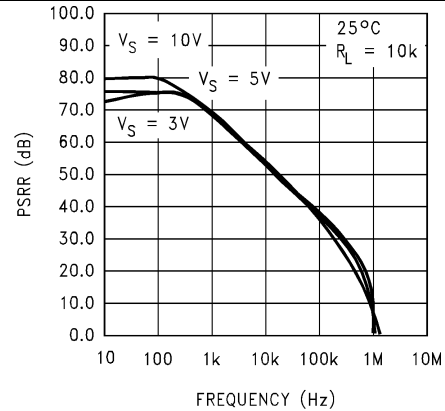


Figure 10. Negative PSRR vs. Frequency

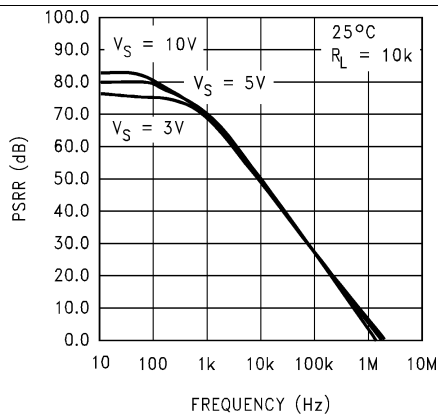


Figure 11. Positive PSRR vs. Frequency

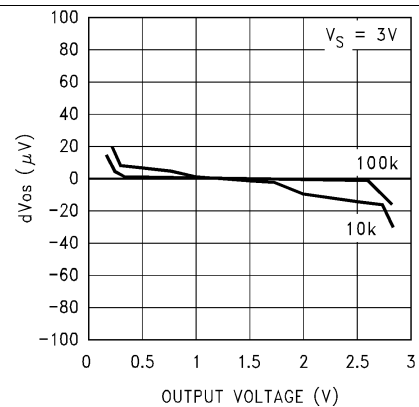
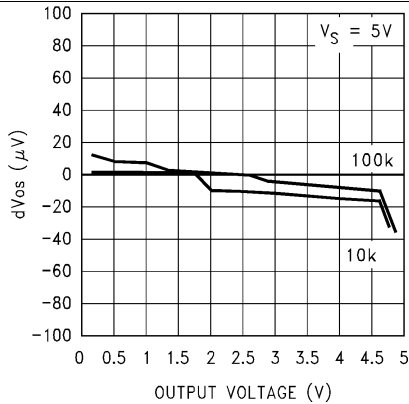
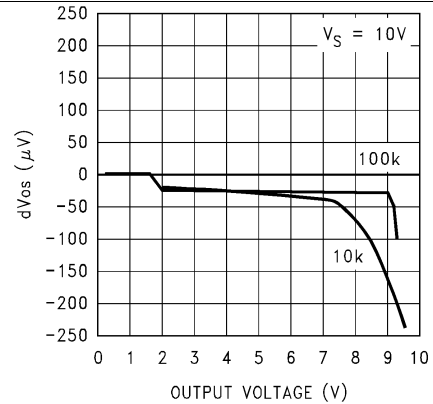
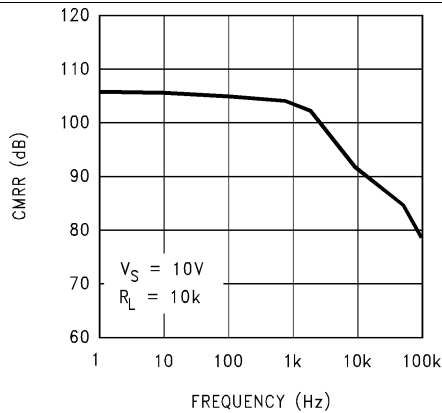
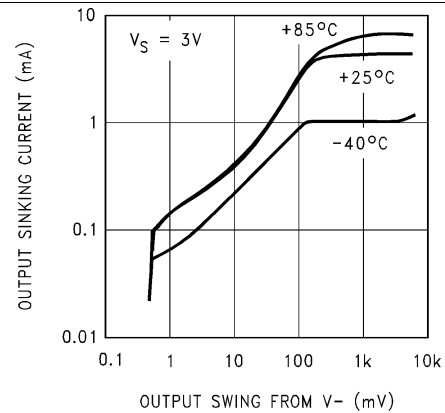
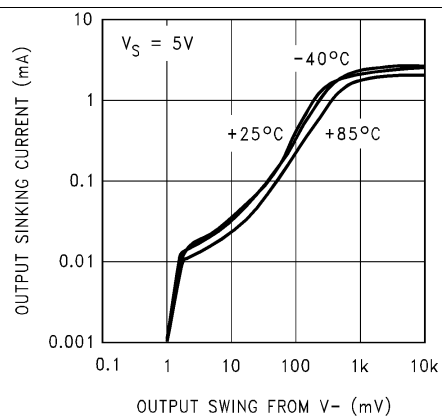
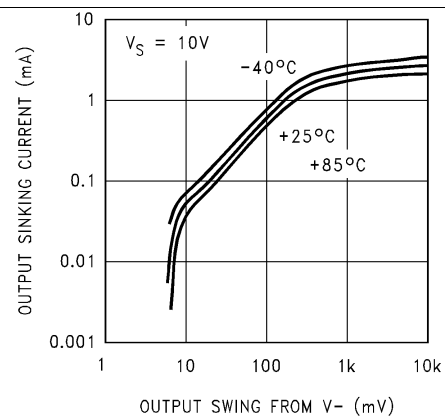


Figure 12.  $dV_{OS}$  vs. Output Voltage

**Typical Performance Characteristics (continued)**
 $T_A = 25^\circ\text{C}$ ,  $R_L = 10\text{ k}\Omega$  unless otherwise specified

**Figure 13.  $dV_{OS}$  vs. Output Voltage**

**Figure 14.  $dV_{OS}$  vs. Output Voltage**

**Figure 15. CMRR vs. Frequency**

**Figure 16. Output Voltage vs. Sinking Current**

**Figure 17. Output Voltage vs. Sinking Current**

**Figure 18. Output Voltage vs. Sinking Current**

Typical Performance Characteristics (continued)

$T_A = 25^\circ\text{C}$ ,  $R_L = 10\text{ k}\Omega$  unless otherwise specified

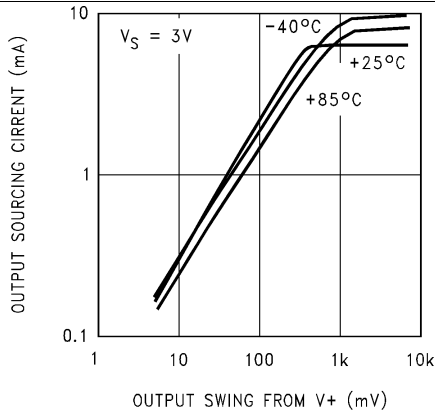


Figure 19. Output Voltage vs. Sourcing Current

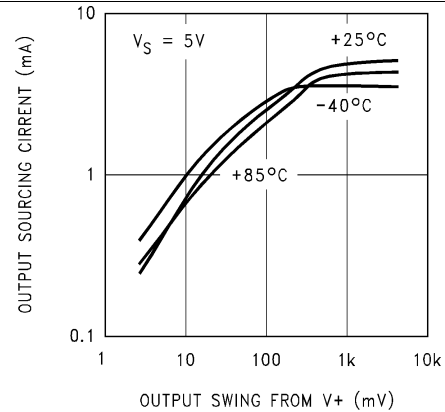


Figure 20. Output Voltage vs. Sourcing Current

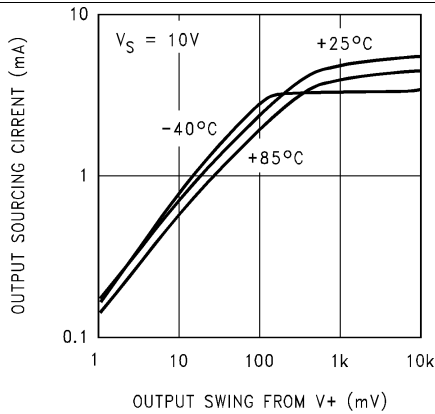


Figure 21. Output Voltage vs. Sourcing Current

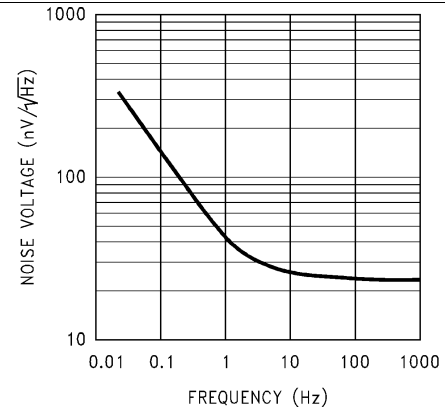


Figure 22. Noise Voltage vs. Frequency

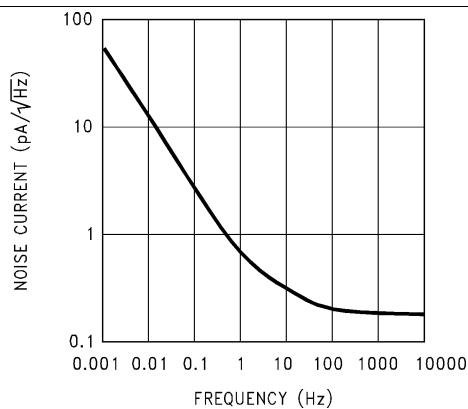


Figure 23. Noise Current vs. Frequency

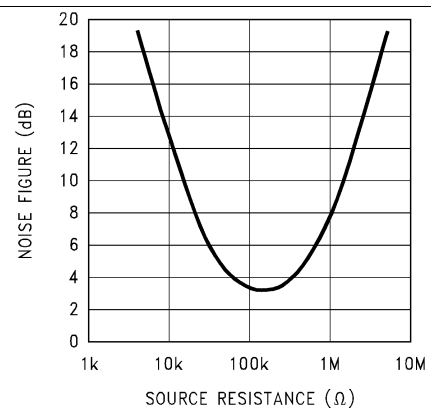
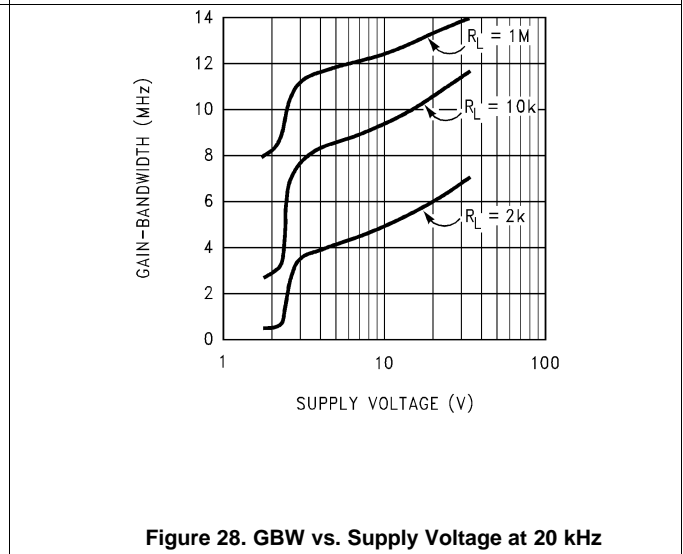
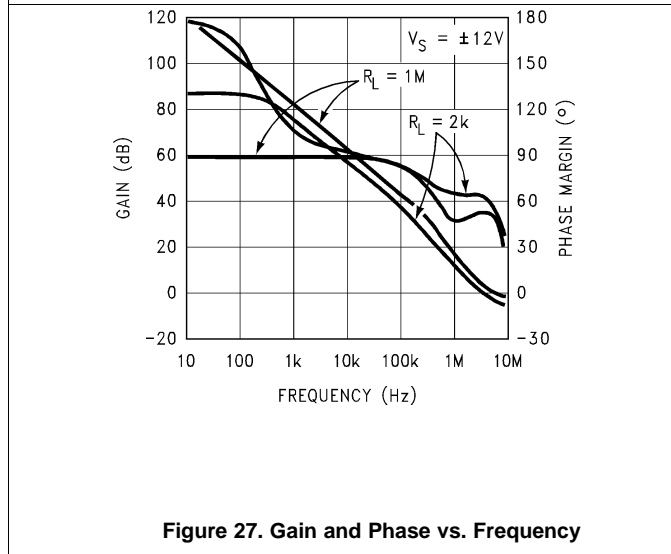
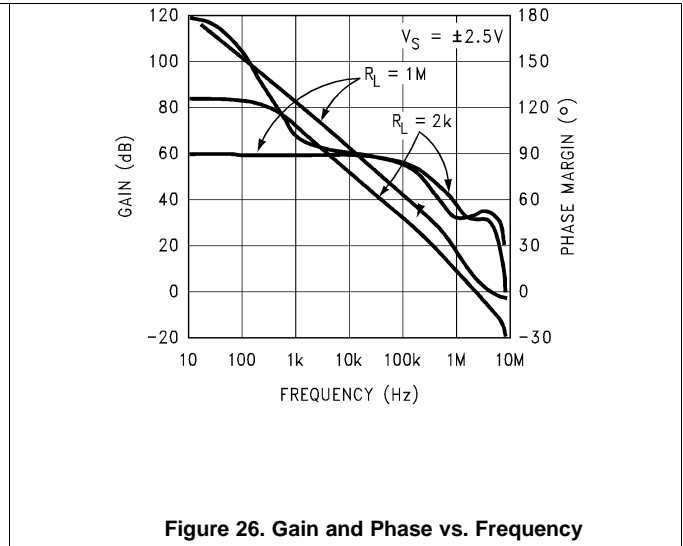
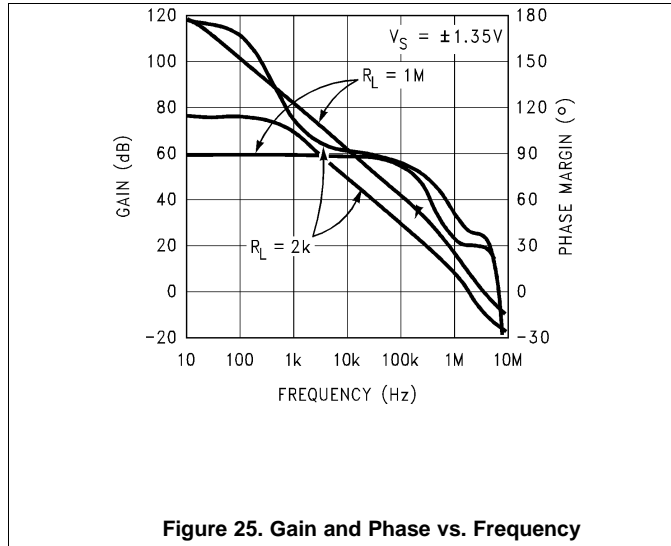


Figure 24. NF vs. Source Resistance

Typical Performance Characteristics (continued)

$T_A = 25^\circ\text{C}$ ,  $R_L = 10\text{ k}\Omega$  unless otherwise specified



## 7 Application and Implementation

### 7.1 Application Information

The LM6132 brings a new level of ease of use to op amp system design. Greater than rail-to-rail input voltage eliminates concern over exceeding the common-mode voltage range.

Rail-to-rail output swing provides the maximum possible dynamic range at the output. This is particularly important when operating on low supply voltages.

The high gain-bandwidth with low supply current opens new battery powered applications, where high power consumption previously reduced battery life to unacceptable levels.

To take advantage of these features, some ideas should be kept in mind, which are outlined in subsequent sections.

### 7.2 Enhanced Slew Rate

Unlike most bipolar op amps, the unique phase reversal prevention/speed-up circuit in the input stage eliminates phase reversal and allows the slew rate to be a function of the input signal amplitude.

Figure 30 shows how excess input signal is routed around the input collector-base junctions directly to the current mirrors.

The LM6132/34 input stage converts the input voltage change to a current change. This current change drives the current mirrors through the collectors of Q1–Q2, Q3–Q4 when the input levels are normal.

If the input signal exceeds the slew rate of the input stage and the differential input voltage rises above a diode drop, the excess signal bypasses the normal input transistors, (Q1–Q4), and is routed in correct phase through the two additional transistors, (Q5, Q6), directly into the current mirrors.

The rerouting of excess signal allows the slew-rate to increase by a factor of 10 to 1 or more. (See Figure 29).

As the overdrive increases, the op amp reacts better than a conventional op amp. Large fast pulses will raise the slew rate to around 25V to 30 V/ $\mu$ s.

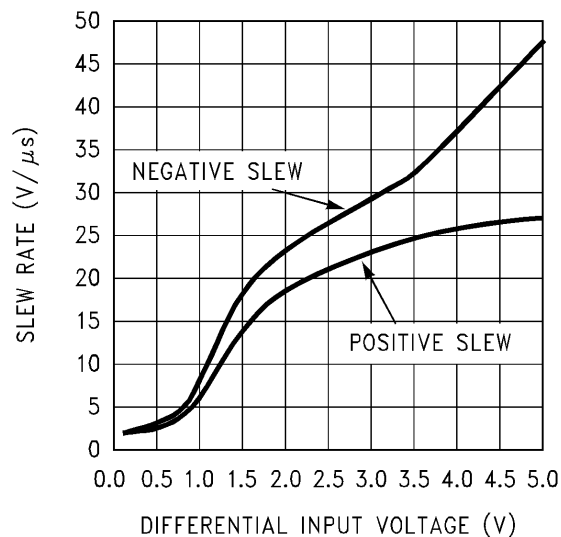


Figure 29. Slew Rate vs. Differential  $V_{IN}$   
 $V_S = \pm 12V$

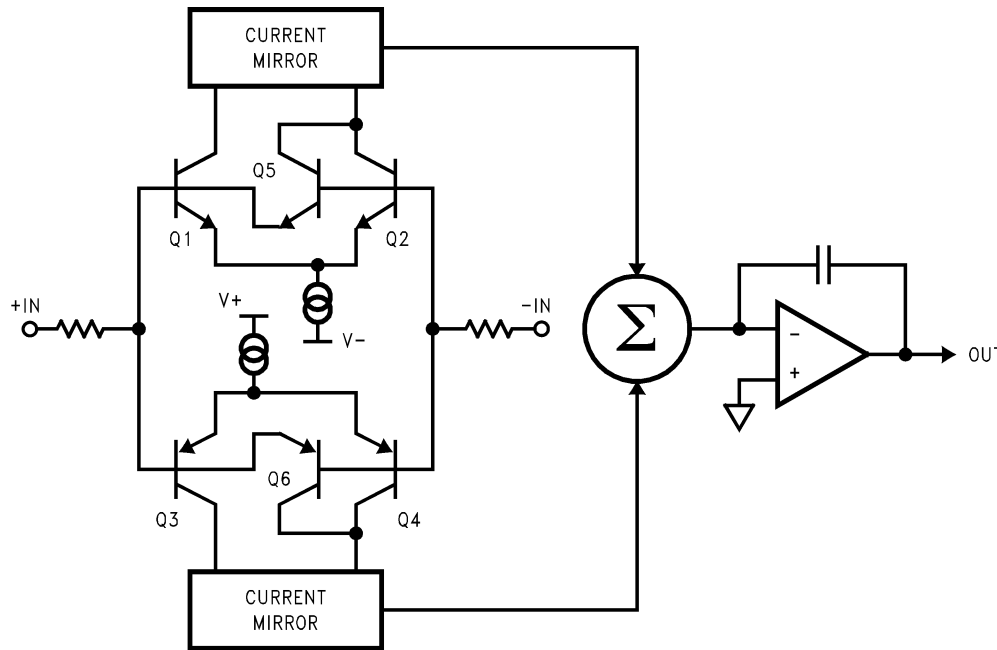
This effect is most noticeable at higher supply voltages and lower gains where incoming signals are likely to be large.

This speed-up action adds stability to the system when driving large capacitive loads.

## Enhanced Slew Rate (continued)

### 7.2.1 Driving Capacitive Loads

Capacitive loads decrease the phase margin of all op amps. This is caused by the output resistance of the amplifier and the load capacitance forming an R-C phase lag network. This can lead to overshoot, ringing and oscillation. Slew rate limiting can also cause additional lag. Most op amps with a fixed maximum slew-rate will lag further and further behind when driving capacitive loads even though the differential input voltage raises. With the LM6132, the lag causes the slew rate to raise. The increased slew-rate keeps the output following the input much better. This effectively reduces phase lag. After the output has caught up with the input, the differential input voltage drops down and the amplifier settles rapidly.



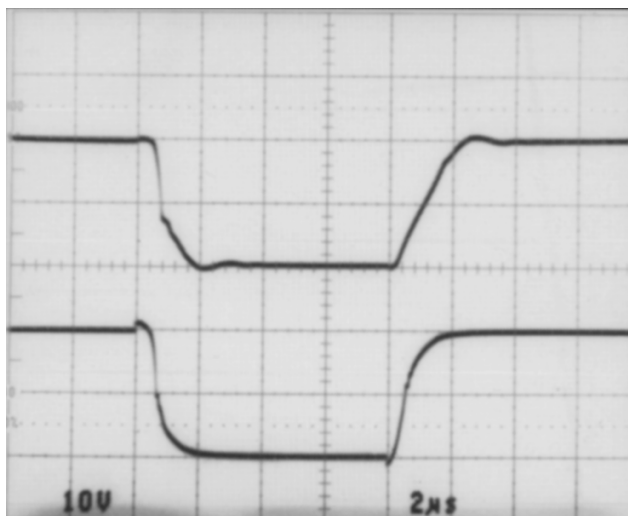
**Figure 30. Internal Block Diagram**

### Enhanced Slew Rate (continued)

These features allow the LM6132 to drive capacitive loads as large as 500 pF at unity gain and not oscillate. The scope photos (Figure 31 and Figure 32) show the LM6132 driving a 500 pF load. In Figure 31, the lower trace is with no capacitive load and the upper trace is with a 500 pF load. Here we are operating on  $\pm 12\text{V}$  supplies with a 20 V<sub>PP</sub> pulse. Excellent response is obtained with a C<sub>F</sub> of 39 pF. In Figure 32, the supplies have been reduced to  $\pm 2.5\text{V}$ , the pulse is 4 V<sub>PP</sub> and C<sub>F</sub> is 39 pF. The best value for the compensation capacitor should be established after the board layout is finished because the value is dependent on board stray capacity, the value of the feedback resistor, the closed loop gain and, to some extent, the supply voltage.

Another effect that is common to all op amps is the phase shift caused by the feedback resistor and the input capacitance. This phase shift also reduces phase margin. This effect is taken care of at the same time as the effect of the capacitive load when the capacitor is placed across the feedback resistor.

The circuit shown in Figure 33 was used for Figure 31 and Figure 32.



**Figure 31. Twenty-Volt Step Response:  
with Cap Load (Top Trace)  
without Cap Load (Bottom Trace)**



**Figure 32. Four-Volt Step Response:  
with Cap Load (Top Trace)  
without Cap Load (Bottom Trace)**

Enhanced Slew Rate (continued)

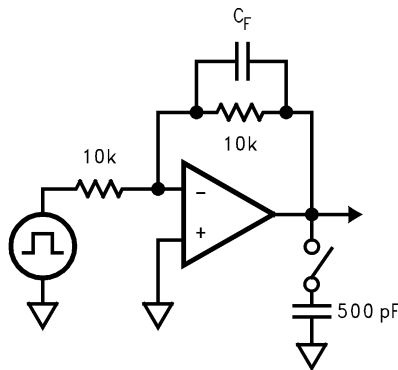


Figure 33. Cap Load Test Circuit

Figure 34 shows a method for compensating for load capacitance ( $C_O$ ) effects by adding both an isolation resistor  $R_O$  at the output and a feedback capacitor  $C_F$  directly between the output and the inverting input pin. Feedback capacitor  $C_F$  compensates for the pole introduced by  $R_O$  and  $C_O$ , minimizing ringing in the output waveform while the feedback resistor  $R_F$  compensates for dc inaccuracies introduced by  $R_O$ . Depending on the size of the load capacitance, the value of  $R_O$  is typically chosen to be between 100  $\Omega$  to 1 k $\Omega$ .

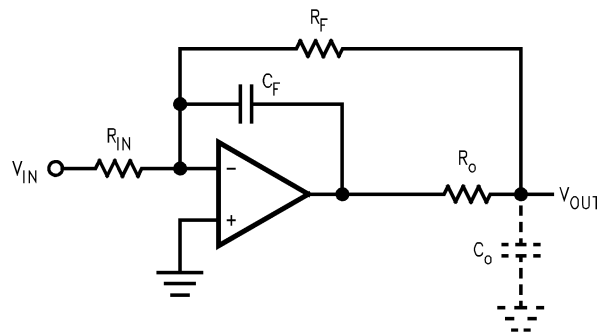


Figure 34. Capacitive Loading Compensation Technique



## 7.3 Typical Applications

### 7.3.1 Three Op Amp Instrumentation Amp with Rail-to-Rail Input and Output

Using the LM6134, a 3 op amp instrumentation amplifier with rail-to-rail inputs and rail to rail output can be made. These features make these instrumentation amplifiers ideal for single supply systems.

Some manufacturers use a precision voltage divider array of 5 resistors to divide the common-mode voltage to get an input range of rail-to-rail or greater. The problem with this method is that it also divides the signal, so to even get unity gain, the amplifier must be run at high closed loop gains. This raises the noise and drift by the internal gain factor and lowers the input impedance. Any mismatch in these precision resistors reduces the CMR as well. Using the LM6134, all of these problems are eliminated.

In this example, amplifiers A and B act as buffers to the differential stage (Figure 35). These buffers assure that the input impedance is over 100 M $\Omega$  and they eliminate the requirement for precision matched resistors in the input stage. They also assure that the difference amp is driven from a voltage source. This is necessary to maintain the CMR set by the matching of R1–R2 with R3–R4.

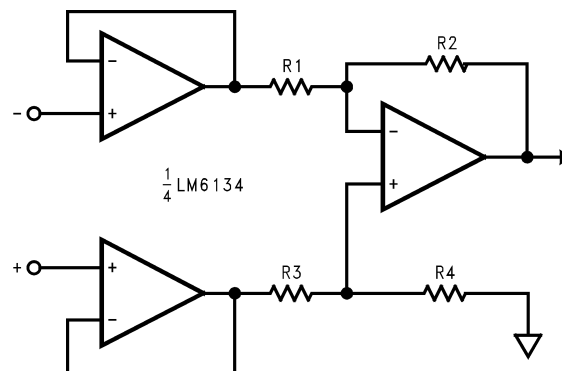


Figure 35. Instrumentation Amplifier

### 7.3.2 Flat Panel Display Buffering

Three features of the LM6132/34 make it a superb choice for TFT LCD applications. First, its low current draw (360  $\mu$ A per amplifier at 5 V) makes it an ideal choice for battery powered applications such as in laptop computers. Second, since the device operates down to 2.7 V, it is a natural choice for next generation 3V TFT panels. Last, but not least, the large capacitive drive capability of the LM6132 comes in very handy in driving highly capacitive loads that are characteristic of LCD display drivers.

The large capacitive drive capability of the LM6132/34 allows it to be used as buffers for the gamma correction reference voltage inputs of resistor-DAC type column (Source) drivers in TFT LCD panels. This amplifier is also useful for buffering only the center reference voltage input of Capacitor-DAC type column (Source) drivers such as the LMC750X series.

Since for VGA and SVGA displays, the buffered voltages must settle within approximately 4  $\mu$ s, the well known technique of using a small isolation resistor in series with the amplifier's output very effectively dampens the ringing at the output.

With its wide supply voltage range of 2.7 V to 24 V, the LM6132/34 can be used for a diverse range of applications. The system designer is thus able to choose a single device type that serves many sub-circuits in the system, eliminating the need to specify multiple devices in the bill of materials. Along with its sister parts, the LM6142 and LM6152 that have the same wide supply voltage capability, choice of the LM6132 in a design eliminates the need to search for multiple sources for new designs.

## 8 Device and Documentation Support

### 8.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 1. Related Links**

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LM6132	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
LM6134	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>

### 8.2 Trademarks

All trademarks are the property of their respective owners.

### 8.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 8.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM6132AIM/NOPB	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 85	LM6132AIM	
LM6132AIMX/NOPB	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LM6132AIM	Samples
LM6132BIMX/NOPB	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LM6132BIM	Samples
LM6132BIN/NOPB	ACTIVE	PDIP	P	8	40	RoHS & Green	NIPDAU	Level-1-NA-UNLIM	-40 to 85	LM6132BIN	Samples
LM6134AIM/NOPB	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	-40 to 85	LM6134AIM	
LM6134AIMX/NOPB	ACTIVE	SOIC	D	14	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LM6134AIM	Samples
LM6134BIM/NOPB	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	-40 to 85	LM6134BIM	
LM6134BIMX/NOPB	ACTIVE	SOIC	D	14	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LM6134BIM	Samples
LM6134BIN/NOPB	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	Level-1-NA-UNLIM	-40 to 85	LM6134BIN	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM6132AIMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM6132BIMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM6134AIMX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
LM6134BIMX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM6132AIMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM6132BIMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM6134AIMX/NOPB	SOIC	D	14	2500	367.0	367.0	35.0
LM6134BIMX/NOPB	SOIC	D	14	2500	367.0	367.0	35.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
LM6132BIN/NOPB	P	PDIP	8	40	502	14	11938	4.32
LM6134BIN/NOPB	N	PDIP	14	25	502	14	11938	4.32

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - $\triangle D$  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AB.





D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed  $.006$  [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MS-001 variation BA.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2024, Texas Instruments Incorporated