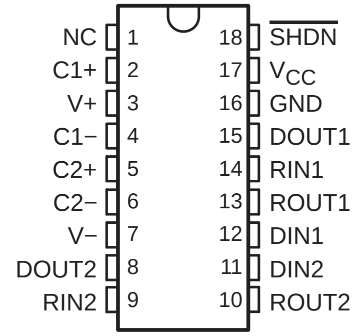
- **ESD Protection for RS-232 Bus Pins**
  - **±15-kV Human-Body Model**
- **Meets or Exceeds the Requirements of TIA/EIA-232-F and ITU v.28 Standards**
- **Operates at 5-V V_{CC} Supply**
- **Operates Up To 200 kbit/s**
- **Low Supply Current in Shutdown Mode . . . 2 µA Typical**
- **External Capacitors . . . 4 × 0.1 µF**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **Applications**
  - **Battery-Powered Systems, PDAs, Notebooks, Laptops, Palmtop PCs, and Hand-Held Equipment**

DW OR N PACKAGE
(TOP VIEW)



description/ordering information

The MAX222 consists of two line drivers, two line receivers, and a dual charge-pump circuit with ±15-kV ESD protection pin to pin (serial-port connection pins, including GND). This device meets the requirements of TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 5-V supply. This device operates at data signaling rates up to 200 kbit/s and a maximum of 30-V/µs driver output slew rate. By using $\overline{\text{SHDN}}$, all receivers can be disabled.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP (N)	Tube of 20	MAX222CN	MAX222CN
	SOIC (DW)	Tube of 20	MAX222CDW	MAX222C
		Reel of 1000	MAX222CDWR	
−40°C to 85°C	PDIP (N)	Tube of 20	MAX222IN	MAX222IN
	SOIC (DW)	Tube of 20	MAX222IDW	MAX222I
		Reel of 1000	MAX222IDWR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Function Tables

EACH DRIVER

INPUT D_{IN}	OUTPUT D_{OUT}
L	H
H	L

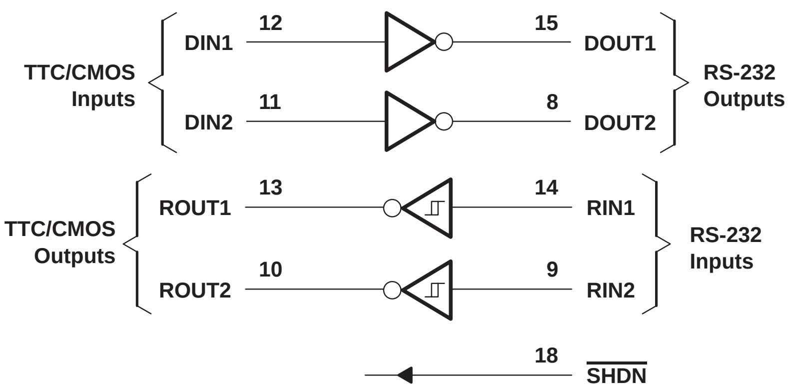
H = high level, L = low level

EACH RECEIVER

INPUT R_{IN}	OUTPUT R_{OUT}
L	H
H	L
Open	H

H = high level, L = low level, Open = input disconnected or connected driver off

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1)		−0.3 V to 6 V
Input voltage range, V_I:	Drivers	−0.3 V to V_{CC} − 0.3 V
	Receivers	±30 V
Output voltage range, V_O:	Drivers	±15 V
	Receivers	−0.3 V to V_{CC} + 0.3 V
Short-circuit duration, D_{OUT}		Continuous
Package thermal impedance, θ_{JA} (see Notes 2 and 3):	DW package	TBD°C/W
	N package	TBD°C/W
Operating virtual junction temperature, T_J		150°C
Storage temperature range, T_{stg}		−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. All voltages are with respect to network GND.
2. Maximum power dissipation is a function of T_J(max), θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) − T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 4 and Figure 4)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	Driver high-level input voltage	D_{IN}	2			V
	Shutdown high-level input voltage	$\overline{SHDN}$	2			V
V_{IL}	Driver low-level input voltage	D_{IN}			0.8	V
	Shutdown low-level input voltage	$\overline{SHDN}$			0.8	V
V_I	Driver input voltage	D_{IN}	0		5.5	V
	Receiver input voltage		−30		30	
T_A	Operating free-air temperature	MAX222C	0		70	°C
		MAX222I	−40		85	

NOTE 4: Test conditions are C1−C4 = 0.1 µF at V_{CC} = 5 V ± 0.5 V.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 4)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
I_{CC}	Supply current	V_{CC} = 5 V	$\overline{SHDN}$ = V_{CC}	No load		4	10	mA
				3 kΩ on both inputs		15		
	Shutdown supply current					2	50	µA
$\overline{SHDN}$	Shutdown input leakage current						±1	µA

NOTE 4: Test conditions are C1−C4 = 0.1 µF at V_{CC} = 5 V ± 0.5 V.

DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 4)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	DOUT at R_L = 3 kΩ to GND,	D_{IN} = GND	5	8		V
V_{OL}	Low-level output voltage	DOUT at R_L = 3 kΩ to GND,	D_{IN} = V_{CC}	−5	−8		V
I_{IH}	Driver high-level input current	DIN = V_{CC}			5	40	μA
	Control high-level input current	$\overline{SHDN}$ = V_{CC}			0.01	1	
I_{IL}	Driver low-level input current	DIN = 0 V			−5	−40	μA
	Control low-level input current	$\overline{SHDN}$ = 0 V			−0.01	−1	
I_{OS}‡	Short-circuit output current	V_{CC} = 5.5 V,	V_O = 0 V	±7	±22		mA
I_{off}	Output leakage current	V_{CC} = 5.5 V, $\overline{SHDN}$ = GND,	V_O = ±10 V		±0.01	±10	μA
r_o	Output resistance	V_{CC}, V+, and V− = 0 V,	V_O = ±2 V	300	10 M		Ω

† All typical values are at V_{CC} = 5 V, and T_A = 25°C.
‡ Short-circuit durations should be controlled to prevent exceeding the device absolute power-dissipation ratings, and not more than one output should be shorted at a time.
NOTE 4: Test conditions are C1−C4 = 0.1 μF at V_{CC} = 5 V ± 0.5 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 4)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
	Data rate	C_L = 1000 pF, One D_{OUT} switching,	R_L = 3 kΩ, See Figure 1	200			kbit/s
t_{PLH} (D)	Propagation delay time, low- to high-level output	See Figure 1			1.5	3.5	μs
t_{PHL} (D)	Propagation delay time, high- to low-level output	See Figure 1			1.3	3.5	μs
t_{PHL} (D) − t_{PLH} (D)	Driver (+ to −) propagation delay difference				300		ns
$t_{sk(p)}$	Pulse skew§	C_L = 150 pF to 2500 pF	R_L = 3 kΩ to 7 kΩ, See Figure 2		300		ns
SR(tr)	Slew rate, transition region (see Figure 1)	R_L = 3 kΩ to 7 kΩ, V_{CC} = 5 V	C_L = 50 pF to 2500 pF	6	12	30	V/μs
t_{ET}	Driver output enable time (after $\overline{SHDN}$ goes high)				250		μs
t_{DT}	Driver output disable time (after $\overline{SHDN}$ goes low)				300		ns

† All typical values are at V_{CC} = 5 V and T_A = 25°C.
§ Pulse skew is defined as $|t_{PLH} − t_{PHL}|$ of each channel of the same device.
NOTE 4: Test conditions are C1−C4 = 0.1 μF at V_{CC} = 5 V ± 0.5 V.

RECEIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 4)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −1 mA	3.5	V_{CC} − 0.2 V		V
V_{OL}	Low-level output voltage	I_{OL} = 3.2 mA			0.4	V
V_{IT+}	Positive-going input threshold voltage	V_{CC} = 5 V		1.7	2.4	V
V_{IT-}	Negative-going input threshold voltage	V_{CC} = 5 V	0.8	1.3		V
V_{hys}	Input hysteresis (V_{IT+} − V_{IT-})		0.2	0.5	1	V
r_i	Input resistance	V_I = ±3 V to ±25 V	3	5	7	kΩ

† All typical values are at V_{CC} = 5 V, and T_A = 25°C.
NOTE 4: Test conditions are C1−C4 = 0.1 µF at V_{CC} = 5 V ± 0.5 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 3)

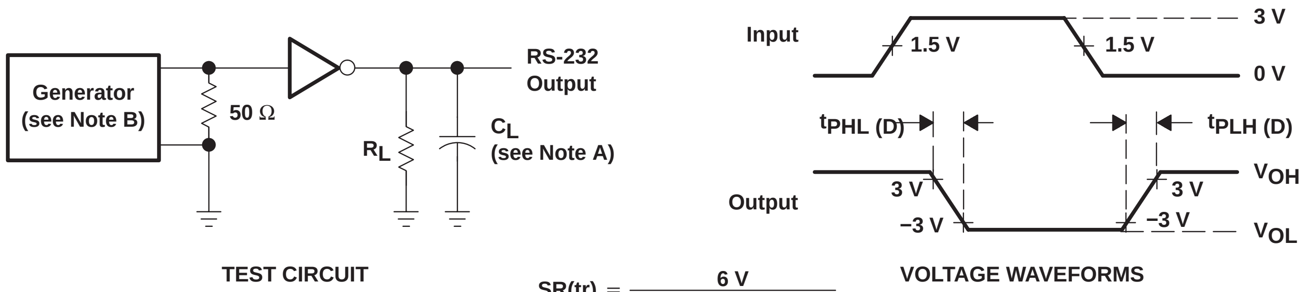
PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH} (R)	Propagation delay time, low- to high-level output	C_L= 150 pF		0.6	1	µs
t_{PHL} (R)	Propagation delay time, high- to low-level output	C_L= 150 pF		0.5	1	µs
t_{PHL} (R) − t_{PLH} (R)	Receiver (+ to −) propagation delay difference			100		ns
$t_{sk(p)}$	Pulse skew‡			100		ns

† All typical values are at V_{CC} = 5 V and T_A = 25°C.
‡ Pulse skew is defined as $|t_{PLH} − t_{PHL}|$ of each channel of the same device.
NOTE 4: Test conditions are C1−C4 = 0.1 µF, at V_{CC} = 5 V ± 0.5 V.

ESD protection

PIN	TEST CONDITIONS	TYP	UNIT
D_{OUT}, R_{IN}	Human-Body Model	±15	kV

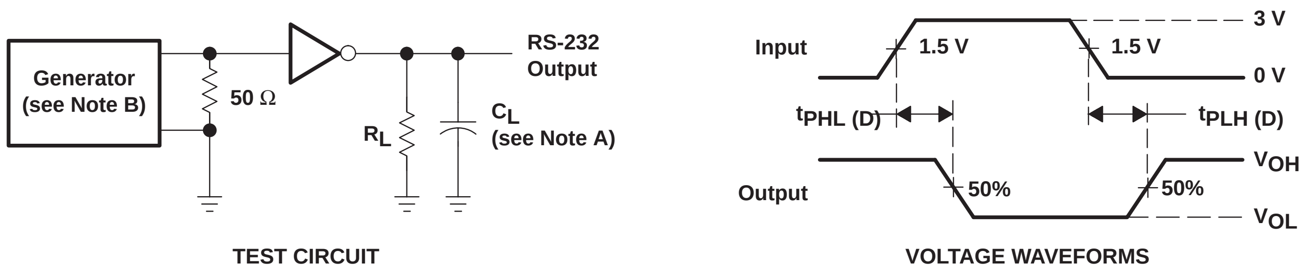
PARAMETER MEASUREMENT INFORMATION



$$SR(tr) = \frac{6\ V}{t_{PHL\ (D)}\ \text{or}\ t_{PLH\ (D)}}$$

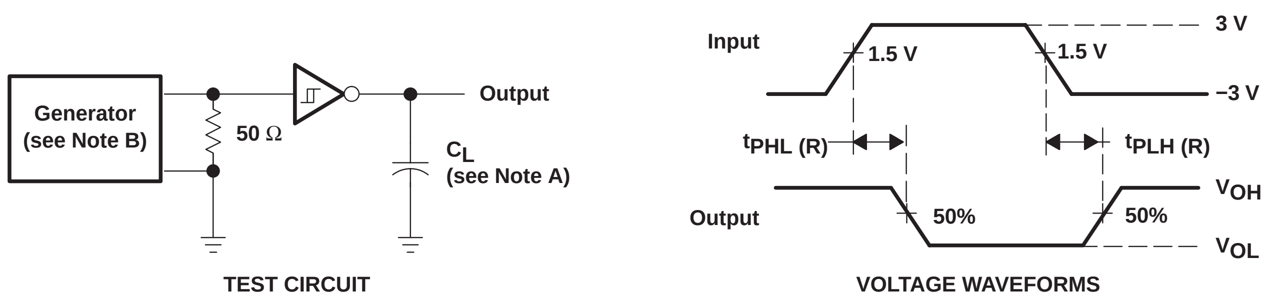
NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 250 kbit/s, Z_O = 50 Ω, 50% duty cycle, $t_r \leq 10$ ns, $t_f \leq 10$ ns.

Figure 1. Driver Slew Rate



NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 250 kbit/s, Z_O = 50 Ω, 50% duty cycle, $t_r \leq 10$ ns, $t_f \leq 10$ ns.

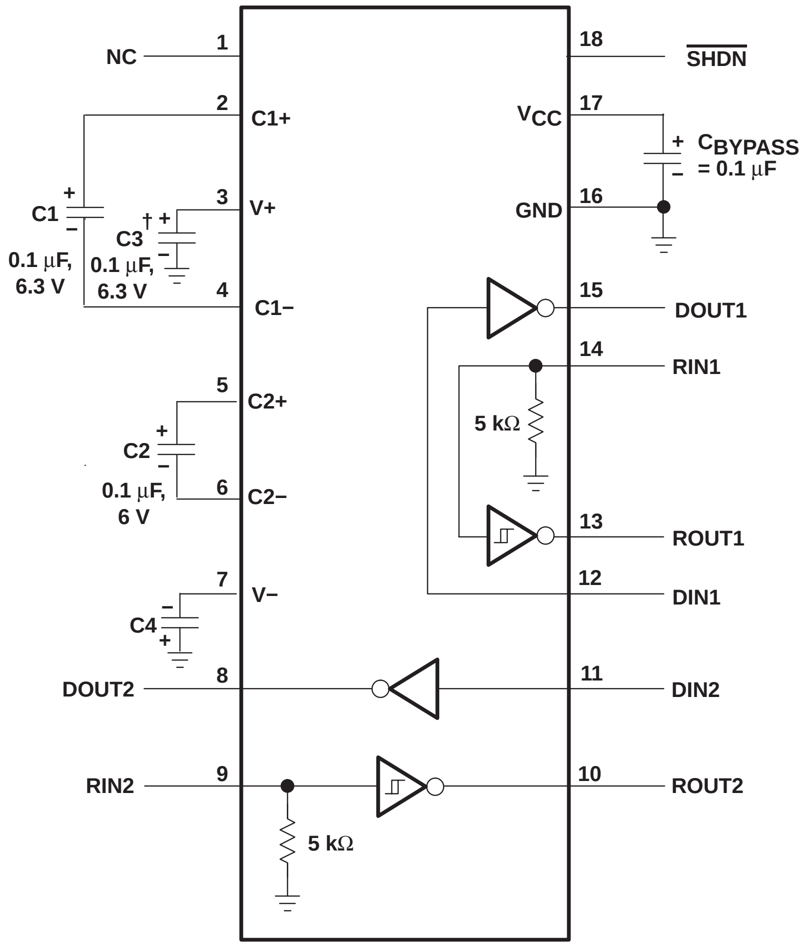
Figure 2. Driver Pulse Skew



NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: Z_O = 50 Ω, 50% duty cycle, $t_r \leq 10$ ns, $t_f \leq 10$ ns.

Figure 3. Receiver Propagation Delay Times

APPLICATION INFORMATION



† C3 can be connected to V_{CC} or GND.

NOTES: A. Resistor values shown are nominal.

B. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown.

Figure 4. Typical Operating Circuit and Capacitor Values

APPLICATION INFORMATION

capacitor selection

The capacitor type used for C1−C4 is not critical for proper operation. The MAX222 requires 0.1-µF capacitors, although capacitors up to 10 µF can be used without harm. Ceramic dielectrics are suggested for the 0.1-µF capacitors. When using the minimum recommended capacitor values, ensure that the capacitance value does not degrade excessively as the operating temperature varies. If in doubt, use capacitors with a larger (e.g., 2×) nominal value. The capacitors' effective series resistance (ESR), which usually rises at low temperatures, influences the amount of ripple on V_+ and V_-.

Use larger capacitors (up to 10 µF) to reduce the output impedance at V_+ and V_-.

Bypass V_{CC} to ground with at least 0.1 µF. In applications sensitive to power-supply noise generated by the charge pumps, decouple V_{CC} to ground with a capacitor the same size as (or larger than) the charge-pump capacitors (C1−C4).

ESD protection

TI MAX222 devices have standard ESD protection structures incorporated on the pins to protect against electrostatic discharges encountered during assembly and handling. In addition, the RS232 bus pins (driver outputs and receiver inputs) of these devices have an extra level of ESD protection. Advanced ESD structures were designed to successfully protect these bus pins against ESD discharge of ±15-kV when powered down.

ESD test conditions

ESD testing stringently is performed by TI, based on various conditions and procedures. Contact TI for a reliability report that documents test setup, methodology, and results.

Human-Body Model

The Human-Body Model (HBM) of ESD testing is shown in Figure 5, while Figure 6 shows the current waveform that is generated during a discharge into a low impedance. The model consists of a 100-pF capacitor, charged to the ESD voltage of concern, and subsequently discharged into the DUT through a 1.5-kΩ resistor.

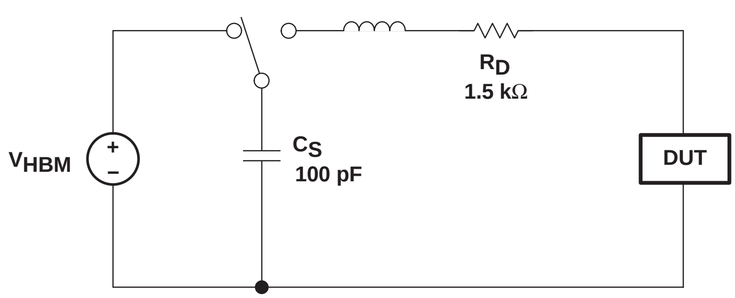


Figure 5. HBM ESD Test Circuit

APPLICATION INFORMATION

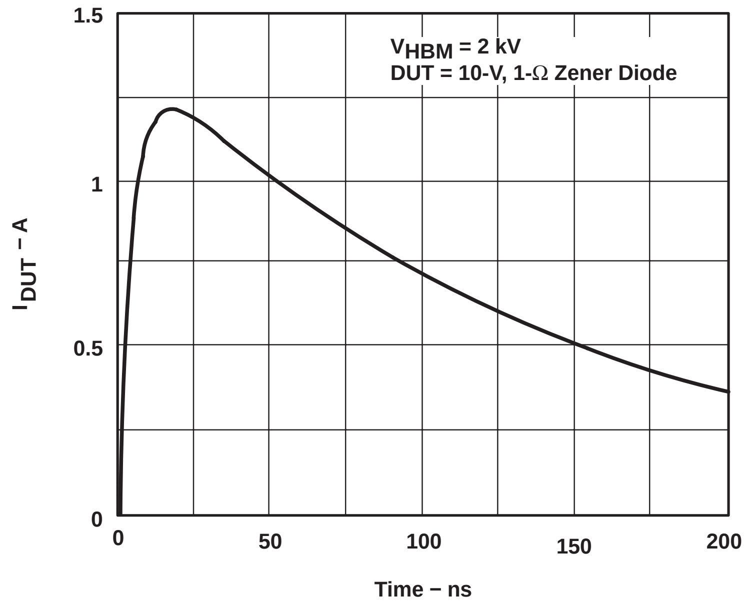


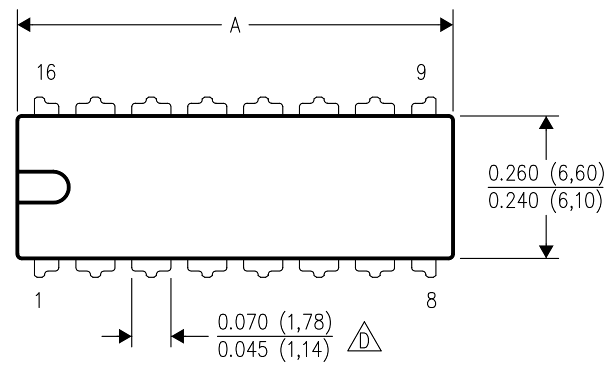
Figure 6. Typical HBM Current Waveform

Machine Model

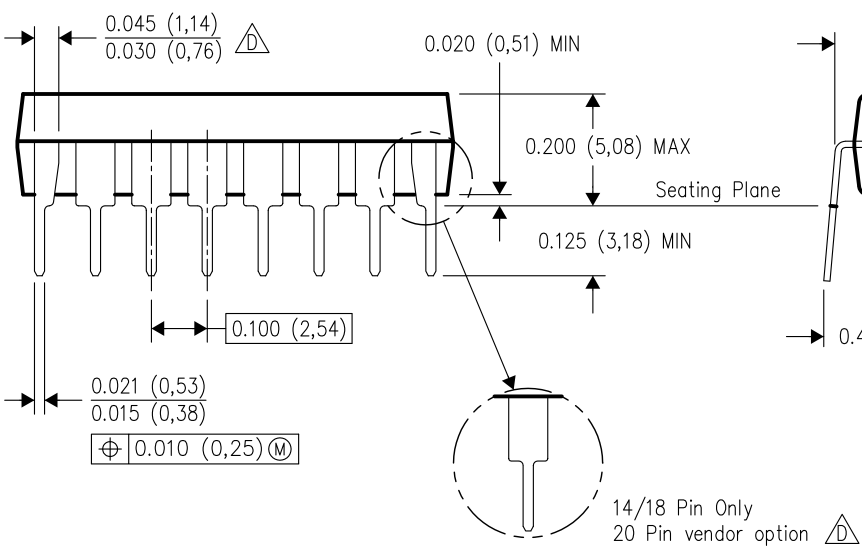
The Machine Model (MM) ESD test applies to all pins using a 200-pF capacitor with no discharge resistance. The purpose of the MM test is to simulate possible ESD conditions that can occur during the handling and assembly processes of manufacturing. In this case, ESD protection is required for all pins, not just RS-232 pins. However, after PC board assembly, the MM test no longer is as pertinent to the RS-232 pins.

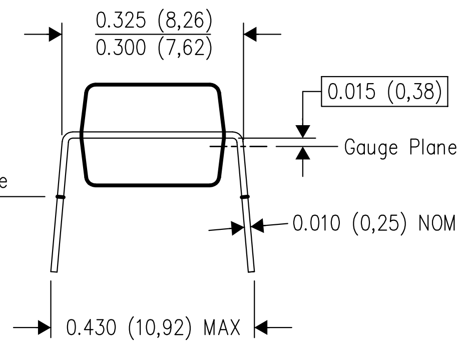
N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



PINS ** / DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD





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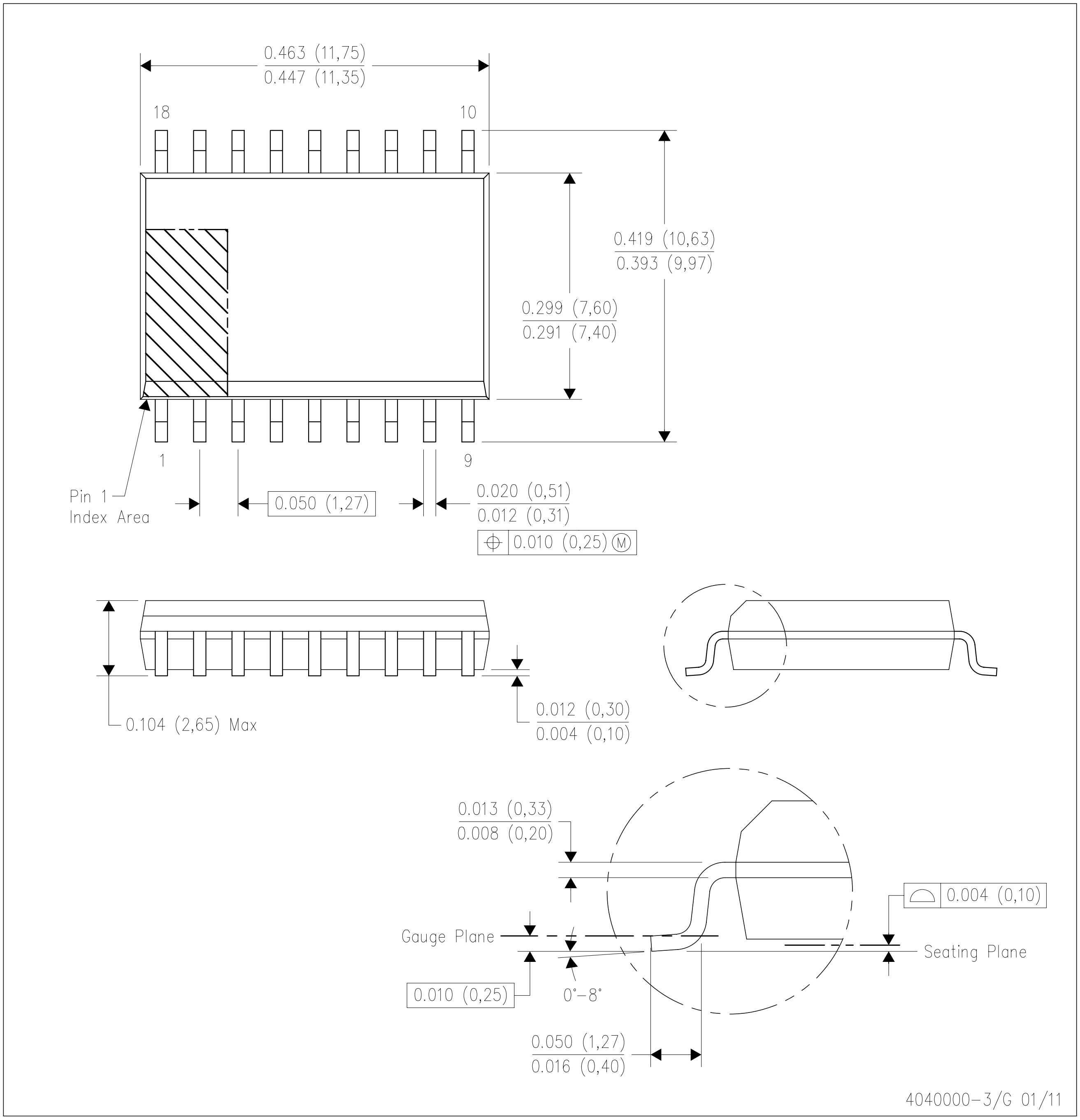
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- (C) Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
- (D) The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW (R-PDSO-G18) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-013 variation AB.