OPA2673 Dual, High Output Current Operational Amplifier With Active Offline Control

1 Features

- Wideband operation: 340 MHz (G = 4 V/V)
- Unity-gain stable: 600 MHz (G = 1 V/V)
- High output current: 700 mA
- Active offline mode for TDMA
- Adjustable power modes:
  - Full-bias mode: 16.5 mA/channel
  - 75% bias mode: 12.5 mA/channel
  - 50% bias mode: 8.5 mA/channel
  - Off-Line mode: 2.4 mA/channel
- Bipolar-supply range: ±3.5 V to ±6.5 V
- Single-supply range: 5.75 V to 13 V
- High slew rate: 3500 V/µs
- Overtemperature protection circuit
- Output current limit (±1 A)

2 Applications

- Power-line modems
- Matched I/Q channel amplifiers
- Broadband video line drivers
- ARB line drivers
- High cap load drivers
- Ultrasonic-Piezo drivers

3 Description

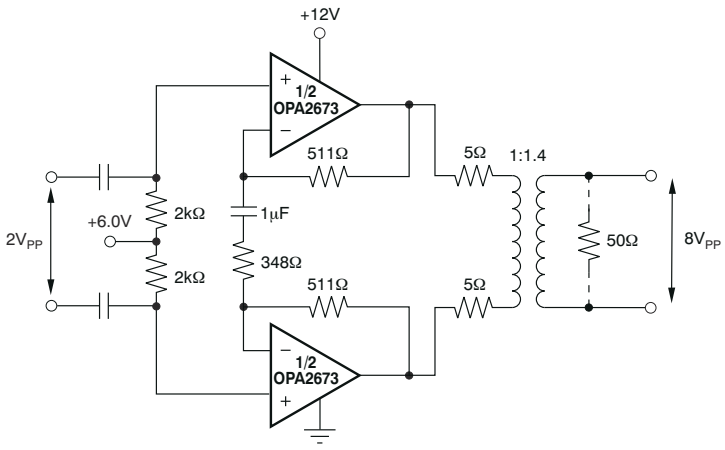
The OPA2673 provides the high output current and low distortion required for power-line modem driver and test and measurement applications. The OPA2673 operates on power-supplies ranging from 5.75 V to 13 V and consumes a low 16.5 mA/channel quiescent current to deliver a very high 700 mA output current. The OPA2673 supports the most demanding power-line modem requirements with an 460 mA specified minimum output current drive (at 25°C).

Power-control features are included to minimize system power consumption. Two logic-control lines allow for four quiescent power settings, full power, 75% bias power, 50% bias power, and offline mode with active offline control, to provide high impedance to large signals present at the output pin. The two channels of the OPA2673 can be used independently as individual op amps, or can be configured as a differential-input to differential-output, high-current line driver.

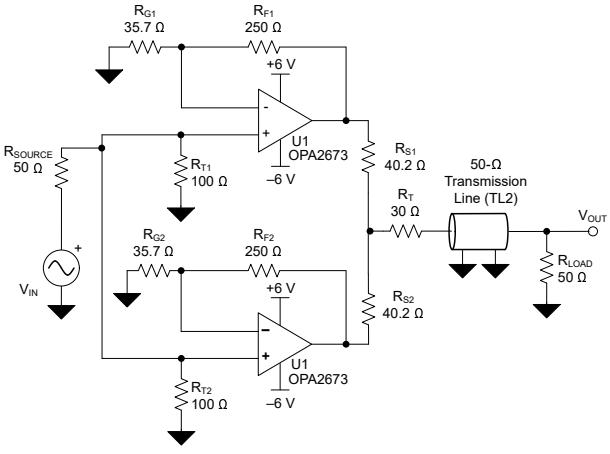
Package Information(1)(2)

PART NUMBER	PACKAGE	PACKAGE SIZE(3)
OPA2673	RGV (VQFN, 16)	4.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) See the *Device Comparison Table*
(3) The package size (length × width) is a nominal value and includes pins, where applicable.



Single-Supply PLC Line Driver



50-Ω Transmission Line Driver

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision G (December 2021) to Revision H (June 2023)	Page
• Changed Figure 7-15, *Open-Loop Transimpedance Gain and Phase* for accuracy	11

Changes from Revision F (April 2010) to Revision G (December 2021)	Page
• Added *Device Information* table, *Pin Functions* table, *ESD Ratings* table, *Recommended Operating Conditions* table, *Thermal Information* table, *Overview* section, *Functional Block Diagram* section, *Feature Description* section, *Device Functional Modes* section, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Changed the title of the *Related Products* section to *Device Family Comparison Table*	4
• Deleted *Package/Ordering Information* table	4
• Changed the title of the *Pin Configuration* section to *Pin Configuration and Functions*	5
• Changed QFN to VQFN throughout the document	5
• Changed all input pin current limit from ±30 mA to ±10 mA	6
• Added new thermal metric table	7
• Changed SSBW across temperaure at G = 4 V/V from 260 MHz to 300 MHz	7
• Changed SSBW across temperaure at G = 8 V/V from 260 MHz to 300 MHz	7
• Added new specifications for LSBW at gain of 9 V/V and 8 V/V	7
• Changed LSBW at G = 4 V/V from 300 MHz to 144 MHz	7
• Changed Slew Rate specification from 3000 V/µs to 3500 V/µs	7
• Changed HD2 from -68 dBc to -70 dBc	7
• Changed HD3 from -72 dBc to -73 dBc	7
• Changed noninverting input current noise from 5.2 pA/√Hz to 3 pA/√Hz	7
• Changed inverting input current noise from 35 pA/√Hz to 25 pA/√Hz	7
• Changed crosstalk from -92 dBc to -85 dBc	7
• Changed typical noninverting input resistance from 1.5 MΩ to 3 MΩ	7
• Changed minimum inverting input resistance from 16Ω to 10Ω	7

- Changed typical short circuit current limit from ±800 mA to ±1000 mA....7
- Changed typical closed-loop output impedance from 10 mΩ to 0.4 mΩ....7
- Changed maximum quiescent current at full bias from 38 mA to 42 mA....7
- Changed maximum quiescent current across temperature at full bias from 42 mA to 46 mA....7
- Added +PSRR specification....7
- Added AC performance data at 75% Bias....9
- Changed HD3 spec at 75% bias from -66 dBc to -72 dBc....9
- Changed maximum quiescent current at 75% bias from 29 mA to 31 mA....9
- Added AC performance data at 50% Bias....10
- Changed HD3 spec at 50% bias from -60 dBc to -70 dBc....10
- Quiescent current at 75% and 50% bias condition at room temperature and across temperature increased by 2mA....10
- Changed maximum quiescent current at full bias from 19 mA to 21 mA....10

Changes from Revision E (April 2010) to Revision F (May 2010) **Page**

- Added *minimum operating voltage* (single supply) parameter....6

Changes from Revision D (January 2010) to Revision E (April 2010) **Page**

- Revised *Absolute Maximum Ratings* table; deleted lead temperature specification, changed storage temperature range from -40°C to -65°C....6

5 Device Family Comparison Table

SINGLES	DUALS	TRIPLES	NOTES
OPA691	OPA2691	OPA3691	Single +12 V capable
—	THS6042	—	±15 V capable
—	OPA2677	—	Single +12 V capable
—	OPA2675	—	Single +12 V capable, output current limit

6 Pin Configuration and Functions

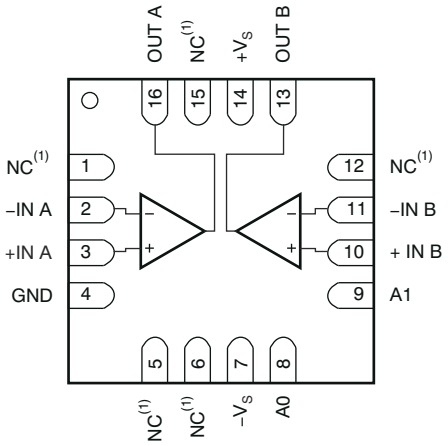


Figure 6-1. RGV Package, 16-Pin VQFN (Top View)

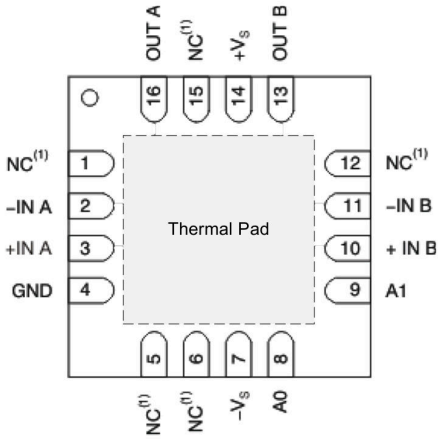


Figure 6-2. RGV Package, 16-Pin VQFN (Bottom View)

Table 6-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
A0	8	Input	Bias mode control
A1	9	Input	Bias mode control
GND	4	Power	Ground
–IN A	2	Input	Amplifier A inverting input
+IN A	3	Input	Amplifier A noninverting input
–IN B	11	Input	Amplifier B inverting input
+IN B	10	Input	Amplifier B noninverting input
NC	1, 5, 6, 12, 15	—	Do not connect. There is no internal connection. Typically GND is the recommended connection to a heat-spreading plane.
OUT A	16	Output	Amplifier A output
OUT B	13	Output	Amplifier B output
$-V_S$	7	Power	Negative power-supply connection
$+V_S$	14	Power	Positive power-supply connection
Thermal Pad		—	Electrically connected to die substrate and V_{S-}. Connect to V_{S-} on the PCB for best performance.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	Supply voltage, $V_S = (V_{S+}) – (V_{S–})$(2)		13	V
	Bias control pin voltage, referenced to GND	0	$V_{S–}$ + 5	
	All pins except V_{S+}, $V_{S–}$ and bias control pins	$V_{S–}$	V_{S+}	
	GND pin	$V_{S–}$	V_{S+}	
	Output pin: Offline mode		±4.5	
	Inverting input pin: Offline mode		±1.1	
	Differential input voltage (each amplifier)		±2	
Current	All input pins, current limit		±10	mA
	Continuous power dissipation	See Thermal Information		
Temperature	Continuous operating junction temperature(3)		139	°C
	Maximum junction, T_J (under any condition)(5)		150	
	Storage, T_{stg}	–65	150	

(1) Operation outside the *Absolute Maximum Rating* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Condition*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Refer to Breakdown Test.
(3) The absolute maximum junction temperature for continuous operation is limited by the package constraints. Operation above this temperature can result in reduced reliability and/or lifetime of the device. The device has thermal protection that shuts down the device at approximately 180°C junction temperature and recovery at approximately 160°C.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_S	Supply voltage, dual supply	±3.5		±6.5	V
V_S	Supply voltage, single supply	5.75		13	
GND	GND pin voltage	$V_{S–}$		V_{S+} – 2.5	
T_A	Ambient operating air temperature	–40	25	85	°C
	Thermal shutdown(1)		180		

(1) The OPA2673 has thermal protection that shuts down the device at approximately 180°C junction temperature and with recovery at approximately 160°C.

7.4 Thermal Information

THERMAL METRIC[1]		OPA2673A RGV (VQFN) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	43	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	43	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	18	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.1	°C/W
Y_{JB}	Junction-to-board characterization parameter	18	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.5	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics: Full Bias and Offline Mode V_S = ±6 V

At T_A = +25°C, A0 = A1 = 0 (full power), G = + 4V/V, R_F = 402 Ω, and R_L = 100 Ω, C_L = 1 pF, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AC PERFORMANCE[1]						
SSBW	Small-signal bandwidth	G = 1 V/V, R_F = 511 Ω, V_O = 0.5 V_{PP}		600		MHz
		G = 2 V/V, R_F = 475 Ω, V_O = 0.5 V_{PP}		450		
		G = 4 V/V, R_F = 402 Ω, V_O = 0.5 V_{PP}	270	340		
		G = 4 V/V, T_A = –40°C to 85°C		300		
		G = 8 V/V, R_F = 250 Ω, V_O = 0.5 V_{PP}	270	340		
		G = 8 V/V, T_A = –40°C to 85°C		300		
	Peaking at G = 1V/V	G = 1V/V, R_F = 511 Ω		1.5		dB
	Peaking at G = 4V/V	G = 4V/V, R_F = 402 Ω		0.1		dB
LSBW	Large-signal bandwidth	G = 9 V/V, R_F = 250 Ω, V_O = 9 V_{PP}		230		MHz
	Large-signal bandwidth	G = 8 V/V, R_F = 250 Ω, V_O = 5 V_{PP}		330		
	Large-signal bandwidth	G = 4 V/V, V_O = 5 V_{PP}		144		
	±0.1-dB bandwidth flatness			70		
SR	Slew rate (20% to 80%)	V_O = 5-V step		3500		V/µs
		T_A = –40°C to 85°C	2300			
	Rise and fall time (10% to 90%)	V_O = 2-V Step		1.2		ns
HD	2nd-order harmonic distortion	V_O = 2 V_{PP}, 20 MHz, R_L = 50 Ω		–70		dBc
	3rd-order harmonic distortion			–73		
HD	2nd-order harmonic distortion	V_O = 2 V_{PP}, 20 MHz, R_L = 50 Ω, T_A = –40°C to 85°C	–63			
	3rd-order harmonic distortion		–61			
e_n	Input voltage noise	f ≥ 1 MHz, input-referred		2.4	2.62	nV/√Hz
i_{n+}	Noninverting input current noise			3	4.6	pA/√Hz
i_{n-}	Inverting input current noise			25	30	
e_n	Input voltage noise	f ≥ 1 MHz, input-referred, T_A = –40°C to 85°C			4.2	nV/√Hz
i_{n+}	Noninverting input current noise				8.3	pA/√Hz
i_{n-}	Inverting input current noise				35	
	Channel-to-channel crosstalk	f ≥ 1 MHz, input-referred		–85		dBc

7.5 Electrical Characteristics: Full Bias and Offline Mode V_S = ±6 V (continued)

At T_A = +25°C, A0 = A1 = 0 (full power), G = + 4V/V, R_F = 402 Ω, and R_L = 100 Ω, C_L = 1 pF, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC PERFORMANCE						
Z_{OL}	Open-loop transimpedance gain		60	90		kΩ
		T_A= –40°C to 85°C	55			
	Input offset voltage (each amplifier)			±2	±7	mV
		T_A = –40°C to 85°C			±9	
	Input offset voltage mismatching	Amplifier A to B		±0.5	±2.2	
		T_A = –40°C to 85°C			±2.5	
	Input offset voltage drift	T_A = –40°C to 85°C			±30	µV/°C
	Noninverting input bias current			±5	±25	µA
		T_A = –40°C to 85°C			±28	
	Inverting input bias current			±6	±48	
		T_A = –40°C to 85°C			±55	
	Noninverting input bias current matching			±0.5	±5	µA
		T_A = –40°C to 85°C			±7	
	Inverting input bias current matching			±6	±25	
		T_A = –40°C to 85°C			±30	
	Noninverting input bias current drift	T_A = –40°C to 85°C			±47	nA/°C
	Inverting input bias current drift				±110	
INPUT CHARACTERISTICS						
CMIR	Common-mode input range		±3.5	±3.6		V
		T_A= –40°C to 85°C	±3.2			
CMRR	Common-mode rejection ratio		50	56		dB
		T_A = –40°C to 85°C	47			
	Noninverting input resistance			3 || 1.5		MΩ || pF
	Inverting input resistance		10	24	40	Ω
	Shutdown Isolation,Offline Mode	Input to Output Isolation at 1 MHz		85		dB
OUTPUT CHARACTERISTICS						
V_O	Output voltage swing(2)	No Load	±4.8	±4.9		V
		No Load, T_A = –40°C to 85°C	±4.7			
V_O	Output voltage swing(2)	R_L = 100 Ω	±4.75	±4.9		V
		R_L = 100 Ω, T_A = –40°C to 85°C	±4.65			
		R_L = 25 Ω	±4.5	±4.7		
		R_L = 25 Ω, T_A = –40°C to 85°C	±4.4			
I_O	Output current (sourcing and sinking) (2)	R_L = 4 Ω	±460	±700		mA
		R_L = 4 Ω, T_A = –40°C to 85°C	±425			
	Short-circuit output current	Sourcing and Sinking		±1000		mA
Z_{OUT}	Closed-Loop output impedance	f = 100 kHz		0.4		mΩ
Z_O	Open-Loop Output impedance	f = 100 kHz, Offline Mode		25 || 4.5		kΩ || pF

7.5 Electrical Characteristics: Full Bias and Offline Mode V_S = ±6 V (continued)

At T_A = +25°C, A0 = A1 = 0 (full power), G = + 4V/V, R_F = 402 Ω, and R_L = 100 Ω, C_L = 1 pF, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
I_Q	Quiescent current, Total both channels	Full bias (A0 = 0, A1 = 0)		33	42	mA
		Full bias, T_A = –40°C to 85°C			46	
		Offline Mode (A0 = 1, A1 = 1)		5.5	7.2	
		Offline Mode, T_A = –40°C to 85°C			9	
+PSRR	Positive power-supply rejection ratio	T_A = –40°C to 85°C	57	60		dB
–PSRR	Negative power-supply rejection ratio		47	55		
BIAS CONTROL						
	Bias control pin logic threshold	Logic 1, with respect to GND	2			V
		Logic 0, with respect to GND			0.8	
	Bias control pin current	A0, A1 = 0.5 V(3) , T_A = –40°C to 85°C			30	µA
		A0, A1 = 3.3 V, T_A = –40°C to 85°C			150	

(1) Min/Max limits for AC performance set by design
(2) See Output Headroom vs Output Current for output voltage vs output current characteristics.
(3) Current flows into the pins.

7.6 Electrical Characteristics: 75% Bias Mode V_S = ±6 V

At T_A = +25°C, A0 = 1, A1 = 0 (75% Bias), G = + 4V/V, R_F = 402 Ω, and R_L = 100 Ω, C_L = 1 pF, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AC PERFORMANCE						
SSBW	Small-signal bandwidth	G = 4 V/V, R_F = 402 Ω, V_O = 0.5 V_{PP}		310		MHz
LSBW	Large-signal bandwidth	V_O = 4 V_{PP}		160		
SR	Slew rate (20% to 80%)	V_O = 5-V step		3000		V/µs
HD2	2nd-order harmonic distortion	V_O = 2 V_{PP}, 20 MHz ,R_L = 50 Ω		-69		dBc
HD3	3rd-order harmonic distortion			-72		
e_n	input voltage noise	f ≥ 1 MHz, input-referred		2.6		nV/√Hz
	Input offset voltage (each amplifier)			±2	±7	mV
		T_A = –40°C to 85°C			±9	
I_O	Output current (sourcing and sinking)	R_L = 4 Ω	±350	±500		mA
		R_L = 4 Ω, T_A = –40°C to 85°C	±300			
	Short-circuit output current	Sourcing and Sinking		±1000		
POWER SUPPLY						
I_Q	Quiescent current, Total both channels			25	31	mA
		T_A = –40°C to 85°C			34	

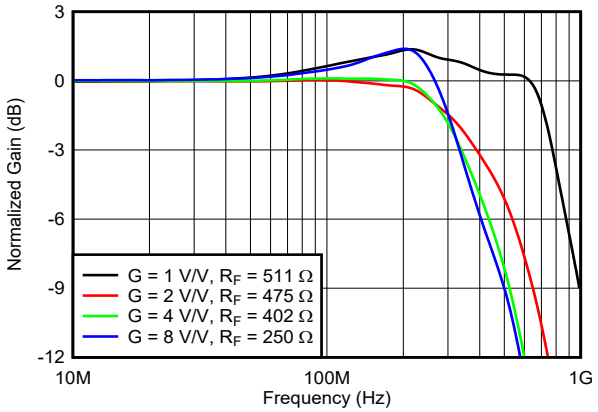
7.7 Electrical Characteristics: 50% Bias Mode V_S = ±6 V

At T_A = +25°C, A0 = 0 , A1 = 1 (50% Bias), G = + 4V/V, R_F = 402 Ω, and R_L = 100 Ω, C_L = 1 pF, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AC PERFORMANCE						
SSBW	Small-signal bandwidth	G = 4 V/V, R_F = 402 Ω, V_O = 0.5 V_{PP}		260		MHz
LSBW	Large-signal bandwidth	V_O = 4 V_{PP}		140		
SR	Slew rate (20% to 80%)	V_O = 5-V step		2700		V/µs
HD2	2nd-order harmonic distortion	V_O = 2 V_{PP}, 20 MHz, R_L = 50 Ω		-66		dBc
HD3	3rd-order harmonic distortion			-70		
e_n	input voltage noise	f ≥ 1 MHz, input-referred		3.2		nV/√Hz
	Input offset voltage (each amplifier)			±2	±7	mV
		T_A = –40°C to 85°C			±9	
I_O	Output current (sourcing and sinking)	R_L = 4 Ω	±120	±180		mA
		R_L = 4 Ω, T_A = –40°C to 85°C	±110			
	Short-circuit output current	Sourcing and Sinking		±1000		
POWER SUPPLY						
I_Q	Quiescent current, Total both channels			17	21	mA
		T_A = –40°C to 85°C			23	

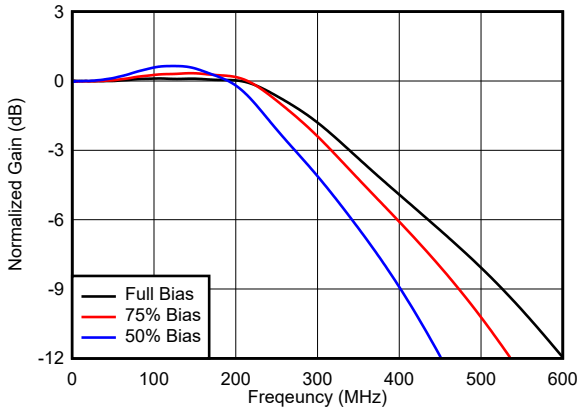
7.8 Typical Characteristics: V_S = ±6 V, Full Bias

At T_A = +25°C, G = +4 V/V, R_F = 402 Ω, and R_L = 100 Ω, unless otherwise specified.



V_O = 500 mV_{PP}

Figure 7-1. Small-Signal Frequency Response



V_O = 500 mV_{PP}

Figure 7-2. Small-Signal Frequency Response Over Power Settings

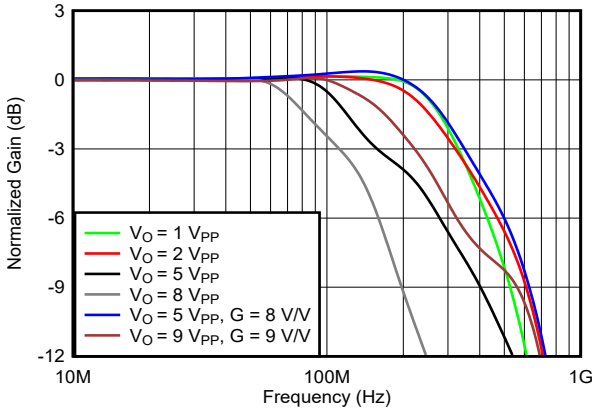
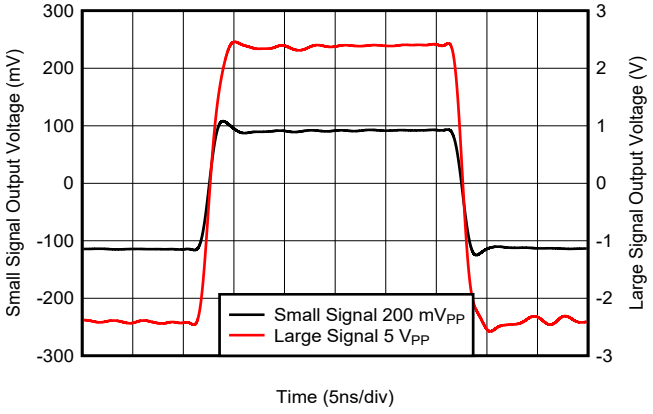
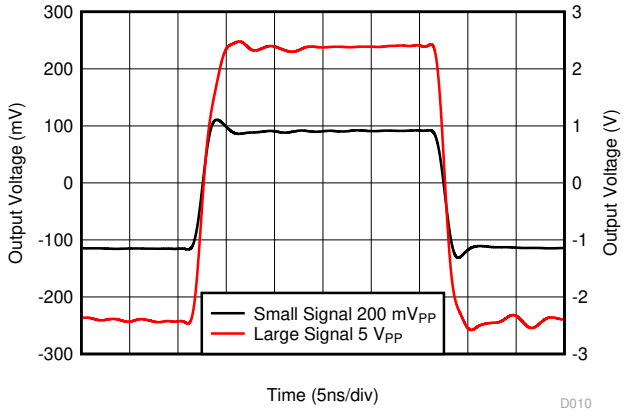


Figure 7-3. Large-Signal Frequency Response



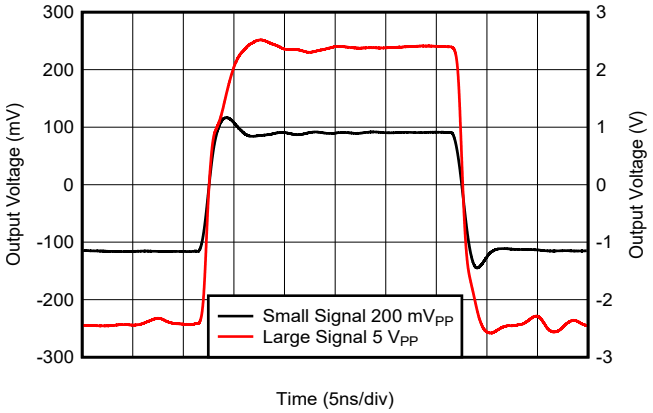
Full Bias Mode

Figure 7-4. Small-Signal and Large-Signal Pulse Responses



75% Bias Mode

Figure 7-5. Small-Signal and Large-Signal Pulse Responses



50% Bias Mode

Figure 7-6. Small-Signal and Large-Signal Pulse Responses

7.8 Typical Characteristics: V_S = ±6 V, Full Bias (continued)

At T_A = +25°C, G = +4 V/V, R_F = 402 Ω, and R_L = 100 Ω, unless otherwise specified.

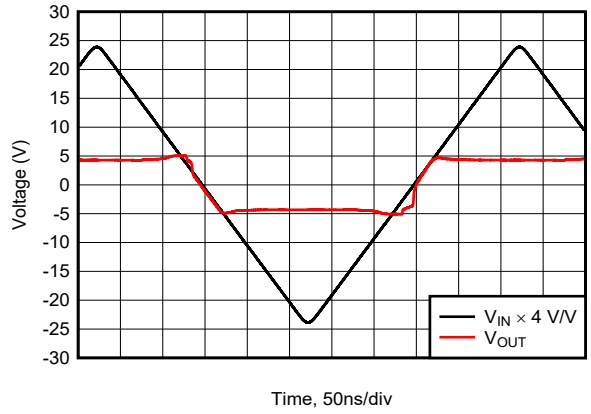


Figure 7-7. Overdrive Recovery

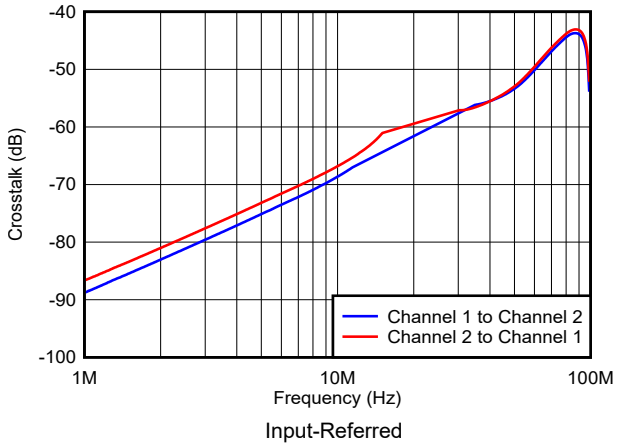


Figure 7-8. Channel-to-Channel Crosstalk

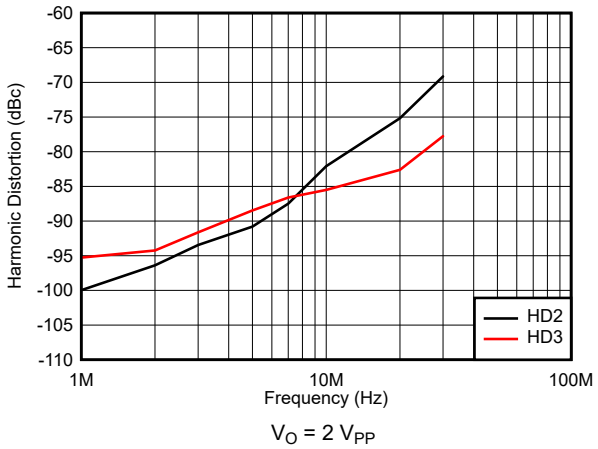


Figure 7-9. Harmonic Distortion vs Frequency

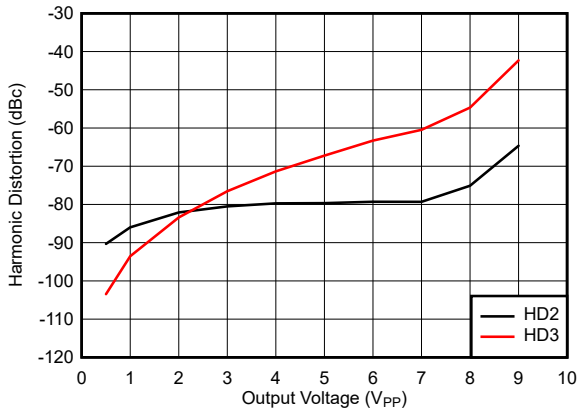


Figure 7-10. Harmonic Distortion vs Output Voltage

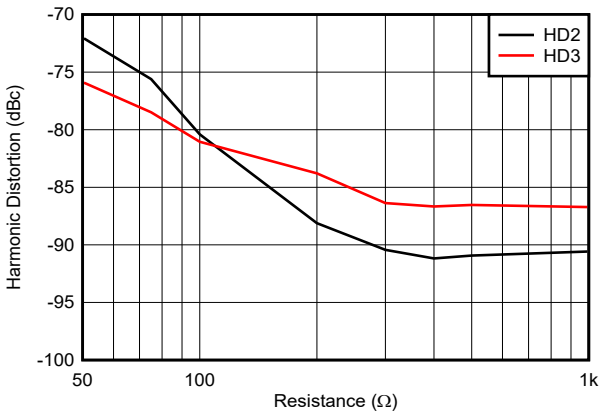


Figure 7-11. Harmonic Distortion vs Load Resistance

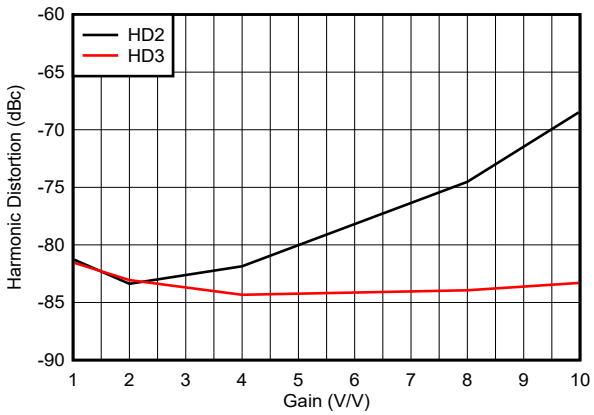


Figure 7-12. Harmonic Distortion vs Noninverting Gain

7.8 Typical Characteristics: V_S = ±6 V, Full Bias (continued)

At T_A = +25°C, G = +4 V/V, R_F = 402 Ω, and R_L = 100 Ω, unless otherwise specified.

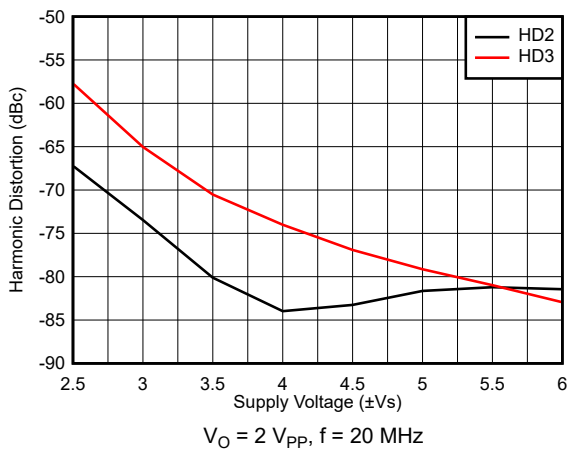


Figure 7-13. Harmonic Distortion vs Supply Voltage

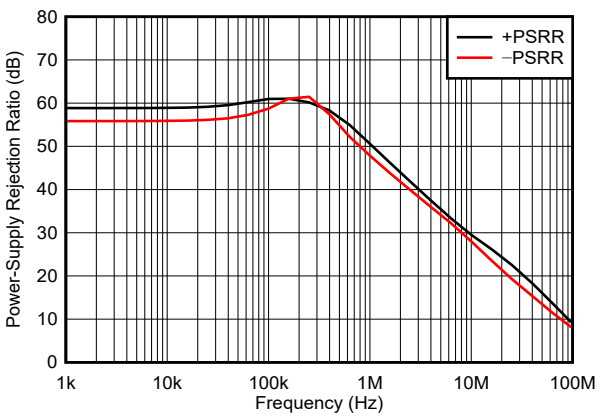


Figure 7-14. CMRR and PSRR vs Frequency

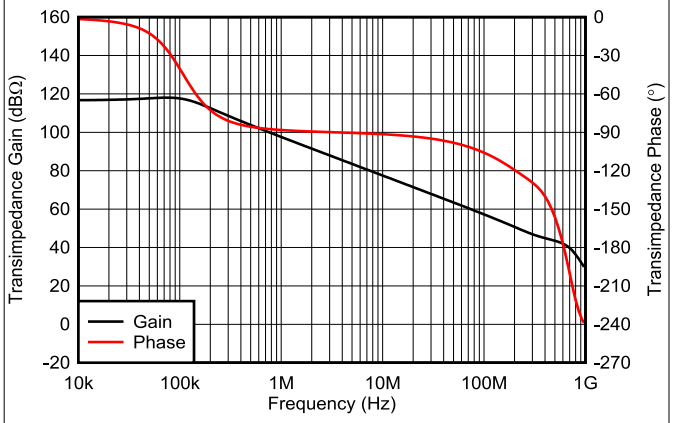


Figure 7-15. Open-Loop Transimpedance Gain and Phase

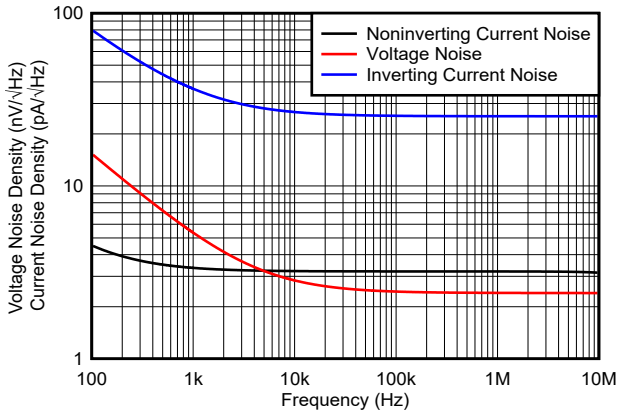


Figure 7-16. Input Voltage and Current Noise Density

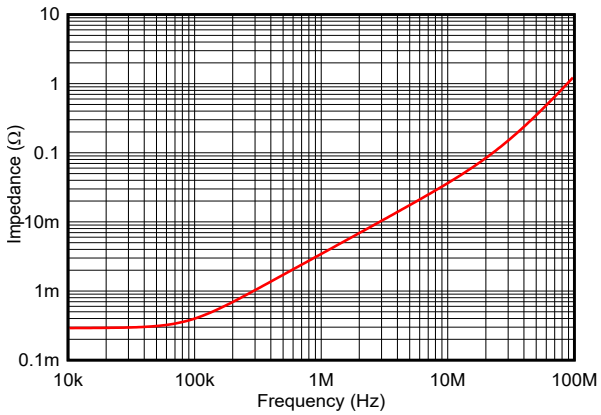


Figure 7-17. Closed-Loop Output Impedance vs Frequency

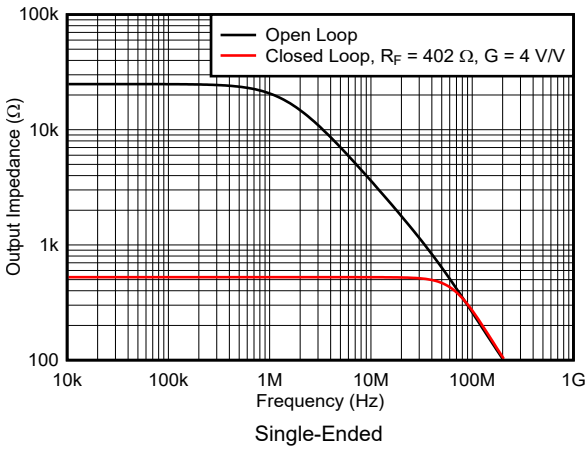


Figure 7-18. Active Off-Line Impedance vs Frequency

7.8 Typical Characteristics: V_S = ±6 V, Full Bias (continued)

At T_A = +25°C, G = +4 V/V, R_F = 402 Ω, and R_L = 100 Ω, unless otherwise specified.

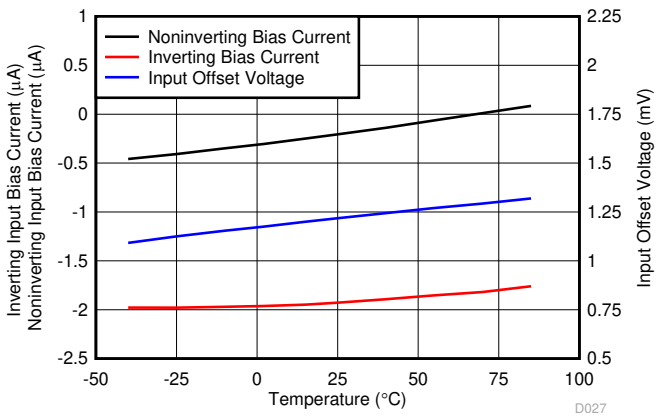


Figure 7-19. Typical DC Drift Over Temperature

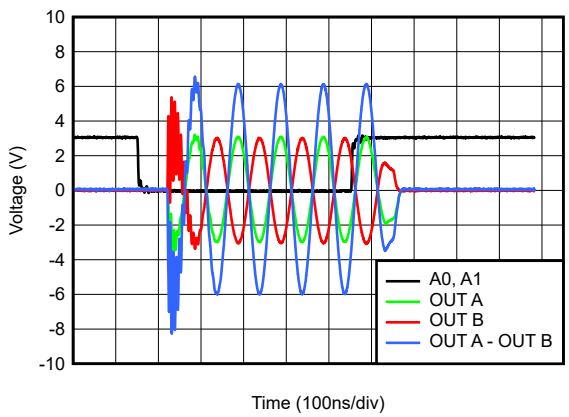


Figure 7-20. Full Bias Mode to Offline Mode Transition Time

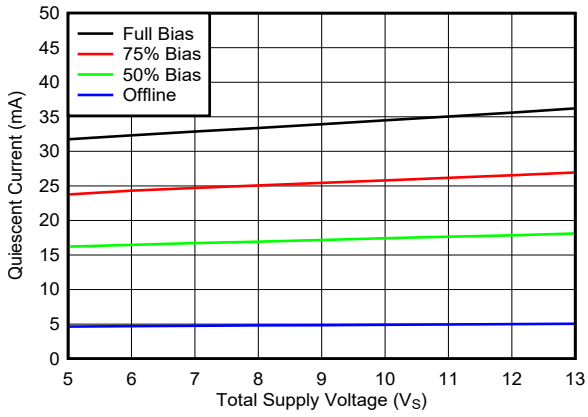


Figure 7-21. Supply Current vs Supply Voltage

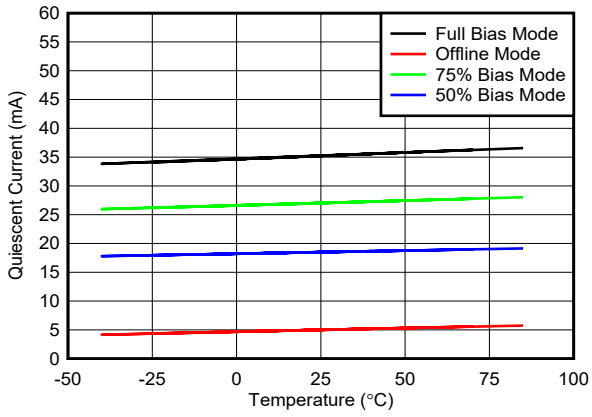
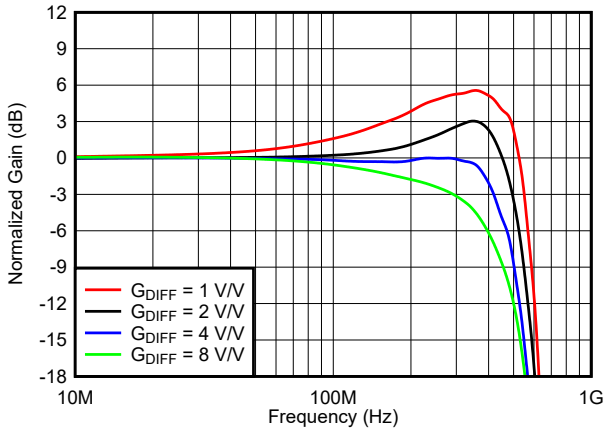


Figure 7-22. Supply Current vs Temperature

7.9 Typical Characteristics: V_S = ±6 V Differential, Full Bias

At T_A = +25°C, R_F = 511 Ω, R_L = 100 Ω Differential, G_{DIFF} = +4 V/V, and G_{CM} = +1 V/V, unless otherwise specified.



V_O = 500 mV_{PP}

Figure 7-23. Small-Signal Frequency Response

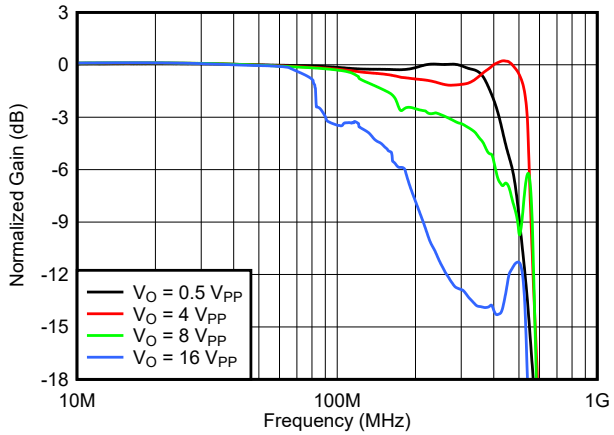


Figure 7-24. Large-Signal Frequency Response

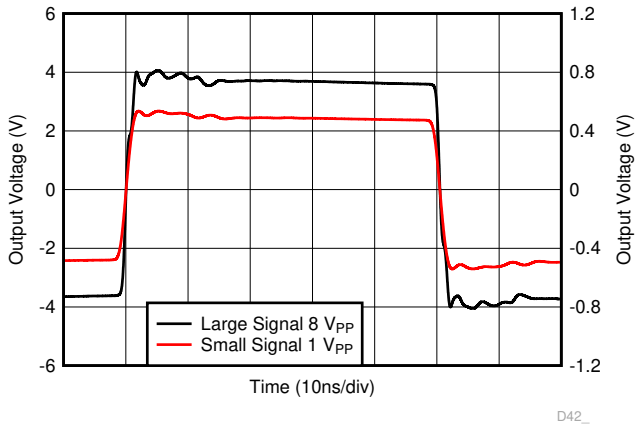
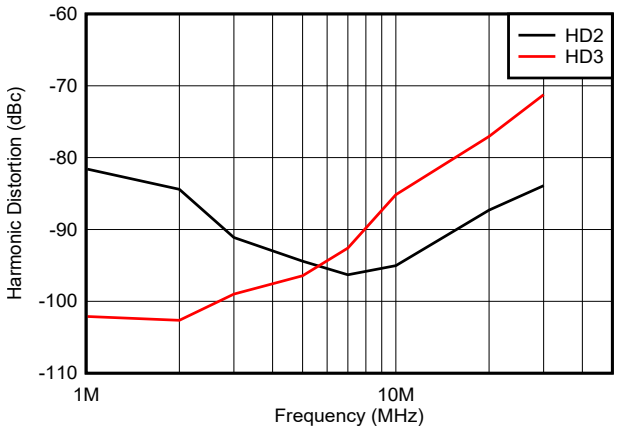
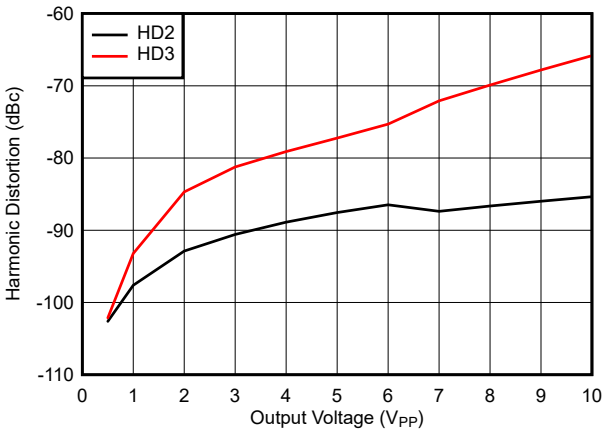


Figure 7-25. Small-Signal and Large-Signal Pulse Responses



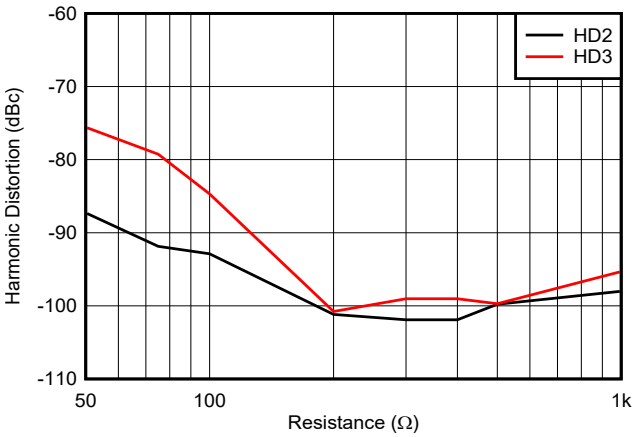
V_O = 2 V_{PP}

Figure 7-26. Harmonic Distortion vs Frequency



f = 20 MHz

Figure 7-27. Harmonic Distortion vs Output Voltage

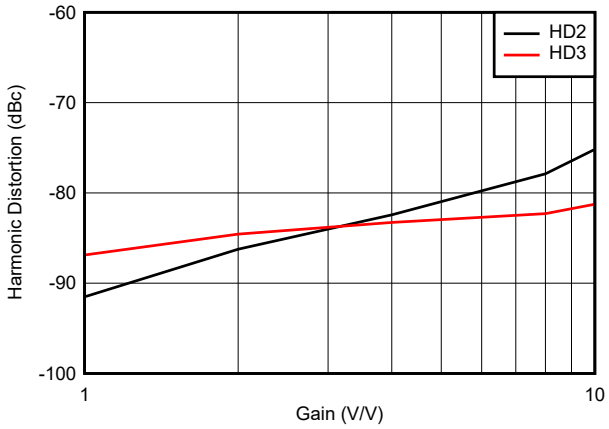


V_O = 2 V_{PP}, f = 20 MHz

Figure 7-28. Harmonic Distortion vs Load Resistance

7.9 Typical Characteristics: V_S = ±6 V Differential, Full Bias (continued)

At T_A = +25°C, R_F = 511 Ω, R_L = 100 Ω Differential, G_{DIFF} = +4 V/V, and G_{CM} = +1 V/V, unless otherwise specified.

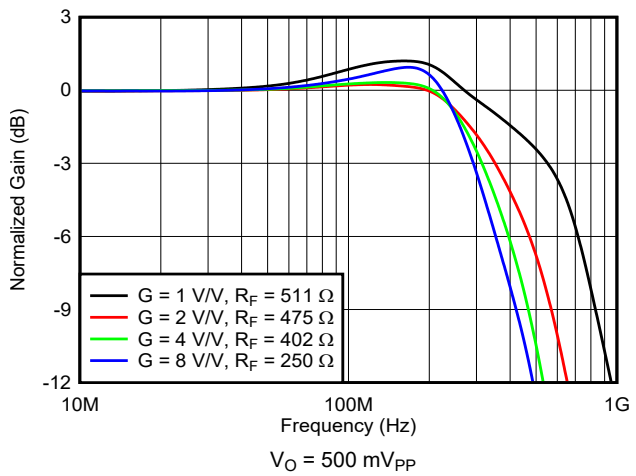


V_O = 2 V_{PP}, f = 20 MHz

Figure 7-29. Harmonic Distortion vs Noninverting Gain

7.10 Typical Characteristics: V_S = ±6 V, 75% Bias

At T_A = +25°C, G = +4 V/V, R_F = 402 Ω, and R_L = 100 Ω, unless otherwise specified.



V_O = 500 mV_{PP}

Figure 7-30. Small-Signal Frequency Response

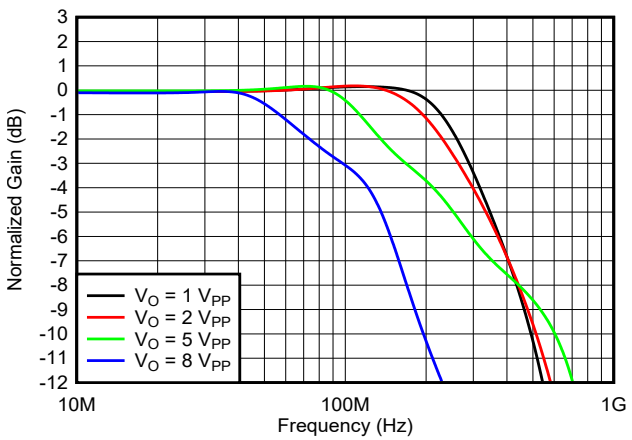
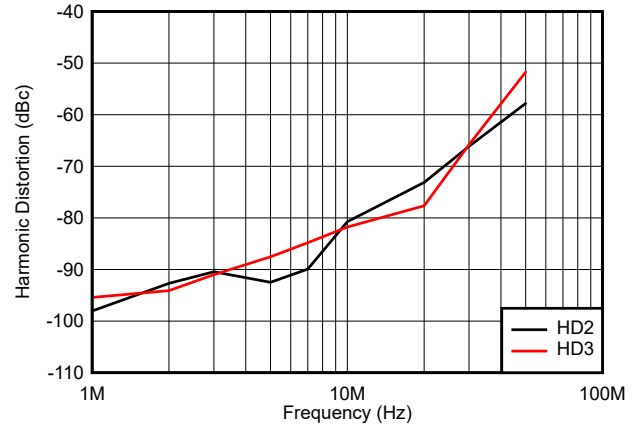
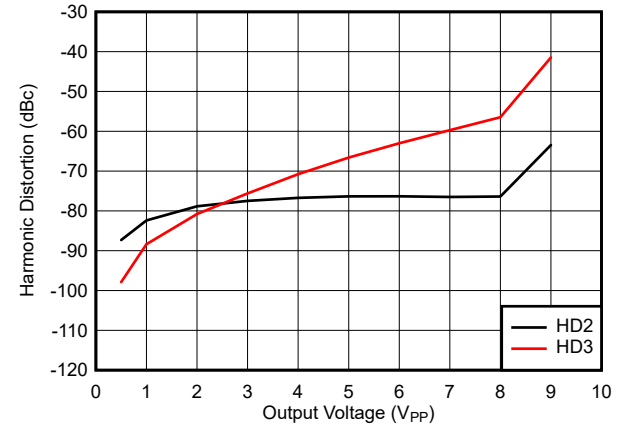


Figure 7-31. Large-Signal Frequency Response



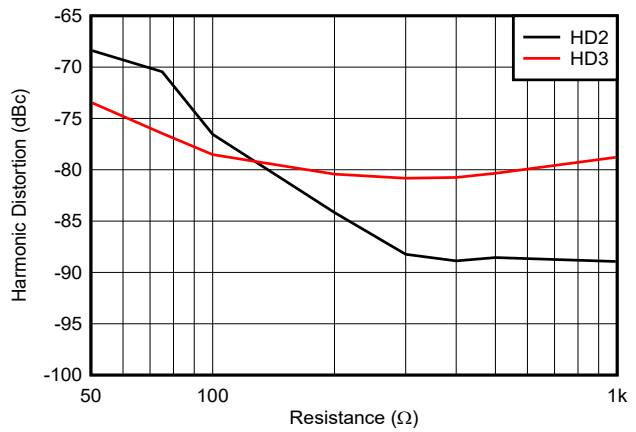
V_O = 2 V_{PP}

Figure 7-32. Harmonic Distortion vs Frequency



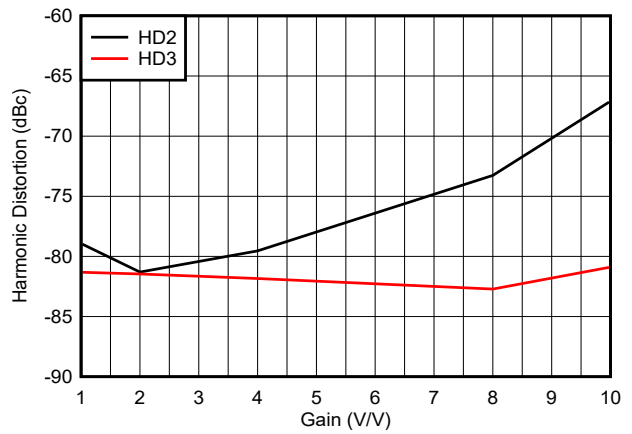
f = 20 MHz

Figure 7-33. Harmonic Distortion vs Output Voltage



V_O = 2 V_{PP}, f = 20 MHz

Figure 7-34. Harmonic Distortion vs Load Resistance



V_O = 2 V_{PP}, f = 20 MHz

Figure 7-35. Harmonic Distortion vs Noninverting Gain

7.11 Typical Characteristics: V_S = ±6 V, 50% Bias

At T_A = +25°C, G = +4 V/V, R_F = 402 Ω, and R_L = 100 Ω, unless otherwise specified.

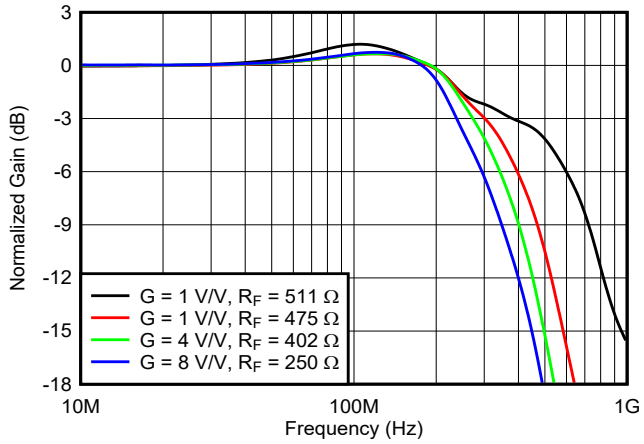


Figure 7-36. Small-Signal Frequency Response

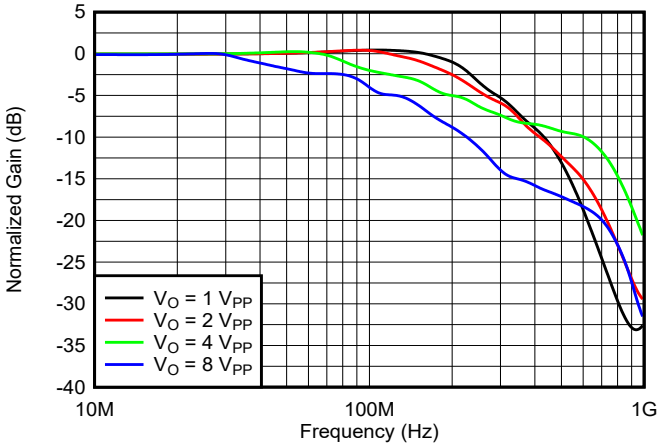
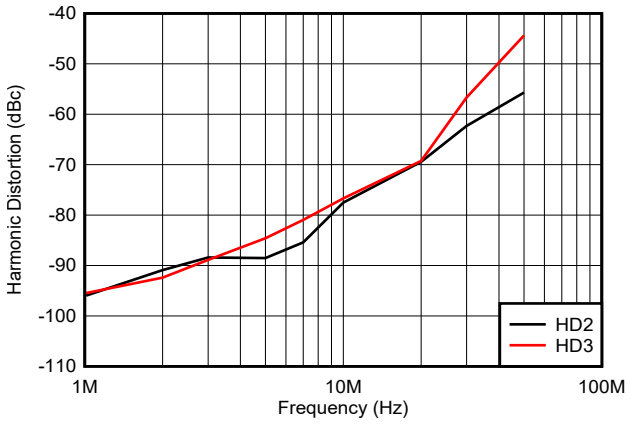
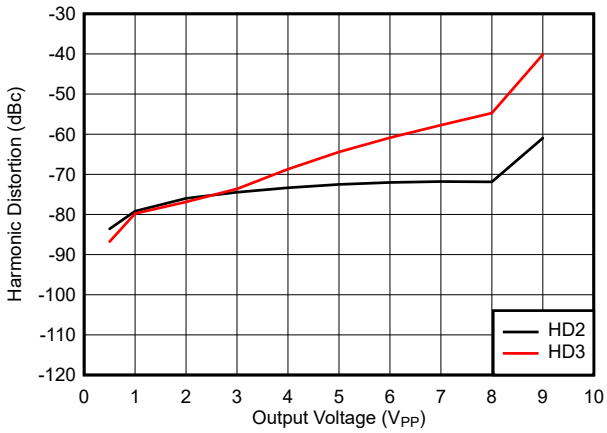


Figure 7-37. Large-Signal Frequency Response



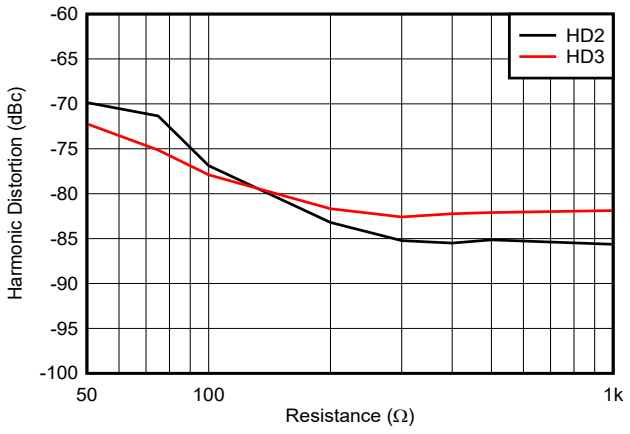
V_O = 2 V_{PP}

Figure 7-38. Harmonic Distortion vs Frequency



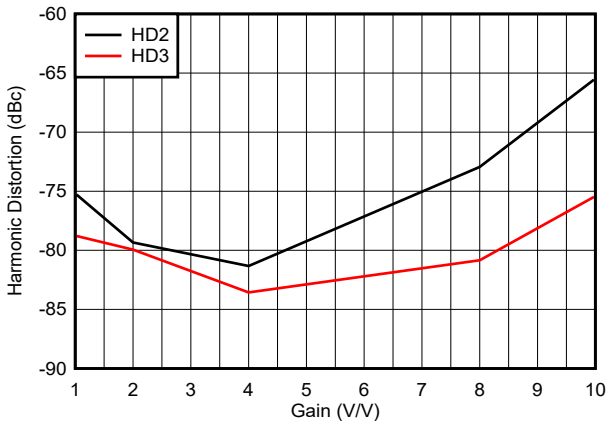
f = 20 MHz

Figure 7-39. Harmonic Distortion vs Output Voltage



V_O = 2 V_{PP}, f = 20 MHz

Figure 7-40. Harmonic Distortion vs Load Resistance



V_O = 2 V_{PP}, f = 20 MHz

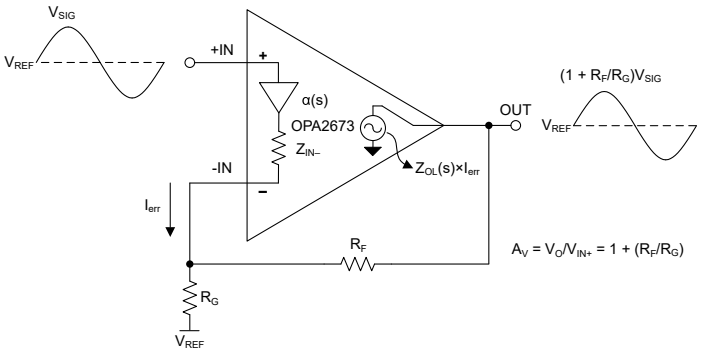
Figure 7-41. Harmonic Distortion vs Noninverting Gain

8 Detailed Description

8.1 Overview

The OPA2673 is a high-speed, high-current output, current-feedback amplifier (CFA) designed to operate over the wide supply range of ±3.5 V to ±6.5 V for applications requiring large-drive currents along with wide bandwidth. The OPA2673 features an offline mode that enables the amplifier to operate in a high-output-impedance condition, with no loading to the network when connected in a bus topology. Figure 3-1 shows how the two channels of the OPA2673 can be used as two independent amplifiers or can be connected in a differential-input to differential-output configuration.

8.2 Functional Block Diagram



8.3 Feature Description

The OPA2673 gives exceptional ac performance with a highly linear, high-power output stage. Requiring 16-mA/ch quiescent current, the OPA2673 swings to within 1.1 V of either supply rail and delivers in excess of 460 mA at room temperature. This low-output headroom requirement, along with supply voltage independent biasing, gives remarkable dual (±6 V) supply operation. The OPA2673 delivers greater than 450 MHz of bandwidth driving a 2-V_{PP} output into 100 Ω on a single 12-V supply.

The primary advantage of a current-feedback op amp over a voltage-feedback op amp is that ac performance (bandwidth and distortion) is relatively independent of signal gain. Figure 8-1 shows the dc-coupled, gain of +4 V/V, dual power-supply circuit configuration used as the test circuit for the ±6-V *Electrical Characteristics* and *Typical Characteristics*. Voltage swings reported in the *Electrical Characteristics* are taken directly at the input and output pins. For measuring the ac performance, the output of the OPA2673 is terminated with a matched 50-Ω load. Thus, the total effective load seen by the OPA2673 is 100 Ω || 402 Ω = 80 Ω.

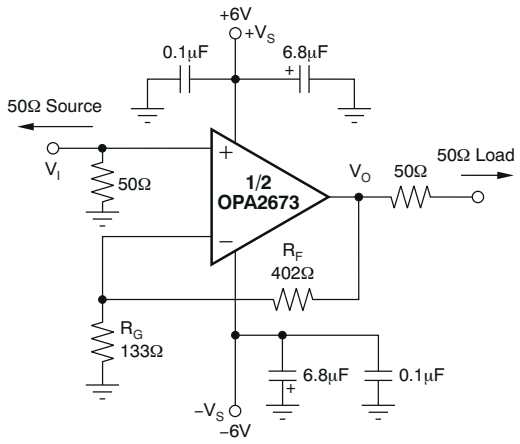


Figure 8-1. DC-Coupled, G = +4 V/V, Bipolar Supply

8.3.1 Operating Suggestions

8.3.1.1 Setting Resistor Values to Optimize Bandwidth

A current-feedback op amp such as the OPA2673 can hold an almost constant bandwidth over signal gain settings with the proper adjustment of the external resistor values, which are shown in the *Typical Characteristics*; the small-signal bandwidth decreases only slightly with increasing gain. These characteristic curves also show that the feedback resistor is changed for each gain setting. The absolute values of R_F on the inverting side of the circuit for a current-feedback op-amp can be treated as a frequency response compensation element, whereas the ratios of R_F and R_G set the signal gain.

Figure 8-2 shows the small-signal frequency response analysis circuit for the OPA2673.

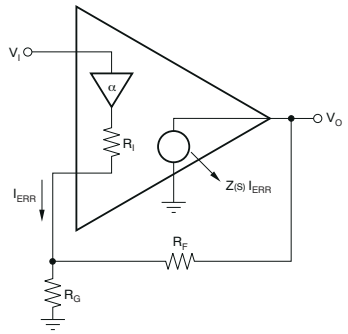


Figure 8-2. Current-Feedback Transfer Function Analysis Circuit

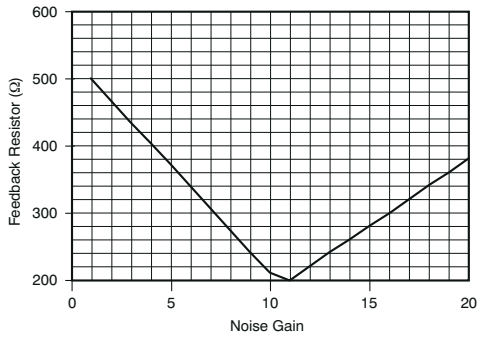


Figure 8-3. Feedback Resistor Versus Noise Gain

The key elements of this current-feedback op amp model are:

- α = buffer gain from the noninverting input to the inverting input
- R_I = buffer output impedance
- I_{ERR} = feedback error current signal
- Z(s) = frequency-dependent open-loop transimpedance gain from I_{ERR} to V_O

$$NG = \text{Noise Gain} = 1 + \frac{R_F}{R_G} \quad (1)$$

A current-feedback op amp senses an error current in the inverting node (as opposed to a differential input error voltage for a voltage-feedback op amp) and passes this on to the output through an internal frequency-dependent transimpedance gain. The *Typical Characteristics* show this open-loop transimpedance response, which is analogous to the open-loop voltage gain curve for a voltage-feedback op amp. Refer to the training videos shown in *TI Precision Labs* for further understanding on the CFA operating theory.

The values for R_F versus gain shown in Figure 8-3 are approximately equal to the values used to generate the *Typical Characteristics* and give a good starting point for designs where bandwidth optimization is desired.

8.3.1.2 Output Current and Voltage

The OPA2673 provides output voltage and current capabilities that are unsurpassed in a low-cost dual monolithic op amp. Under no-load conditions at +25°C, the output voltage typically swings closer than 1.1 V to either supply rail; the tested (+25°C) swing limit is within 1.2 V of either rail. The OPA2673 is capable of delivering around 700 mA of source and sink current at room temperature. Figure 8-4 and Figure 8-5 shows the relation between current output of the OPA2673 at different temperatures and maximum voltage swing at that current output under loaded conditions.

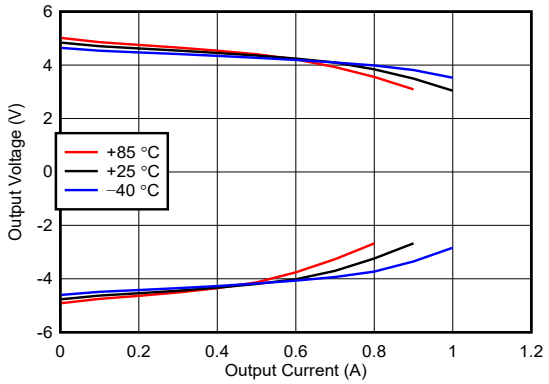


Figure 8-4. Output Headroom vs Output Current

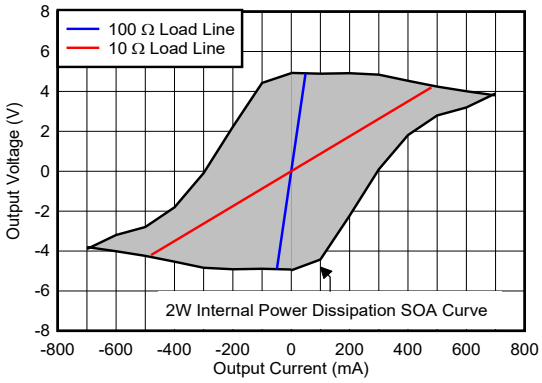


Figure 8-5. Output Voltage and Current Limitations

For the specifications described previously, consider voltage and current limits separately. In many applications, the voltage times the current (or V-I product) is more relevant to circuit operation. Figure 8-5 shows the zero-voltage output current limit and the zero-current output voltage limit on the X- and Y-axes, respectively. The four quadrants give a more detailed view of the OPA2673 output drive capabilities, noting that the graph is bounded by a safe operating area of 2-W maximum internal power dissipation (in this case, for one channel only). Superimposing resistor load lines onto the plot shows that the OPA2673 can drive ±4 V into 10 Ω or ±4.5 V into 25 Ω without exceeding the output capabilities or the 2-W dissipation limit. A 100-Ω load line (the standard test circuit load) shows the full ±4.8-V output swing capability, as stated in the *Electrical Characteristics*.

8.3.1.3 Driving Capacitive Loads

One of the most demanding and yet very common load conditions for an op amp is capacitive loading. The capacitive load is often the input of an analog-to-digital converter (ADC), including additional external capacitance that can be recommended to improve the ADC linearity. A high-speed, high-open-loop gain amplifier, such as the OPA2673, can be very susceptible to decreased stability and closed-loop response peaking when a capacitive load is placed directly on the output pin. When the amplifier open-loop output resistance is considered, this capacitive load introduces an additional pole in the signal path that can decrease the phase margin.

When the primary considerations are frequency-response flatness, pulse-response fidelity, and distortion, the simplest and most effective solution is to isolate the capacitive load (C_L) from the feedback loop by inserting a series isolation resistor (R_{ISO}) between the amplifier output and the capacitive load. Figure 8-6 shows this configuration. This approach does not eliminate the pole from the loop response, but rather shifts the pole and adds a zero at a higher frequency. The additional zero acts to cancel the phase lag from the capacitive load pole, thus increasing the phase margin and improving stability. Figure 8-7 shows the *Recommended R_{ISO} vs C_L*, and Figure 8-8 shows the resulting frequency response with the optimized R_{ISO} value.

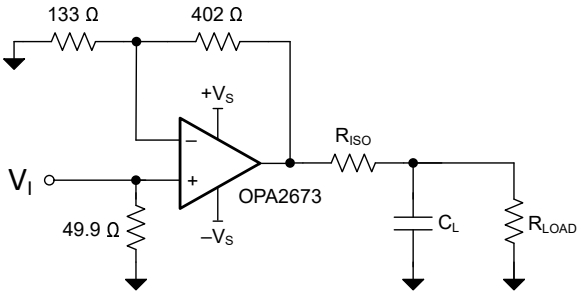


Figure 8-6. Driving a Large Capacitive Load Using an Output Series Isolation Resistor

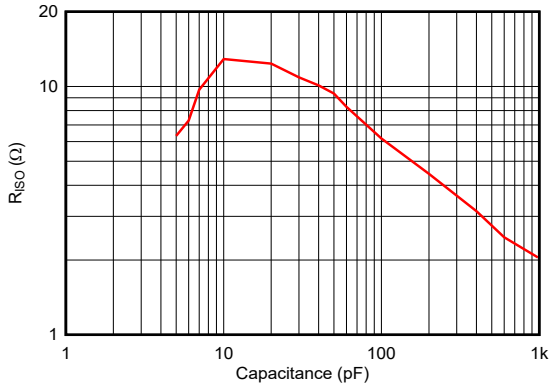


Figure 8-7. Recommended R_{ISO} vs Capacitive Load

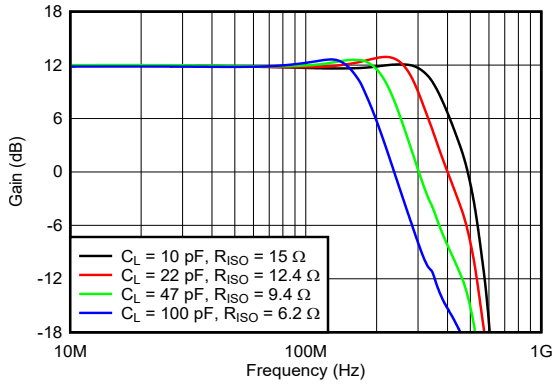


Figure 8-8. Frequency Response vs Capacitive Load

8.3.1.4 Line Driver Headroom Model

The first step in a driver design is to compute the peak-to-peak output voltage from the target specifications. This calculation is done using the following equations:

$$P_L = 10 \times \log \frac{V_{RMS}^2}{(1mW) \times R_L} \tag{2}$$

With P_L power and V_{RMS} voltage at the load, and R_L load impedance, this calculation gives:

$$V_{RMS} = \sqrt{(1mW) \times R_L \times 10^{\frac{P_L}{10}}} \tag{3}$$

$$V_P = \text{CrestFactor} \times V_{RMS} = CF \times V_{RMS} \tag{4}$$

With V_P peak voltage at the load and the crest factor, CF:

$$V_{LPP} = 2 \times CF \times V_{RMS} \tag{5}$$

With V_{LPP}: peak-to-peak voltage at the load.

Consolidating Equation 2 through Equation 5 allows the required peak-to-peak voltage at the load function of the crest factor, the load impedance, and the power in the load to be expressed. Thus:

$$V_{LPP} = 2 \times CF \times \sqrt{(1mW) \times R_L \times 10^{\frac{P_L}{10}}} \tag{6}$$

This V_{LPP} is usually computed for a nominal line impedance and can be taken as a fixed design target.

The next step for the driver is to compute the individual amplifier output voltage and currents as a function of V_{PP} on the line and transformer turns ratio. As the turns ratio changes, the minimum allowed supply voltage also changes. The peak current in the amplifier is given by:

$$\pm I_P = \frac{1}{2} \times \frac{2 \times V_{LPP}}{n} \times \frac{1}{4R_M} \tag{7}$$

With V_{LPP} defined in Equation 6 and R_M defined in Equation 8.

$$R_M = \frac{Z_{LINE}}{2n^2} \tag{8}$$

The peak current is computed in Figure 8-9 by noting that the total load is $4R_M$ and that the peak current is half of the peak-to-peak calculated using V_{LPP}.

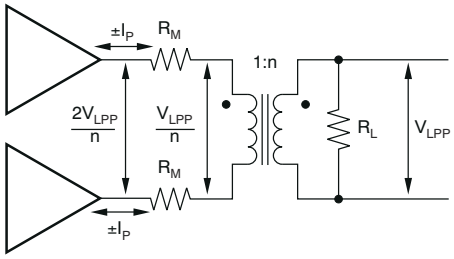


Figure 8-9. Driver Peak Output Model

With the required output voltage and current versus turns ratio set, an output stage headroom model allows the required supply voltage versus turns ratio to be developed.

The headroom model (see Figure 8-10) can be described with the following set of equations:

First, as available output voltage for each amplifier:

$$V_{OPP} = V_{CC} - (V_1 + V_2) - I_P \times (R_1 + R_2) \tag{9}$$

Or, second, as required single-supply voltage:

$$V_{CC} = V_{OPP} + (V_1 + V_2) + I_P \times (R_1 + R_2) \tag{10}$$

The minimum supply voltage for a set of power and load requirements is given by Equation 10, where V_1, V_2, R_1, and R_2 are internal to the OPA2673.

Table 8-1 gives V_1, V_2, R_1, and R_2 for +12-V operation of the OPA2673.

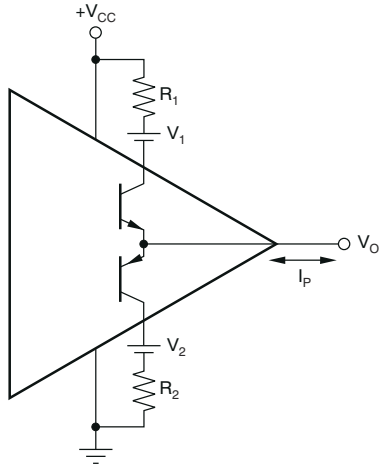


Figure 8-10. Line Driver Headroom Model

Table 8-1. Line Driver Headroom Model Values

V_1	R_1	V_2	R_2
0.9 V	2 Ω	0.9 V	2 Ω

8.3.1.5 Noise Performance

Wideband current-feedback op amps generally have a higher output noise than comparable voltage-feedback op amps. The OPA2673 offers an excellent balance between voltage and current noise terms to achieve low output noise. The low input voltage noise is achieved at the price of higher noninverting input current noise (3 pA/√ Hz). As long as the ac source impedance from the noninverting node is less than 100 Ω, this current noise does not contribute significantly to the total output noise. The op amp input voltage noise and the two input current noise terms combine to give low output noise under a wide variety of operating conditions. Figure 8-11 shows the op amp noise analysis model with all noise terms included. In this model, voltage noise and current noise have the units nV/√ Hz or pA/√ Hz.

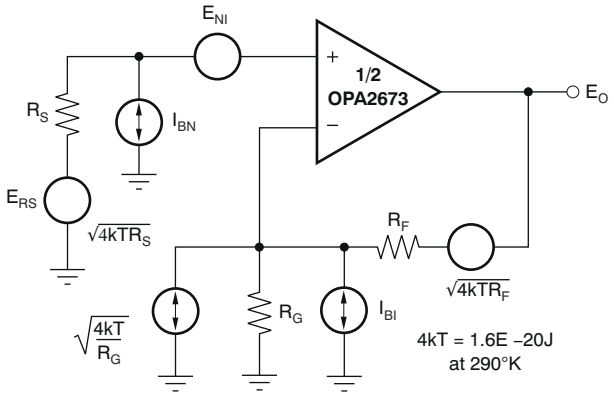


Figure 8-11. Op Amp Noise Analysis Model

The total output spot noise voltage can be computed as the square root of the sum of all squared output noise voltage contributors. Equation 11 shows the general form for the output noise voltage using the terms given in Figure 8-11.

$$E_O = \sqrt{\left[E_{NI}^2 + (I_{BN}R_S)^2 + 4kTR_S\right] \times NG + (I_{BI}R_F)^2 + 4kTR_FNG} \quad (11)$$

Dividing this expression by the noise gain [NG = (1 + R_F / R_G)] gives the equivalent input-referred spot noise voltage at the noninverting input, as shown in Equation 12.

$$E_I = \sqrt{E_{NI}^2 + (I_{BN} \times R_S)^2 + 4kTR_S + \frac{(I_{BI} \times R_F)^2}{NG^2} + \frac{4kTR_F}{NG}} \quad (12)$$

Evaluating these two equations for the OPA2673 circuit and component values of Figure 8-1 gives a total output spot noise voltage of 15.6 nV/√ Hz and a total equivalent input spot noise voltage of 3.9 nV/√ Hz. This total input-referred spot noise voltage is higher than the 2.4 nV/√ Hz specification for the op amp voltage noise alone. This result is due to the noise added to the output by the inverting current noise times the feedback resistor 402 Ω in this case. If the feedback resistor is reduced in high-gain configurations (as suggested previously), the total input-referred voltage noise given by Equation 12 approaches only the 2.4 nV/√ Hz of the op amp. For example, going to a gain of +8 V/V using R_F = 250 Ω gives a total input-referred noise of 2.9 nV/√ Hz.

8.4 Device Functional Modes

OPA2673 has four different functional modes set by the A0 and A1 pins. Table 8-2 shows the truth table for the device mode pin configuration and the associated description of each mode.

Table 8-2. A0 and A1 Logic Table

A0	A1	FUNCTION	DESCRIPTION
0	0	Full-bias mode (100%)	Both amplifiers are on with the lowest distortion possible
1	0	Mid-bias mode (75%)	Both amplifiers are on with power savings and a reduction in distortion performance
0	1	Low-bias mode (50%)	Both amplifiers are on with enhanced power savings and a reduction of overall performance
1	1	Offline mode	Both amplifiers are off and the output is high impedance

OPA2673 can be switched between the full-bias and offline mode using just one control bit by tying the A0 and A1 together. If switching between the mid-bias or low-bias modes and the offline mode is required for the application, then either the A0 or A1 pin can be connected to ground and the control pin can be connected to the non-grounded BIAS pin.

The OUT pin of OPA2673 enters high output impedance in offline mode. However, because of the presence of feedback resistor R_F (shown in Figure 8-12), the impedance detected by the load going into the OPA2673 is high impedance || R_F, making the net impedance as detected from the load equal to R_F. The maximum voltage allowed to be incident on the OUT pin and the Inverting Input pin during offline mode is mentioned in the *Absolute Maximum Ratings*. Figure 8-12 shows the voltage appearing on the Inverting Input pin is a resistor divided value of the voltage on the OUT pin. Make sure that both the absolute maximum limits mentioned for the OUT and Inverting pins are satisfied.

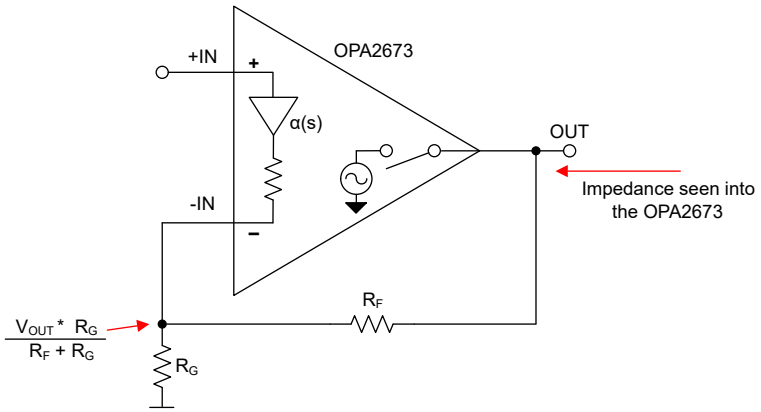


Figure 8-12. OPA2673 Offline Mode

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The OPA2673 is a high-speed, high-current output, current-feedback amplifier (CFA) that operates over a wide supply range of ±3.5 V to ±6.5 V. This device is designed for applications that require large-drive currents along with a wide bandwidth. The two channels of the OPA2673 can be used as two independent amplifiers or can be connected in a differential-input to differential-output configuration.

9.2 Typical Applications

9.2.1 High-Speed Active Filter

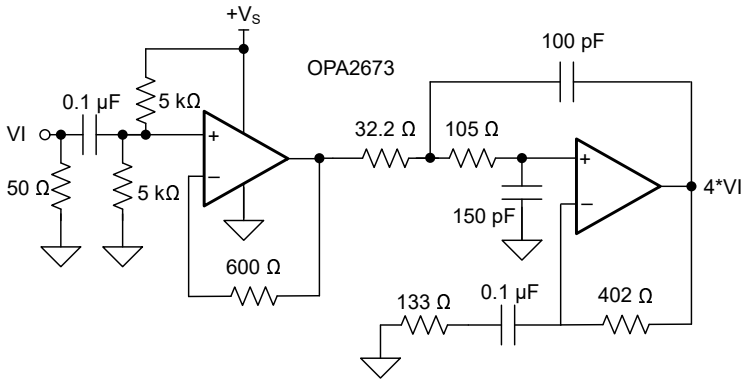


Figure 9-1. Buffered Single-Supply Active Filter

9.2.1.1 Design Requirements

Wideband current-feedback op amps make ideal elements for implementing high-speed active filters where the amplifier is used as a fixed gain block inside a passive RC circuit network. The relatively constant bandwidth versus gain provides low interaction between the actual filter poles and the required gain for the amplifier. shows an example single-supply buffered filter application. In this case, one of the OPA2673 channels is used to set up the dc operating point and provide impedance isolation from the signal source into the second-stage filter. That stage is set up to implement a 20 MHz, maximally flat Butterworth frequency response and provide an ac gain of +4 V/V.

9.2.1.2 Detailed Design Procedure

The 51 Ω input matching resistor is optional in this case. The input signal is ac-coupled to the 5-V dc reference voltage developed through the resistor divider from the 10-V power supply. This first stage acts as a gain of +1-V/V voltage buffer for the signal where the 600-Ω feedback resistor is required for stability. This first stage easily drives the low input resistors required at the input of this high-frequency filter. The second stage is set for a dc gain of +1 V/V, carrying the 5-V operating point through to the output pin, and an ac gain of +4 V/V. The feedback resistor has been adjusted to optimize bandwidth for the amplifier itself. Figure 9-1 and Figure 9-2 show that the OPA2673 in this configuration gives greater than 400-MHz small-signal bandwidth. Choose capacitor values as low as possible but adequate to override the parasitic input capacitance of the amplifier. The resistor values were slightly adjusted to give the desired filter frequency response while accounting for the approximate 1-ns propagation delay through each channel of the OPA2673.

9.2.1.3 Application Curve

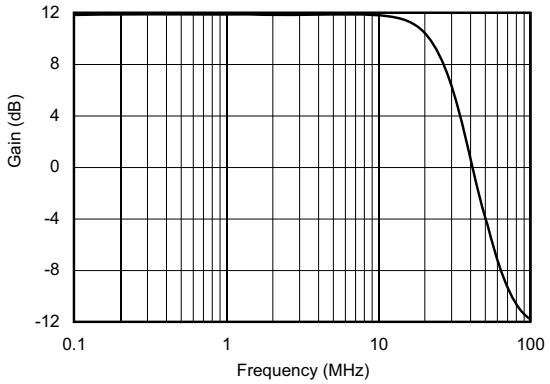


Figure 9-2. Buffered Single-Supply Active Filter: Gain vs Frequency

9.2.2 PLC Line Driver

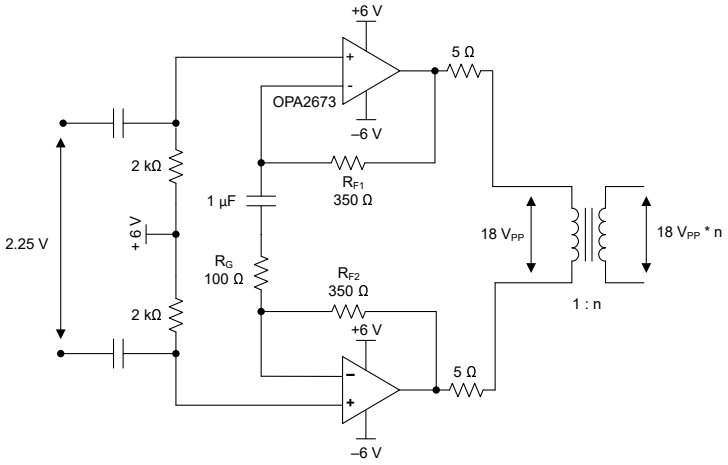


Figure 9-3. Typical Schematic for PLC Applications

9.2.2.1 Design Requirements

The main design requirements for an ac-coupled wideband current-feedback operation are power supplies that satisfy the output voltage requirement, and to use a feedback resistor value that allows for the proper bandwidth while maintaining stability. Use the requirements shown in Table 9-1 to design a broadband PLC application circuit.

Table 9-1. Design Requirements

DESIGN PARAMETER	VALUE
Power supply	12 V, single-supply
Differential gain G_{DIFF}	8 V/V
Output voltage	18 V_{PP}
Large-signal bandwidth	220 MHz

9.2.2.2 Detailed Design Procedure

The closed-loop gain equation for a differential line driver configuration is given as $G_{DIFF} = 1 + 2 \times (R_F / R_G)$, where $R_F = R_{F1} = R_{F2}$. The OPA2673 is a current-feedback amplifier and thus the bandwidth of the closed-loop configuration is set by the value of the R_F resistor. This advantage of the current-feedback architecture allows for flexibility in setting the differential gain by choosing the value of the R_G resistor without reducing the bandwidth, as is the case with voltage-feedback amplifiers. The OPA2673 is designed to provide excellent bandwidth performance with $R_{F1} = R_{F2} = 350\ \Omega$. To configure the device in a gain of 8 V/V, use a 100-Ω R_G resistor.

9.2.2.3 Application Curve

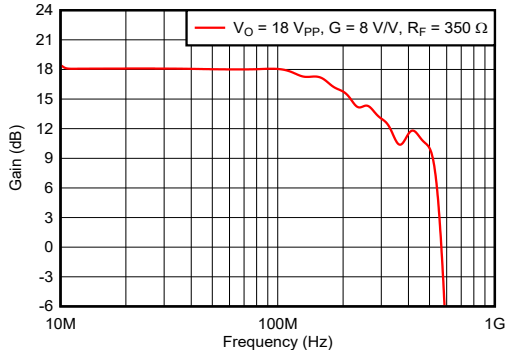


Figure 9-4. Large-Signal Frequency Response

9.3 Power Supply Recommendations

9.3.1 Thermal Analysis

As a result of the high-output power capability of the OPA2673, heat-sinks or forced airflow can be required under extreme operating conditions. The maximum desired junction temperature sets the maximum allowed internal power dissipation, and is described in the following paragraph. Do not exceed the maximum junction temperature of 150°C.

Operating junction temperature (T_J) is given by:

$$T_J = T_A + P_D \times \theta_{JA} \quad (13)$$

The total internal power dissipation (P_D) is the sum of quiescent power (P_{DQ}) and additional power dissipation in the output stage (P_{DL}) to deliver load power. Quiescent power is the specified no-load supply current times the total supply voltage across the part. The P_{DL} depends on the required output signal and load; however, P_{DL} is at a maximum when the output is fixed at a voltage equal to 1/2 of either supply voltage (for equal bipolar supplies). Under this condition,

$$P_{DL} = V_S{}^2 / (4 \times R_L) \quad (14)$$

where R_L includes feedback network loading.

Equation 14 is the power dissipated at the output stage of OPA2673 that determines the internal power dissipation.

As a worst-case example, compute the maximum T_J using an OPA2673 VQFN-16 in the circuit of Figure 8-1 operating at the maximum specified ambient temperature of 85°C with both outputs driving a grounded 20-Ω load to 2.5 V.

$$P_D = 12\ V \times 33\ mA + 2 \times [5^2 / (4 \times [20\ \Omega \parallel 535\ \Omega])] = 1.05\ W \quad (15)$$

$$\text{Maximum } T_J = +85°C + (1.05 \times 45°C/W) = 132.2°C \quad (16)$$

The output V-I plot in *Output Current and Voltage* includes a boundary for 2-W maximum internal power dissipation under these conditions.

9.3.2 Input and ESD Protection

The OPA2673 is built using a high-speed complementary bipolar process. The internal junction breakdown voltages are shown in the *Absolute Maximum Ratings*. All device pins have limited ESD protection using internal diodes to the power supplies, as shown in Figure 9-5.

These diodes provide moderate protection to input overdrive voltages above the supplies as well. The protection diodes typically support a 10-mA continuous current. Where higher currents are possible (for example, in systems with ±15-V supply parts driving into the OPA2673), add current-limiting series resistors into the two inputs.

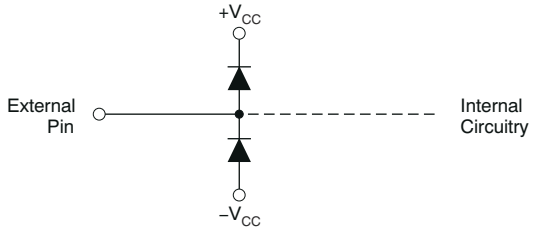


Figure 9-5. ESD Steering Diodes

9.4 Layout

9.4.1 Layout Guidelines

Achieving optimum performance with a high-frequency amplifier such as the OPA2673 requires careful attention to board layout parasitic and external component types.

a) Minimize parasitic capacitance to any ac ground for all of the signal I/O pins. Parasitic capacitance on the output and inverting input pins can cause instability; on the noninverting input, parasitic capacitance can react with the source impedance to cause unintentional band limiting. To reduce unwanted capacitance, open a window around the signal I/O pins in all of the ground and power planes around those pins. Otherwise, make sure that ground and power planes are unbroken elsewhere on the board.

b) Minimize the distance (< 0.25 inches or 6.35 0 mm) from the power-supply pins to high-frequency, 0.1-µF decoupling capacitors. Always decouple the power-supply connections (on pins 7 and 14 for a VQFN package) with low-ESR capacitors. Do not have the ground and power-plane layout in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. An optional supply decoupling capacitor connected across the two power supplies (for bipolar operation) improves second-harmonic distortion performance.

c) Careful selection and placement of external components preserve the high-frequency performance of the OPA2673. Use very low reactance resistors. Surface-mount resistors, metal film, and carbon-composition-based axially-leaded resistors can provide good high-frequency performance. Keep the leads and PCB trace length as short as possible. Although the output pin and inverting input pin are the most sensitive to parasitic capacitance, always position the feedback and series output resistor, if any, as close as possible to the output pin. Where double-side component mounting is allowed, place the feedback resistor directly under the package on the other side of the board between the output and inverting input pins.

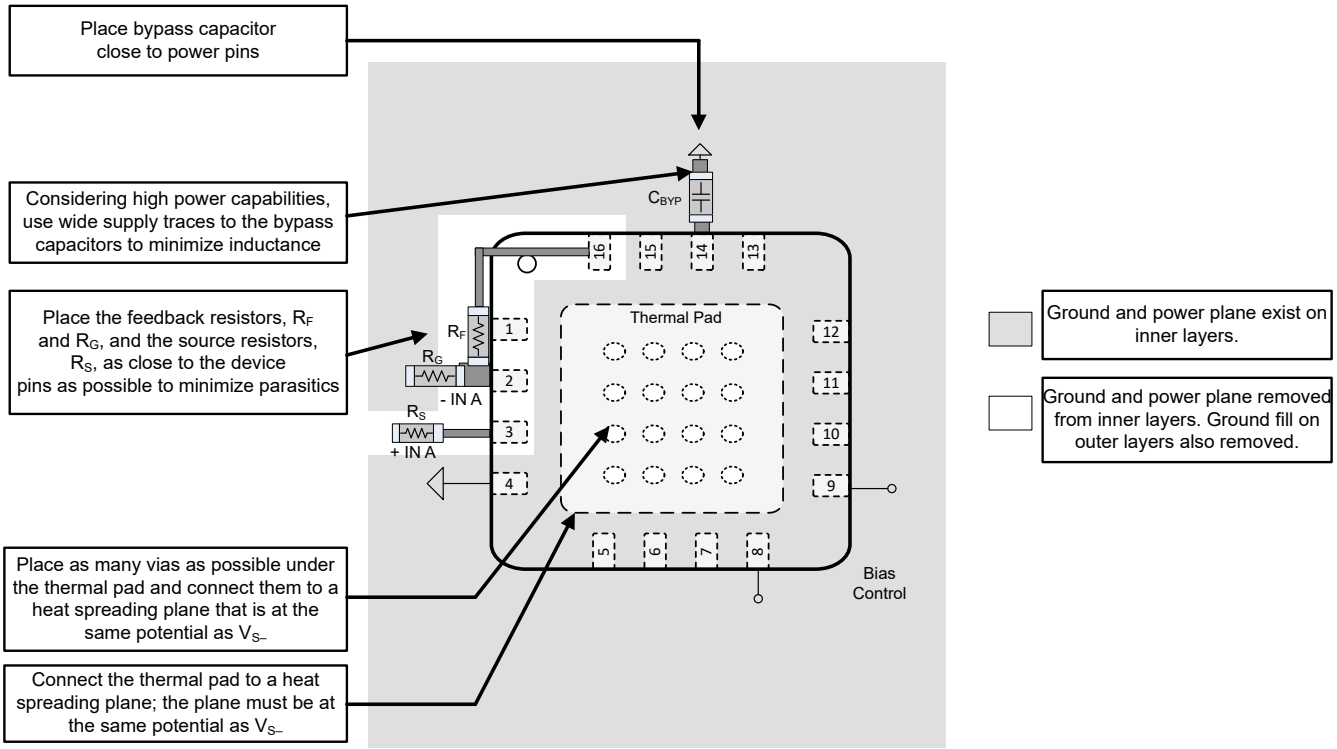
d) The frequency response is primarily determined by the feedback resistor value as described previously. Increasing the value reduces the bandwidth, whereas decreasing the value gives a more peaked frequency response. The 402-Ω feedback resistor used in the *Typical Characteristics* at a gain of +4 V/V on ±6-V supplies is a good starting point for design. Note that a current-feedback op amp requires a feedback resistor even in the unity-gain follower configuration to control stability. Use a 511-Ω feedback resistor, rather than a direct short, for the unity-gain follower application.

e) Connections to other wideband devices on the board can be made with short, direct traces or through onboard transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Use relatively wide traces (50 mils to 100 mils, or 1.27 mm to 2.54 mm), preferably with ground and power planes opened up around them. Estimate the total capacitive load and set R_{ISO} from the plot of Figure 8-7. Low-parasitic capacitive loads (< 5 pF) may not need an R_{ISO} because the OPA2673 is nominally compensated to operate with a 2-pF parasitic load.

If a long trace is required, and the 6-dB signal loss intrinsic to a doubly-terminated transmission line is acceptable, implement a matched-impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques).

The high output voltage and current capability of the OPA2673 allows multiple destination devices to be handled as separate transmission lines, each with respective series and shunt terminations. If the 6-dB attenuation of a doubly-terminated transmission line is unacceptable, a long trace can be series-terminated at the source end only.

9.4.2 Layout Example



Layout Recommendations have been shown for Channel A only, follow similar precautions for Channel B.

Figure 9-6. Layout Recommendations

10 Device and Documentation Support

10.1 Device Support

10.1.1 Development Support

10.1.1.1 TINA-TI™ Simulation Software (Free Download)

TINA-TI™ simulation software is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI simulation software is a free, fully-functional version of the TINA™ software, preloaded with a library of macromodels, in addition to a range of both passive and active models. TINA-TI simulation software provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Design tools and simulation web page, TINA-TI simulation software offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

Note

These files require that either the TINA software or TINA-TI software be installed. Download the free TINA-TI simulation software from the TINA-TI™ software folder.

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.4 Trademarks

TINA-TI™ and TI E2E™ are trademarks of Texas Instruments.
TINA™ is a trademark of DesignSoft, Inc.
All trademarks are the property of their respective owners.

10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2673IRGVR	ACTIVE	VQFN	RGV	16	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2673	Samples
OPA2673IRGVT	ACTIVE	VQFN	RGV	16	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2673	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

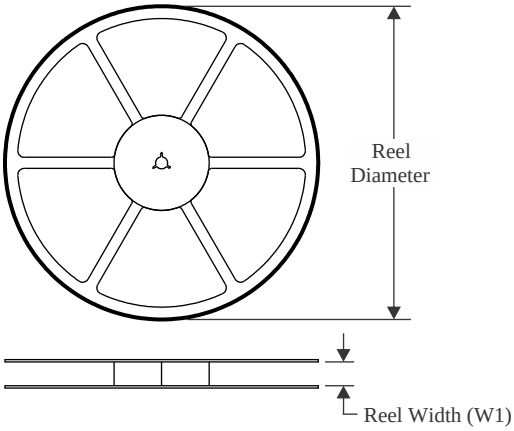
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

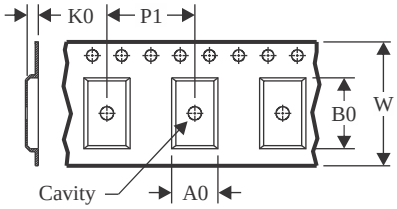
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

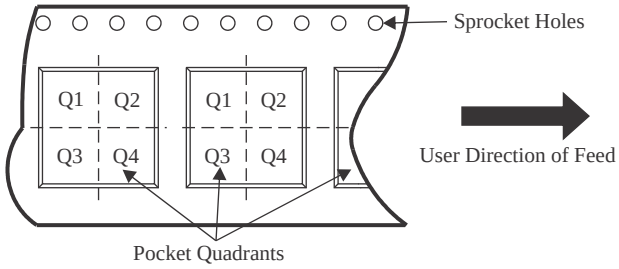


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

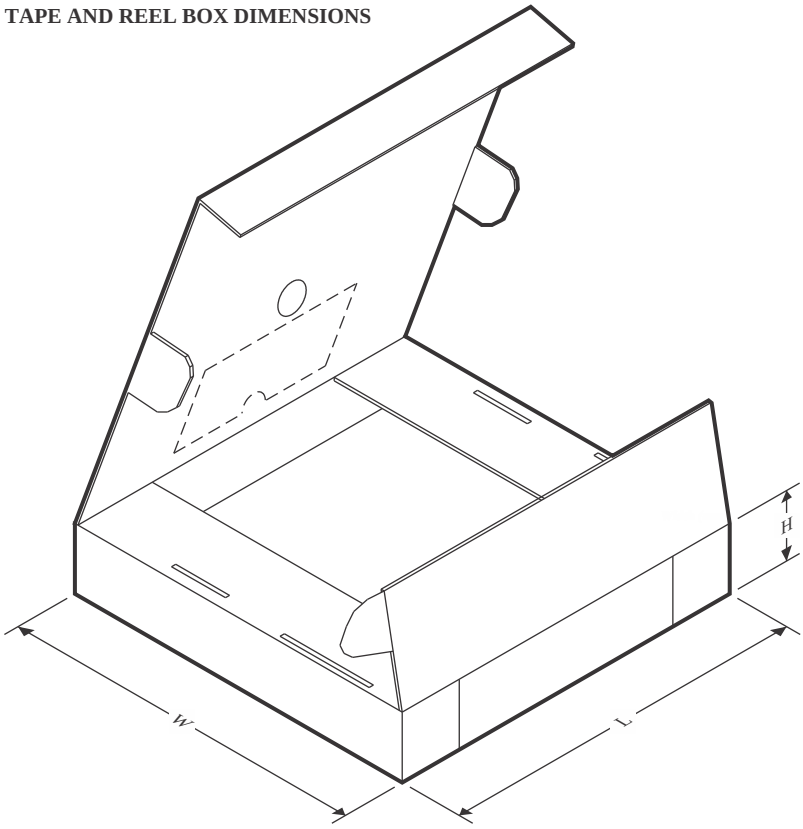
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2673IRGVR	VQFN	RGV	16	2500	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
OPA2673IRGVT	VQFN	RGV	16	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2673IRGVR	VQFN	RGV	16	2500	367.0	367.0	35.0
OPA2673IRGVT	VQFN	RGV	16	250	210.0	185.0	35.0

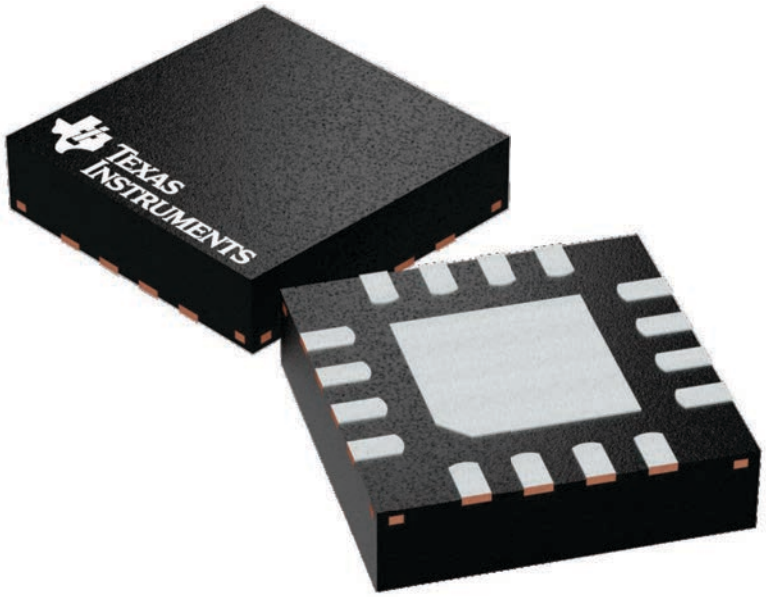
GENERIC PACKAGE VIEW

RGV 16

VQFN - 1 mm max height

4 x 4, 0.65 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

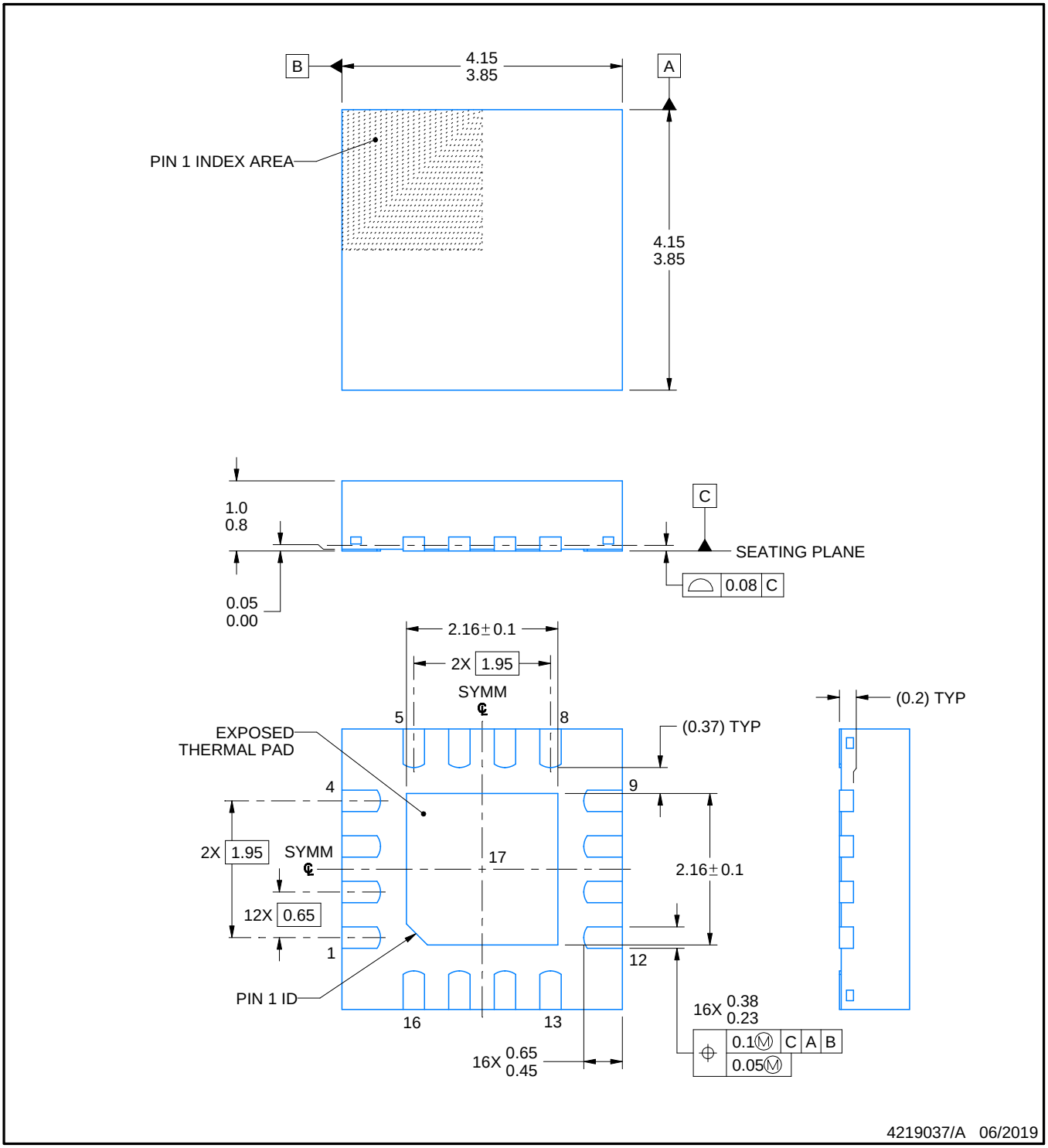
4224748/A

RGV0016A

PACKAGE OUTLINE

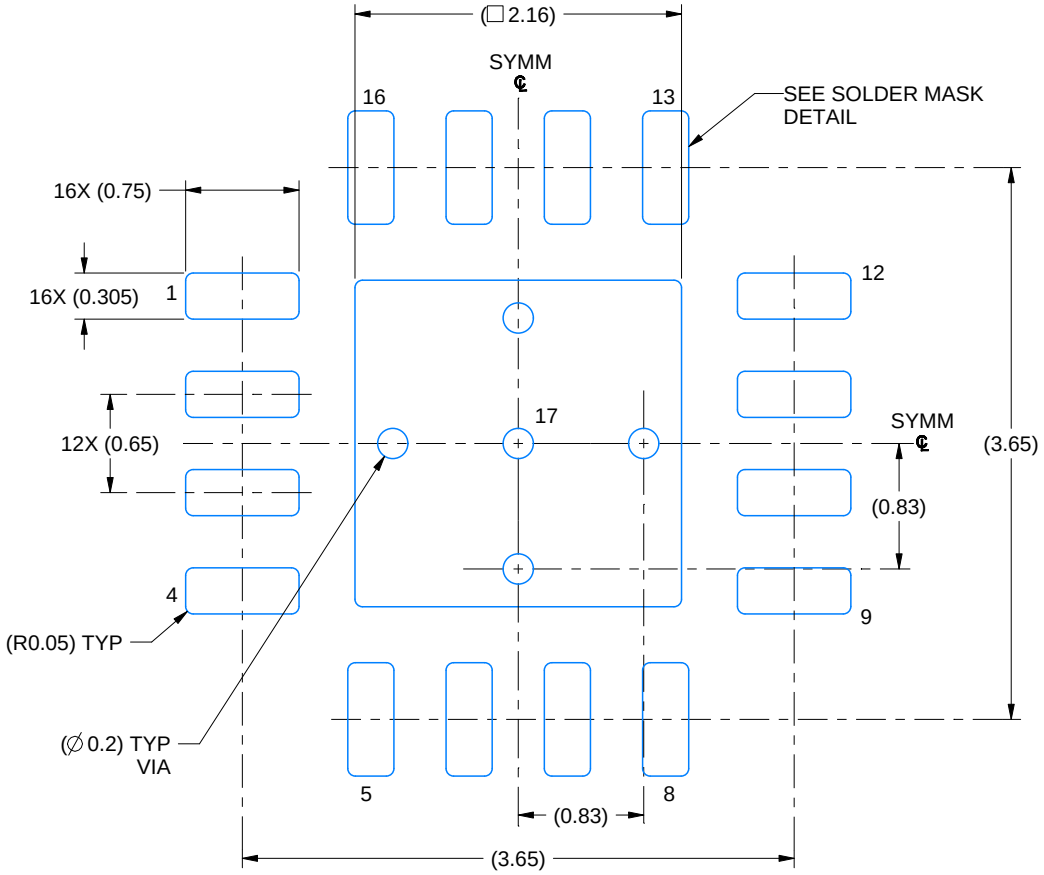
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

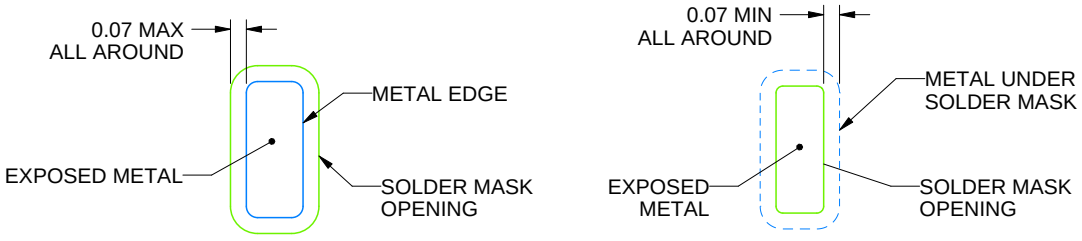


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



NON SOLDER MASK DEFINED (PREFERRED)

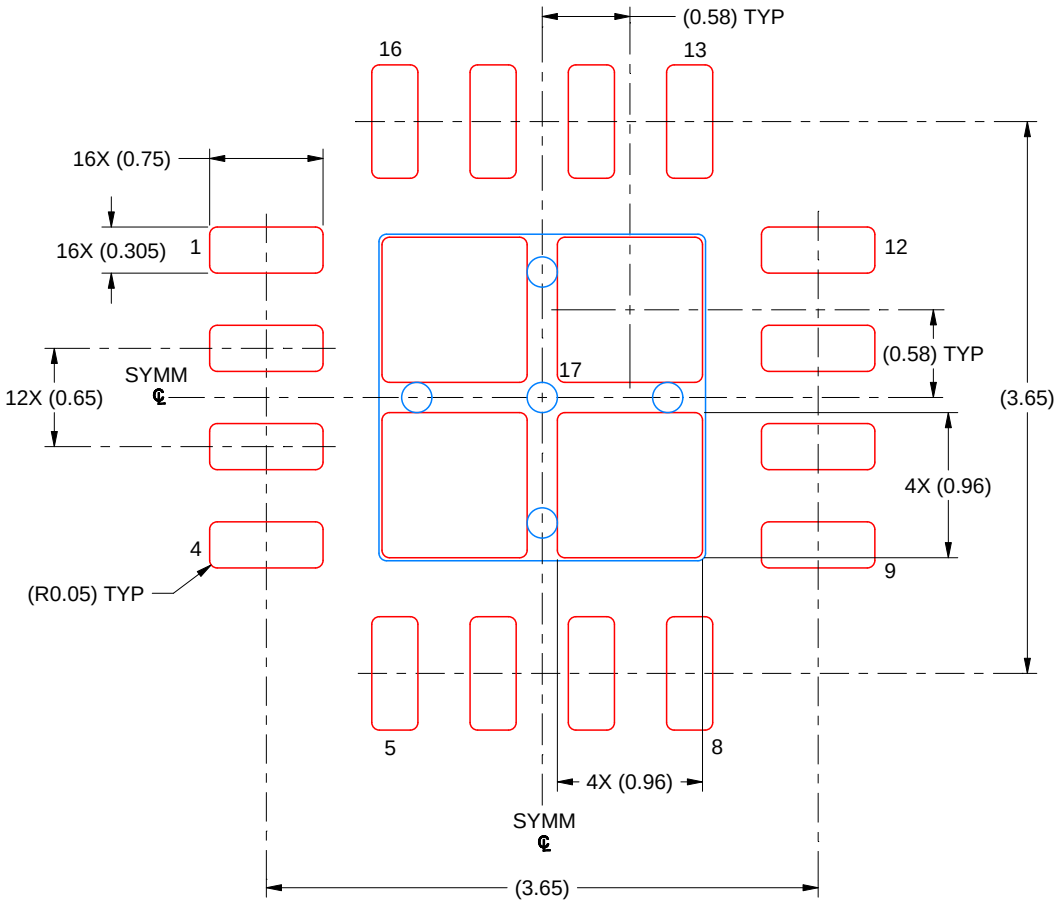
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4219037/A 06/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 17
79% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4219037/A 06/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265