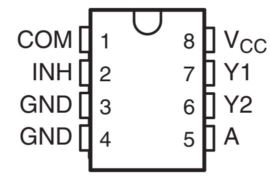
SINGLE-POLE DOUBLE-THROW (SPDT) ANALOG SWITCH OR 2:1 ANALOG MULTIPLEXER/DEMULTIPLEXER

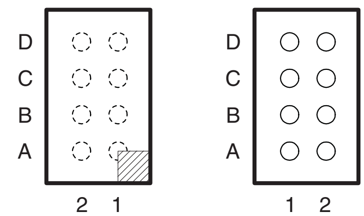
FEATURES

- **Available in the Texas Instruments NanoFree™ Package**
- **Operates at 0.8 V to 2.7 V**
- **Sub-1-V Operable**
- **Low Power Consumption, 10 μA at 2.7 V**
- **High On-Off Output Voltage Ratio**
- **High Degree of Linearity**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

DCT OR DCU PACKAGE (TOP VIEW)



YZP PACKAGE



Laser Marking View   Bump View

YZP TERMINAL ASSIGNMENTS

D	GND	A
C	GND	Y2
B	INH	Y1
A	COM	V_{CC}
	1	**2**

DESCRIPTION/ORDERING INFORMATION

This analog switch is operational at 0.8-V to 2.7-V V_{CC}, but is designed specifically for 1.1-V to 2.7-V V_{CC} operation.

The SN74AUC2G53 can handle both analog and digital signals. The device permits signals with amplitudes of up to V_{CC} (peak) to be transmitted in either direction.

NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

Applications include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.

ORDERING INFORMATION

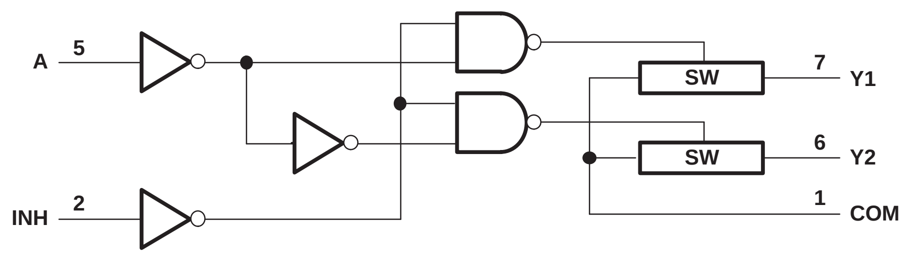
T_A	PACKAGE[1][2]		ORDERABLE PART NUMBER	TOP-SIDE MARKING[3]
–40C to 85C	NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)	Reel of 3000	SN74AUC2G53YZPR	_ _ _U4_
	SSOP – DCT	Reel of 3000	SN74AUC2G53DCTR	U53_ _ _
	VSSOP – DCU	Reel of 3000	SN74AUC2G53DCUR	U53_

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(3) DCT: The actual top-side marking has three additional characters that designate the year, month, and assembly/test site.
DCU: The actual top-side marking has one additional character that designates the assembly/test site.
YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).

FUNCTION TABLE

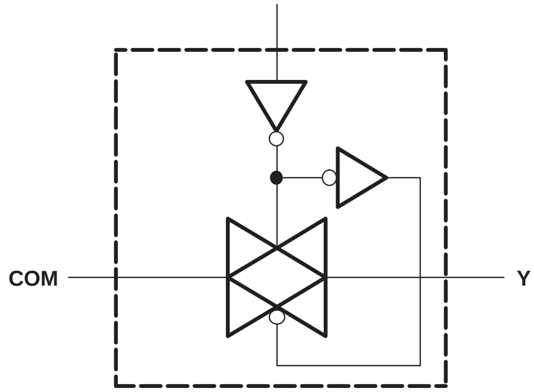
CONTROL INPUTS		ON CHANNEL
INH	A	
L	L	Y1
L	H	Y2
H	X	None

LOGIC DIAGRAM (POSITIVE LOGIC)



NOTE A: For simplicity, the test conditions shown in Figures 1 through 4 and 6 through 10 are for the demultiplexer configuration. Signals may be passed from COM to Y1 (Y2) or from Y1 (Y2) to COM.

SIMPLIFIED SCHEMATIC, EACH SWITCH (SW)



Absolute Maximum Ratings[1]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range[2]		–0.5	3.6	V
V_I	Input voltage range[2][3]		–0.5	3.6	V
$V_{I/O}$	Switch I/O voltage range[2][3]		–0.5	V_{CC} + 0.5	V
I_{IK}	Control input clamp current	V_I < 0		–50	mA
$I_{I/OK}$	I/O port diode current	$V_{I/O}$ < 0 or $V_{I/O}$ > V_{CC}		50	mA
I_T	On-state switch current current	$V_{I/O}$ = 0 to V_{CC}		50	mA
	Continuous current through V_{CC} or GND			100	mA
θ_{JA}	Package thermal impedance[4]	DCT package		220	C/W
		DCU package		227	
		YZP package		102	
T_{stg}	Storage temperature range		–65	150	C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground unless otherwise specified.
(3) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage		0.8	2.7	V
V_{IH}	High-level input voltage	V_{CC} = 0.8 V	V_{CC}		V
		V_{CC} = 1.1 V to 1.95 V	0.65 ıV_{CC}		
		V_{CC} = 2.3 V to 2.7 V	1.7		
V_{IL}	Low-level input voltage	V_{CC} = 0.8 V		0	V
		V_{CC} = 1.1 V to 1.95 V		0.35 ıV_{CC}	
		V_{CC} = 2.3 V to 2.7 V		0.7	
$V_{I/O}$	I/O port voltage		0	V_{CC}	V
V_I	Control input voltage		0	3.6	V
Δt/Δv	Input transition rise or fall rate	V_{CC} = 0.8 V to 1.6 V		20	ns/V
		V_{CC} = 1.65 V to 1.95 V		10	
		V_{CC} = 2.3 V to 2.7 V		3.5	
T_A	Operating free-air temperature		–40	85	C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP[1]	MAX	UNIT
r_{on}	On-state switch resistance	V_I = V_{CC} or GND, V_{INH} = V_{IL} (see Figure 1 and Figure 2)	I_S = 4 mA	1.1 V			40	Ω
				1.65 V		12.5	20	
			I_S = 8 mA	2.3 V		6	15	
$r_{on(p)}$	Peak on resistance	V_I = V_{CC} to GND, V_{INH} = V_{IL} (see Figure 1 and Figure 2)	I_S = 4 mA	1.1 V		131	180	Ω
				1.65 V		32	80	
			I_S = 8 mA	2.3 V		15	20	

(1) T_A = 25C

Electrical Characteristics (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		V_{CC}	MIN	TYP[(1)]	MAX	UNIT
Δr_{on}	Difference of on-state resistance between switches		$V_I = V_{CC}$ to GND, $V_C = V_{IH}$ (see Figure 1 and Figure 2)	I_S = 4 mA	1.1 V			4	Ω
					1.65 V			1	
				I_S = 8 mA	2.3 V			1	
$I_{S(off)}$	Off-state switch leakage current		$V_I = V_{CC}$ and V_O = GND, or V_I = GND and $V_O = V_{CC}$, $V_{INH} = V_{IH}$ (see Figure 3)		2.7 V			1	µA
								0.1[(1)]	
$I_{S(on)}$	On-state switch leakage current		$V_I = V_{CC}$ or GND, $V_{INH} = V_{IL}$, V_O = Open (see Figure 4)		2.7 V			1	µA
								0.1[(1)]	
I_I	Control input current		$V_C = V_{CC}$ or GND		2.7 V			5	µA
I_{CC}	Supply current		$V_C = V_{CC}$ or GND		2.7 V			10	µA
C_{ic}	Control input capacitance				2.5 V		2		pF
$C_{io(off)}$	Switch input/output capacitance	Y			2.5 V		3		pF
		COM					4.5		
$C_{io(on)}$	Switch input/output capacitance				2.5 V		9		pF

Switching Characteristics

over recommended operating free-air temperature range, C_L = 15 pF (unless otherwise noted) (see Figure 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 0.8 V	V_{CC} = 1.2 V ± 0.1 V		V_{CC} = 1.5 V ± 0.1 V		V_{CC} = 1.8 V ± 0.15 V			V_{CC} = 2.5 V ± 0.2 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX	
t_{pd}[(1)]	COM or Y	Y or COM	0.3		0.3		0.3			0.2		0.1	ns
t_{en}	INH	COM or Y	9.2	0.5	3.5	0.5	2.2	0.5	1	1.9	0.5	1.8	ns
t_{dis}			8.1	0.5	4.2	0.5	3.2	0.5	1.9	3.4	0.5	2.6	
t_{en}	A	COM or Y	9.2	0.5	3.6	0.5	2.3	0.5	1.1	1.9	0.5	1.6	ns
t_{dis}			10	0.5	3.6	0.5	2.3	0.5	1.1	2	0.5	1.6	

(1) The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

Switching Characteristics

over recommended operating free-air temperature range, C_L = 30 pF (unless otherwise noted) (see Figure 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 1.8 V ± 0.15 V			V_{CC} = 2.5 V ± 0.2 V		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{pd}[(1)]	COM or Y	Y or COM			0.4		0.2	ns
t_{en}	INH	COM or Y	0.5	1.6	3.1	0.5	2.2	ns
t_{dis}			0.5	2.2	3.4	0.5	2.2	
t_{en}	A	COM or Y	0.5	1.6	3	0.5	2.2	ns
t_{dis}			0.5	1.6	3	0.5	2.3	

(1) The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

Analog Switch Characteristics

T_A = 25C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CC}	TYP	UNIT
Frequency response(1) (switch ON)	COM or Y	Y or COM	C_L = 50 pF, R_L = 600 Ω, f_{in} = sine wave (see Figure 6)	0.8 V	90	MHz
				1.1 V	101	
				1.4 V	110	
				1.65 V	122	
				2.3 V	198	
			C_L = 5 pF, R_L = 50 Ω, f_{in} = sine wave (see Figure 6)	0.8 V	>500	
				1.1 V	>500	
				1.4 V	>500	
				1.65 V	>500	
				2.3 V	>500	
Crosstalk(2) (between switches)	COM or Y	Y or COM	C_L = 50 pF, R_L = 600 Ω, f_{in} = 1 MHz (sine wave) (see Figure 7)	0.8 V	–59	dB
				1.1 V	–59	
				1.4 V	–59	
				1.65 V	–59	
				2.3 V	–60	
			C_L = 5 pF, R_L = 50 Ω, f_{in} = 1 MHz (sine wave) (see Figure 7)	0.8 V	–55	
				1.1 V	–55	
				1.4 V	–55	
				1.65 V	–55	
				2.3 V	–55	
Crosstalk (control input to signal output)	INH	COM or Y	C_L = 50 pF, R_L = 600 Ω, f_{in} = 1 MHz (square wave) (see Figure 8)	0.8 V	0.56	mV
				1.1 V	0.68	
				1.4 V	0.81	
				1.65 V	0.93	
				2.3 V	1.5	
Feed-through attenuation(3) (switch OFF)	COM or Y	Y or COM	C_L = 50 pF, R_L = 600 Ω, f_{in} = 1 MHz (sine wave) (see Figure 9)	0.8 V	–60	dB
				1.1 V	–60	
				1.4 V	–60	
				1.65 V	–60	
				2.3 V	–60	
			C_L = 5 pF, R_L = 600 Ω, f_{in} = 1 MHz (sine wave) (see Figure 9)	0.8 V	–59	
				1.1 V	–59	
				1.4 V	–59	
				1.65 V	–59	
				2.3 V	–59	

(1) Adjust f_{in} voltage to obtain 0 dBm at output. Increase f_{in} frequency until dB meter reads –3 dB.
(2) Adjust f_{in} voltage to obtain 0 dBm at input.
(3) Adjust f_{in} voltage to obtain 0 dBm at input.

Analog Switch Characteristics (continued)

T_A = 25C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CC}	TYP	UNIT
Sine-wave distortion	COM or Y	Y or COM	C_L = 50 pF, R_L = 10 kΩ, f_{in} = 1 kHz (sine wave) (see Figure 10)	0.8 V	6.19	%
				1.1 V	0.39	
				1.4 V	0.06	
				1.65 V	0.02	
				2.3 V	0.01	
			C_L = 50 pF, R_L = 10 kΩ, f_{in} = 10 kHz (sine wave) (see Figure 10)	0.8 V	3.55	
				1.1 V	0.38	
				1.4 V	0.04	
				1.65 V	0.02	
				2.3 V	0.02	

Operating Characteristics

for INH input, T_A = 25C

PARAMETER		TEST CONDITIONS	V_{CC} = 0.8 V	V_{CC} = 1.2 V	V_{CC} = 1.5 V	V_{CC} = 1.8 V	V_{CC} = 2.5 V	UNIT
			TYP	TYP	TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance	f = 10 MHz	3	3	3	3	3	pF

Operating Characteristics

for A input, T_A = 25C

PARAMETER			TEST CONDITIONS	V_{CC} = 0.8 V	V_{CC} = 1.2 V	V_{CC} = 1.5 V	V_{CC} = 1.8 V	V_{CC} = 2.5 V	UNIT
				TYP	TYP	TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance	Outputs enabled	f = 10 MHz	5.5	5.5	5.5	5.5	5.5	pF
		Outputs disabled		0.5	0.5	0.5	0.5	0.5	

PARAMETER MEASUREMENT INFORMATION

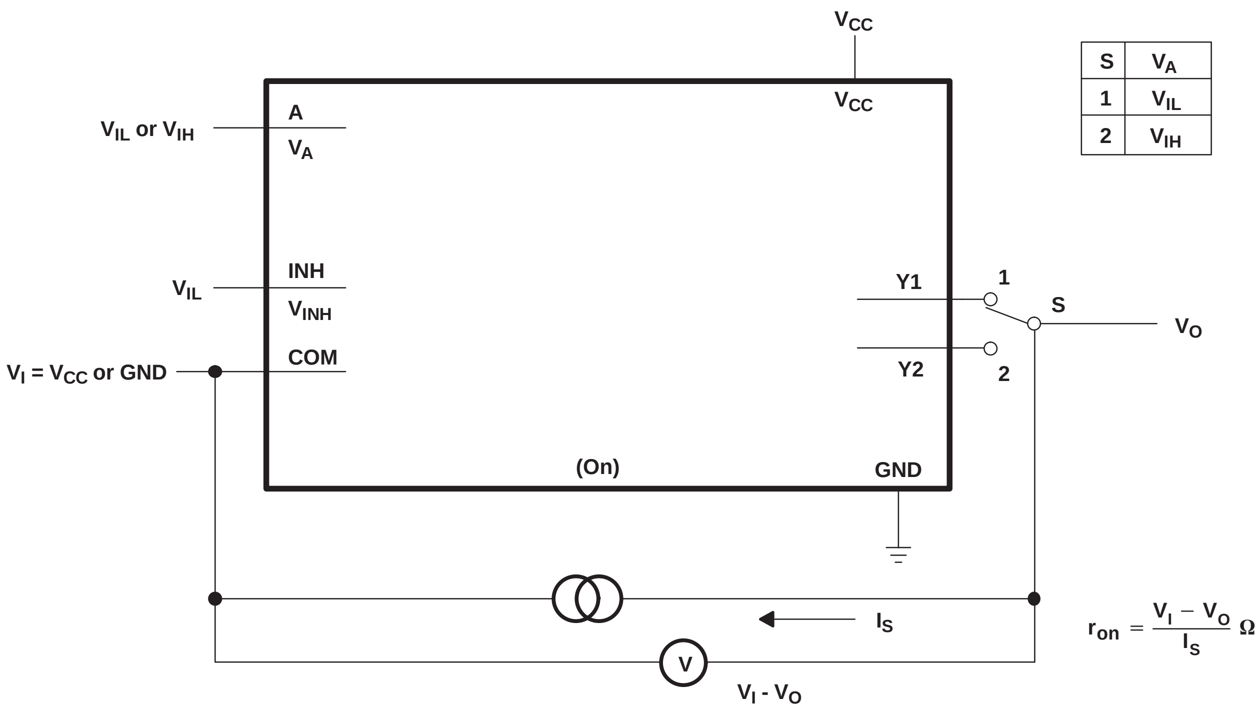


Figure 1. On-State Resistance Test Circuit

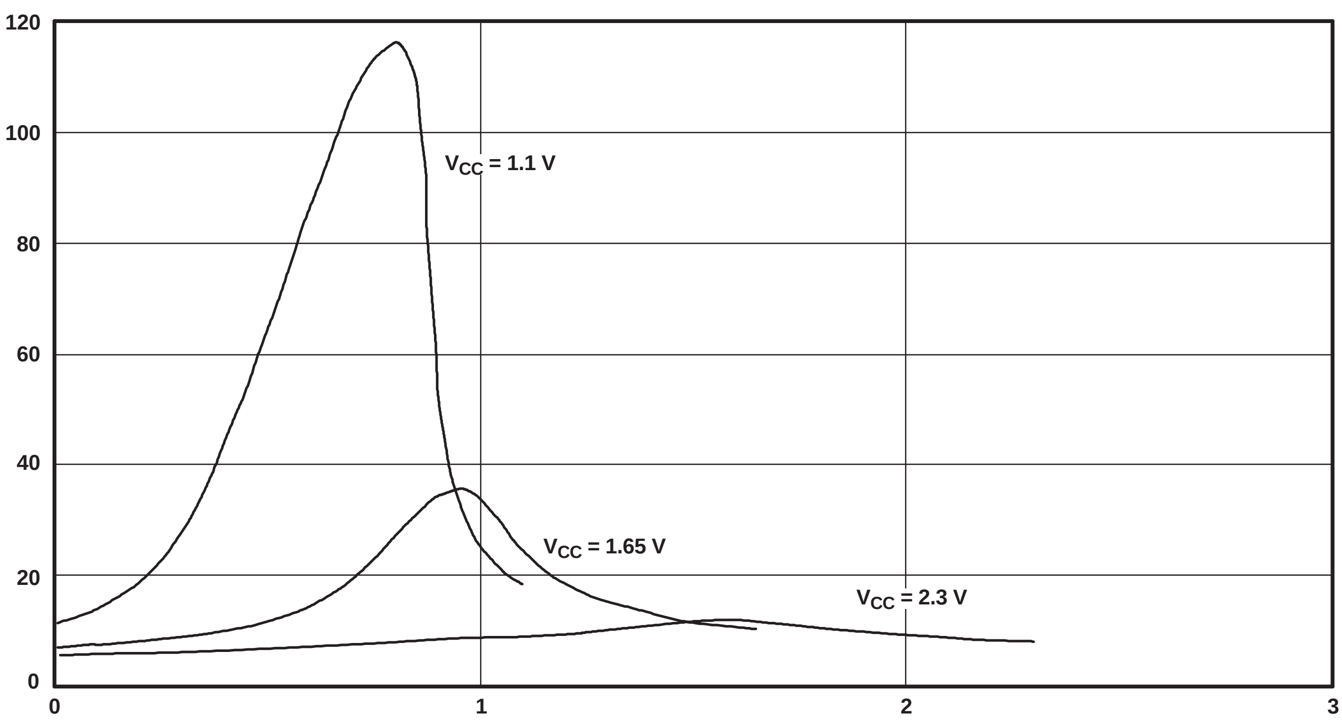
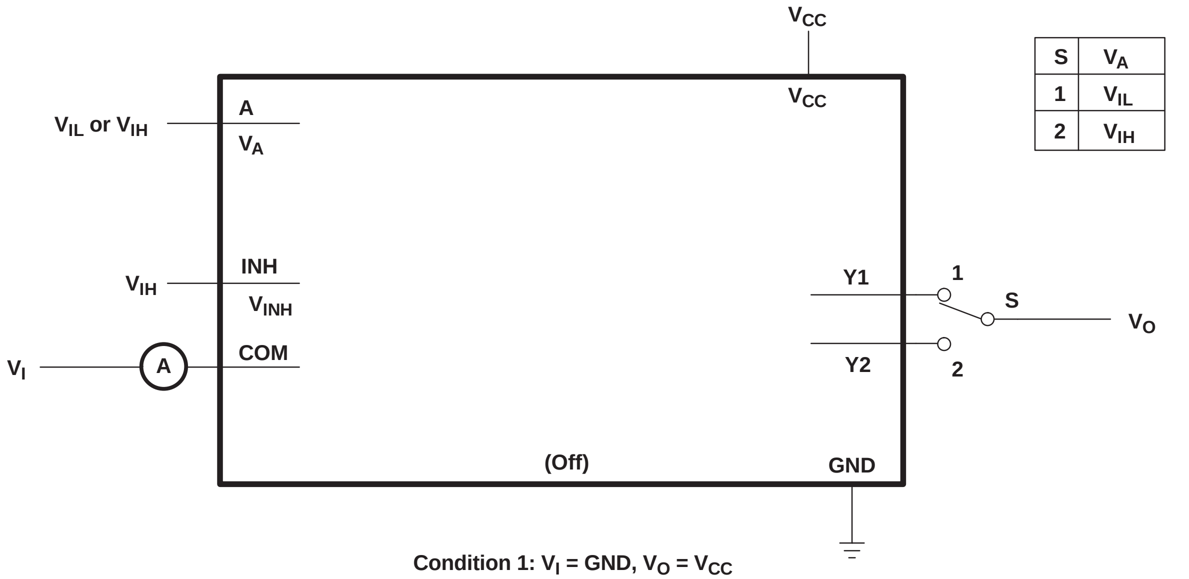


Figure 2. Typical r_{on} as a Function of Voltage (V_I) for V_I = 0 to V_{CC}

PARAMETER MEASUREMENT INFORMATION



Condition 1: V_I = GND, V_O = V_{CC}
Condition 2: V_I = V_{CC}, V_O = GND

Figure 3. Off-State Switch Leakage-Current Test Circuit

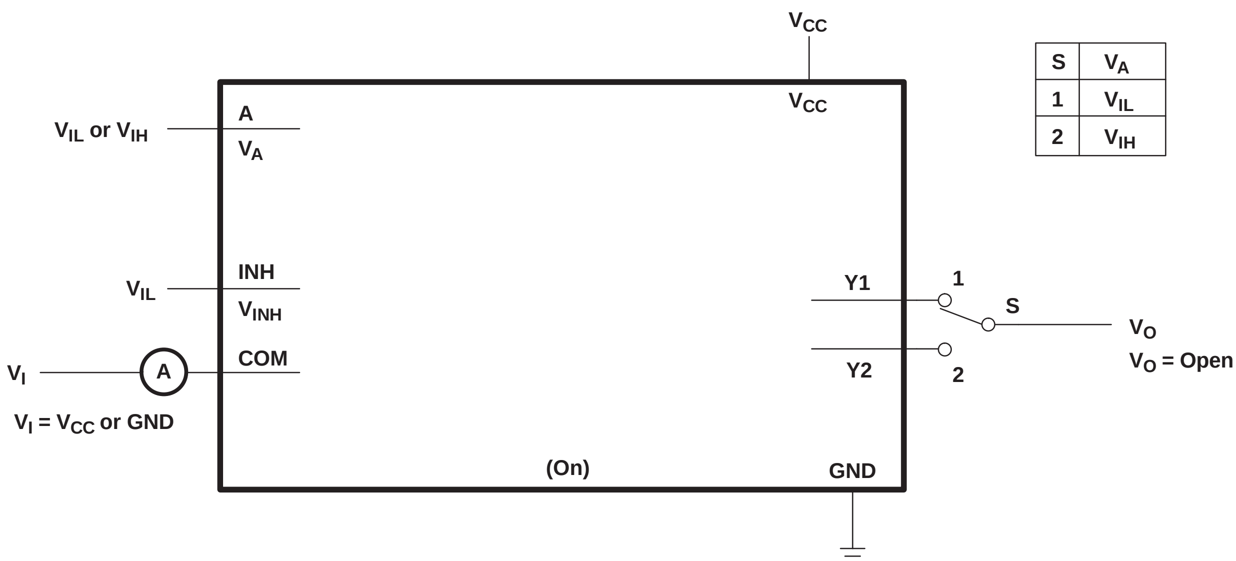
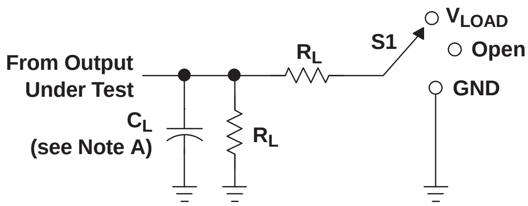


Figure 4. On-State Switch Leakage-Current Test Circuit

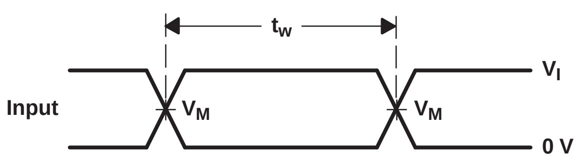
PARAMETER MEASUREMENT INFORMATION



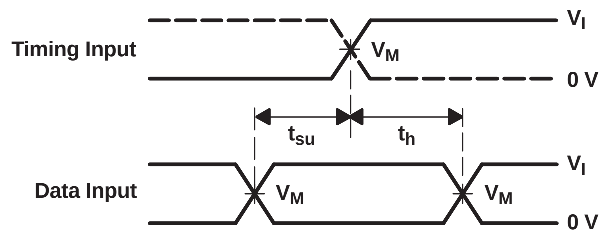
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

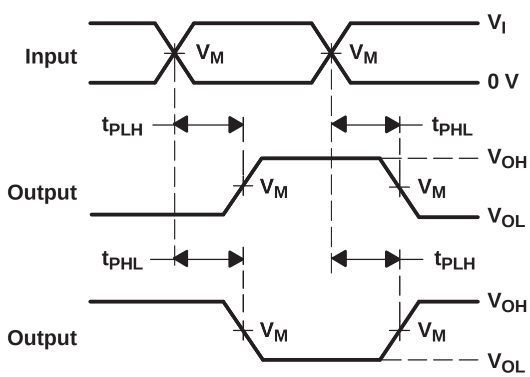
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
0.8 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	2 kΩ	0.1 V
1.2 V ± 0.1 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	2 kΩ	0.1 V
1.5 V ± 0.1 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	2 kΩ	0.1 V
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	2 kΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	2 kΩ	0.15 V
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V



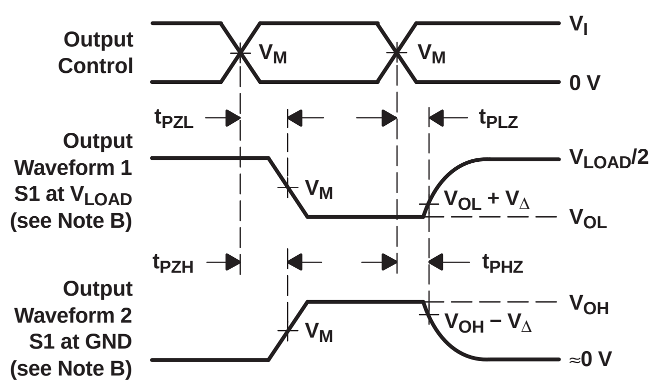
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, slew rate ≥ 1 V/ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 5. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

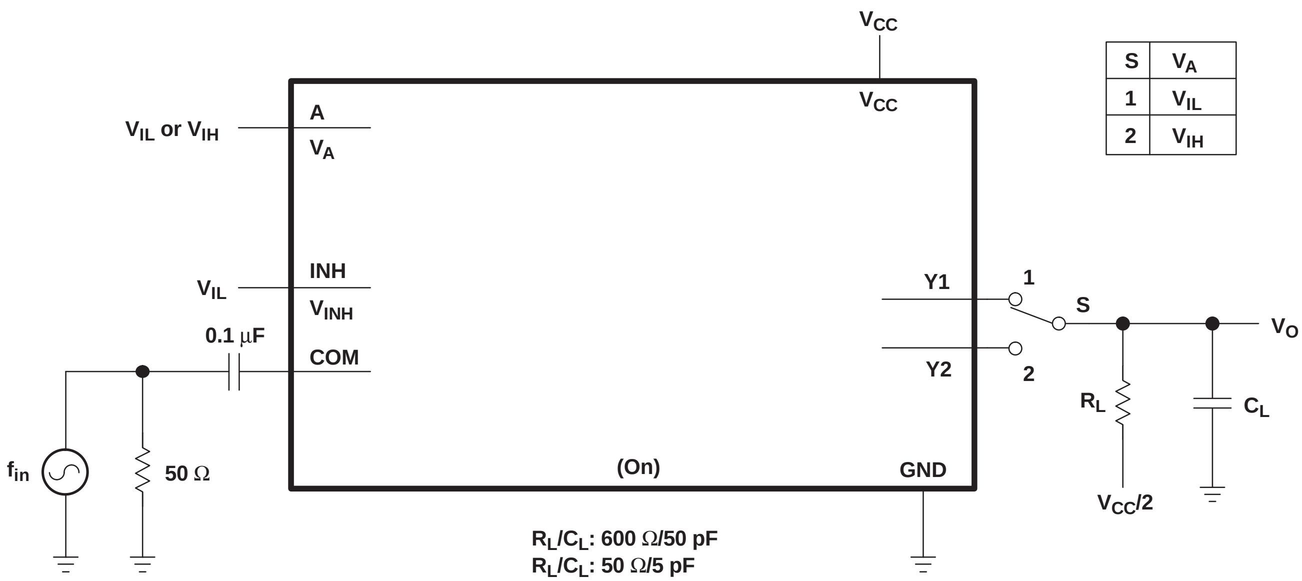


Figure 6. Frequency Response (Switch On)

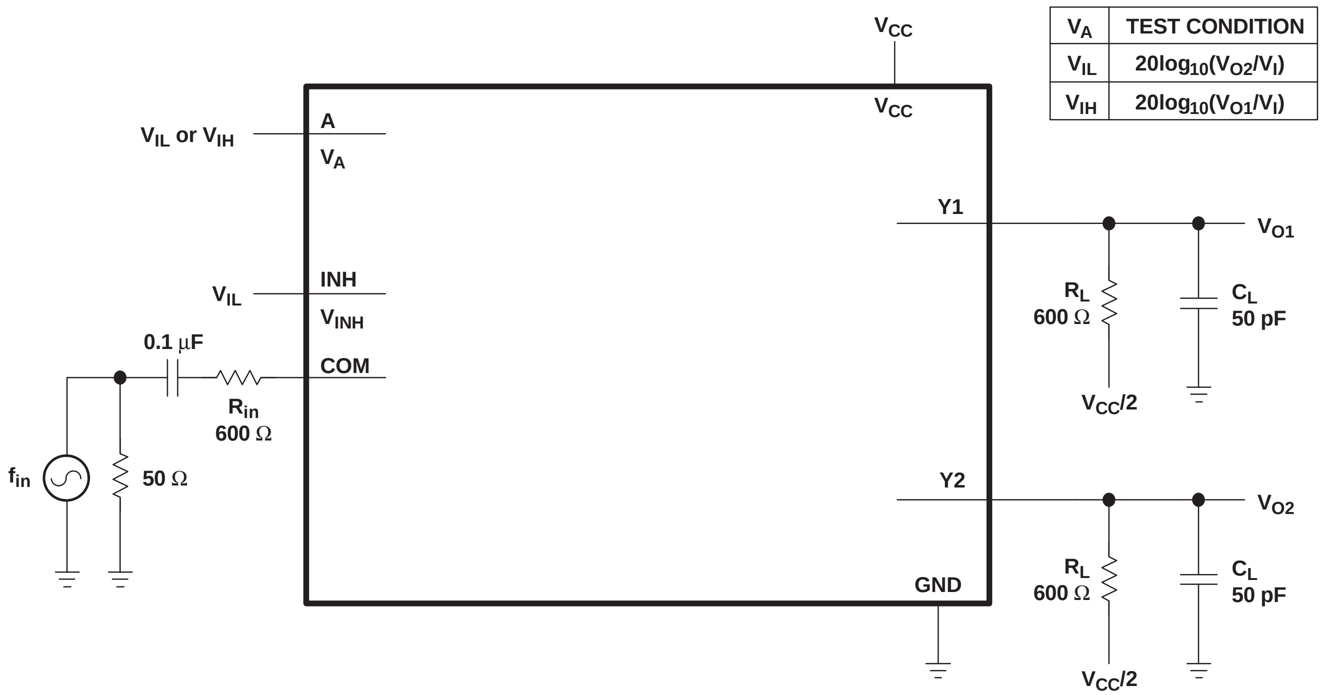


Figure 7. Crosstalk (Between Switches)

PARAMETER MEASUREMENT INFORMATION

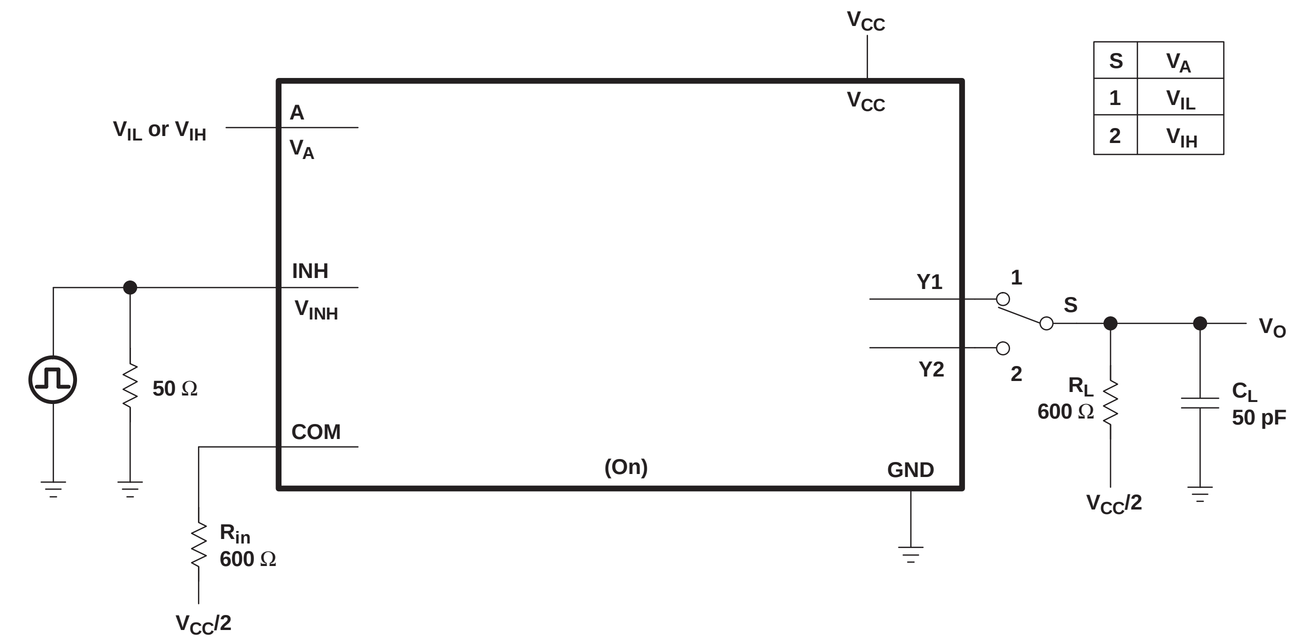


Figure 8. Crosstalk (Control Input, Switch Output)

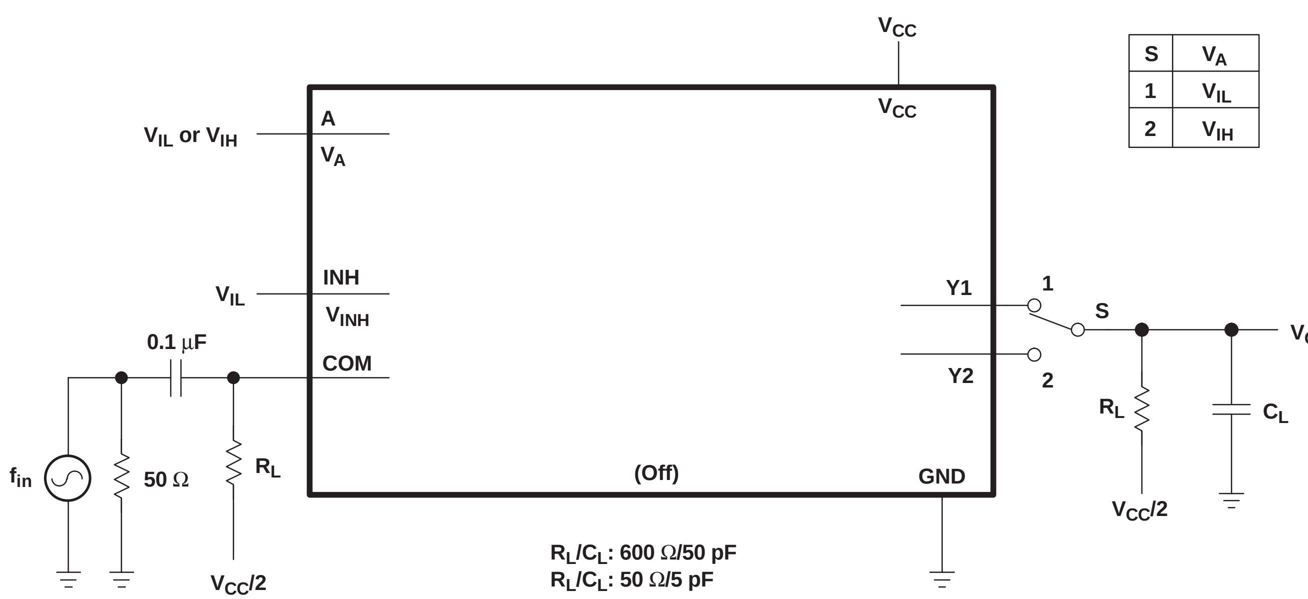
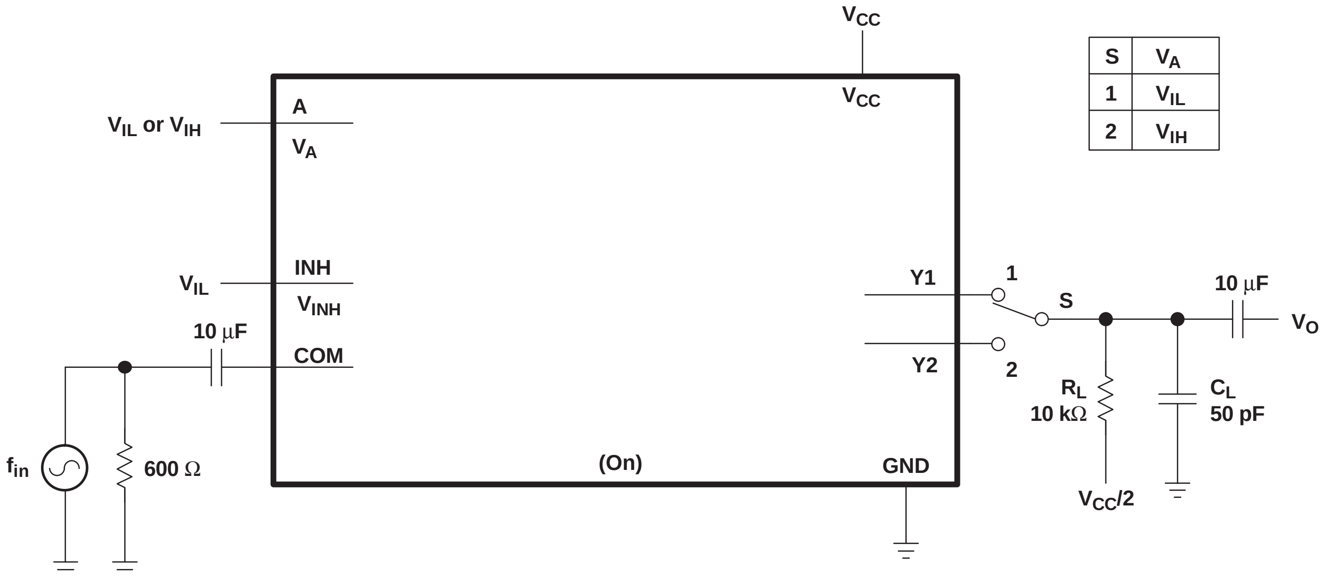


Figure 9. Feedthrough (Switch Off)

PARAMETER MEASUREMENT INFORMATION



V_{CC} = 0.8 V, V_I = 0.7 $V_{P\text{-}P}$
V_{CC} = 1.1 V, V_I = 1 $V_{P\text{-}P}$
V_{CC} = 1.4 V, V_I = 1.2 $V_{P\text{-}P}$
V_{CC} = 1.65 V, V_I = 1.4 $V_{P\text{-}P}$
V_{CC} = 2.3 V, V_I = 2 $V_{P\text{-}P}$

Figure 10. Sine-Wave Distortion

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AUC2G53DCTR	ACTIVE	SM8	DCT	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	U53 Z	Samples
SN74AUC2G53DCTRE4	ACTIVE	SM8	DCT	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	U53 Z	Samples
SN74AUC2G53DCUR	ACTIVE	VSSOP	DCU	8	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	(U53Q, U53R)	Samples
SN74AUC2G53DCURG4	ACTIVE	VSSOP	DCU	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	U53R	Samples
SN74AUC2G53YZPR	ACTIVE	DSBGA	YZP	8	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	U4N	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

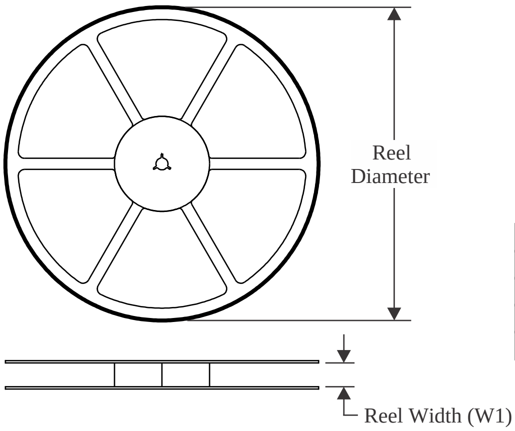
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

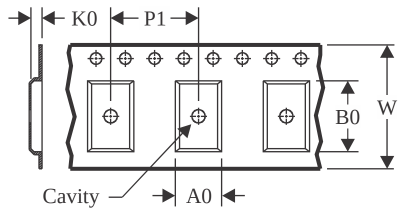
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

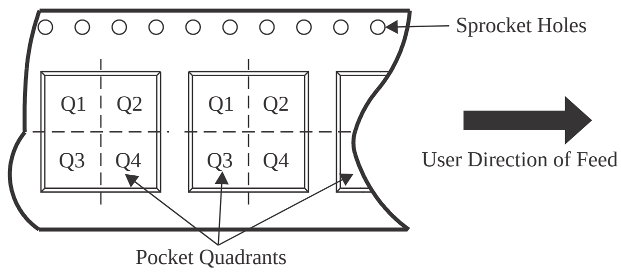


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

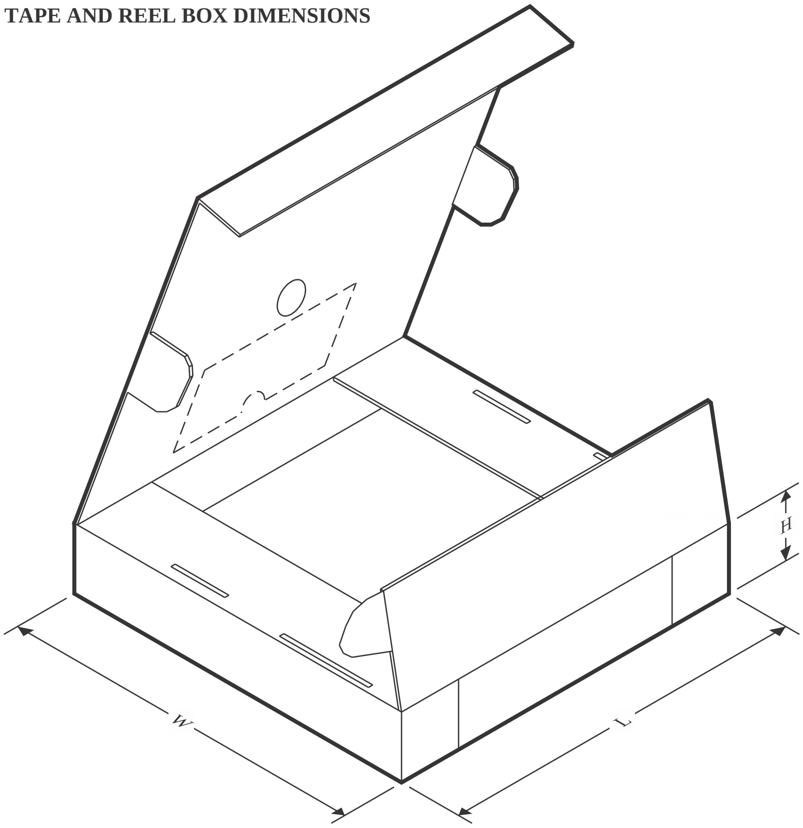
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

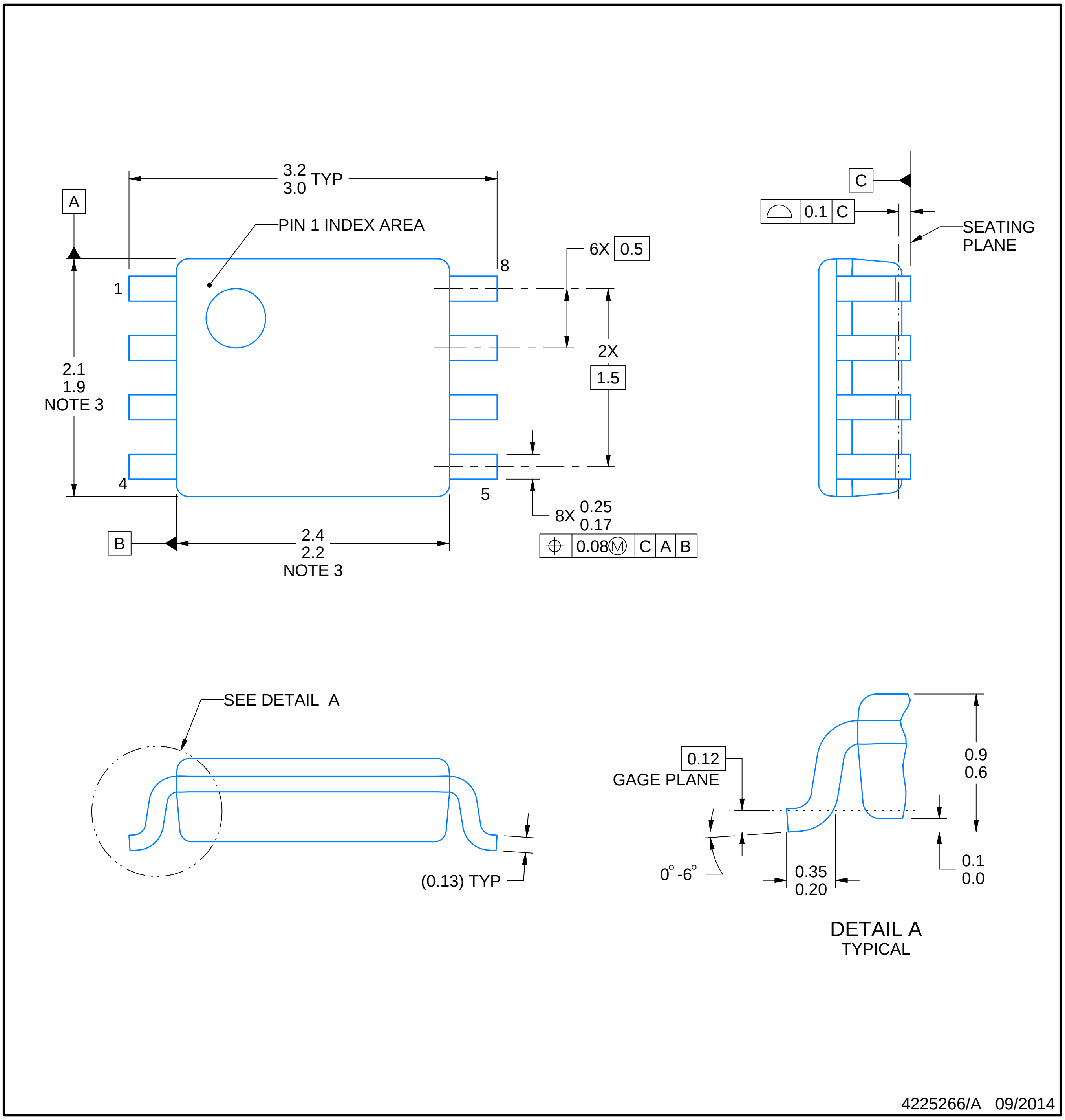
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUC2G53DCTR	SM8	DCT	8	3000	180.0	13.0	3.35	4.5	1.55	4.0	12.0	Q3
SN74AUC2G53DCUR	VSSOP	DCU	8	3000	178.0	9.5	2.25	3.35	1.05	4.0	8.0	Q3
SN74AUC2G53DCUR	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74AUC2G53DCURG4	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74AUC2G53YZPR	DSBGA	YZP	8	3000	178.0	9.2	1.02	2.02	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



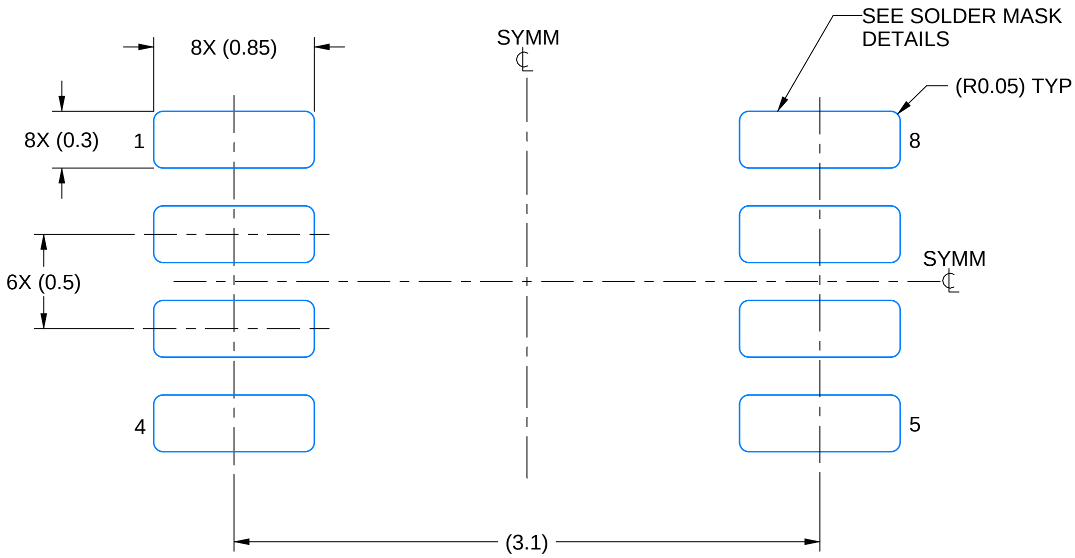
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUC2G53DCTR	SM8	DCT	8	3000	182.0	182.0	20.0
SN74AUC2G53DCUR	VSSOP	DCU	8	3000	202.0	201.0	28.0
SN74AUC2G53DCUR	VSSOP	DCU	8	3000	202.0	201.0	28.0
SN74AUC2G53DCURG4	VSSOP	DCU	8	3000	202.0	201.0	28.0
SN74AUC2G53YZPR	DSBGA	YZP	8	3000	220.0	220.0	35.0

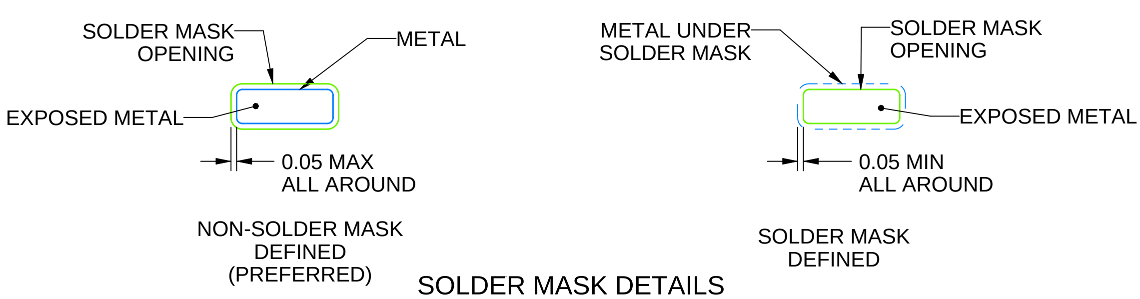


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-187 variation CA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X

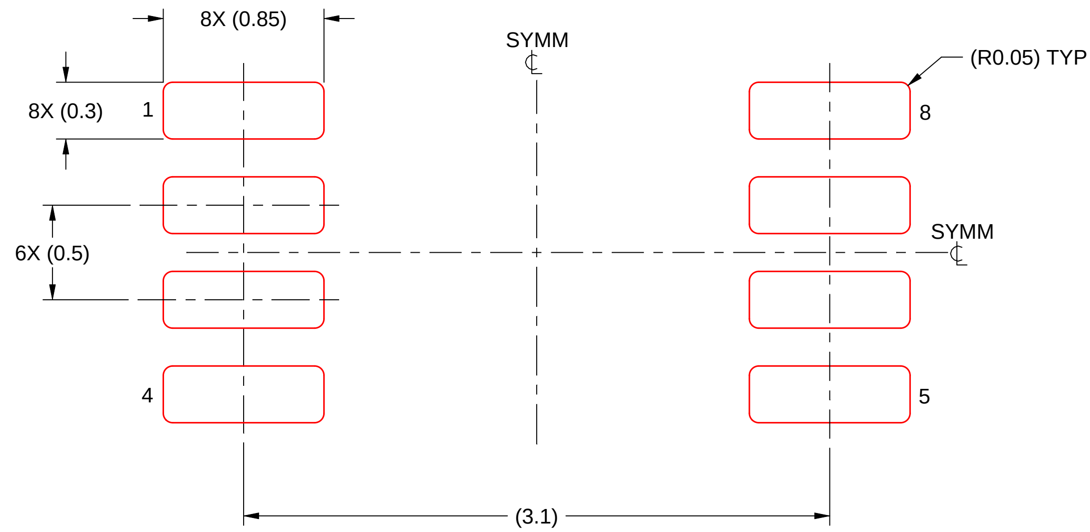


SOLDER MASK DETAILS

4225266/A 09/2014

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

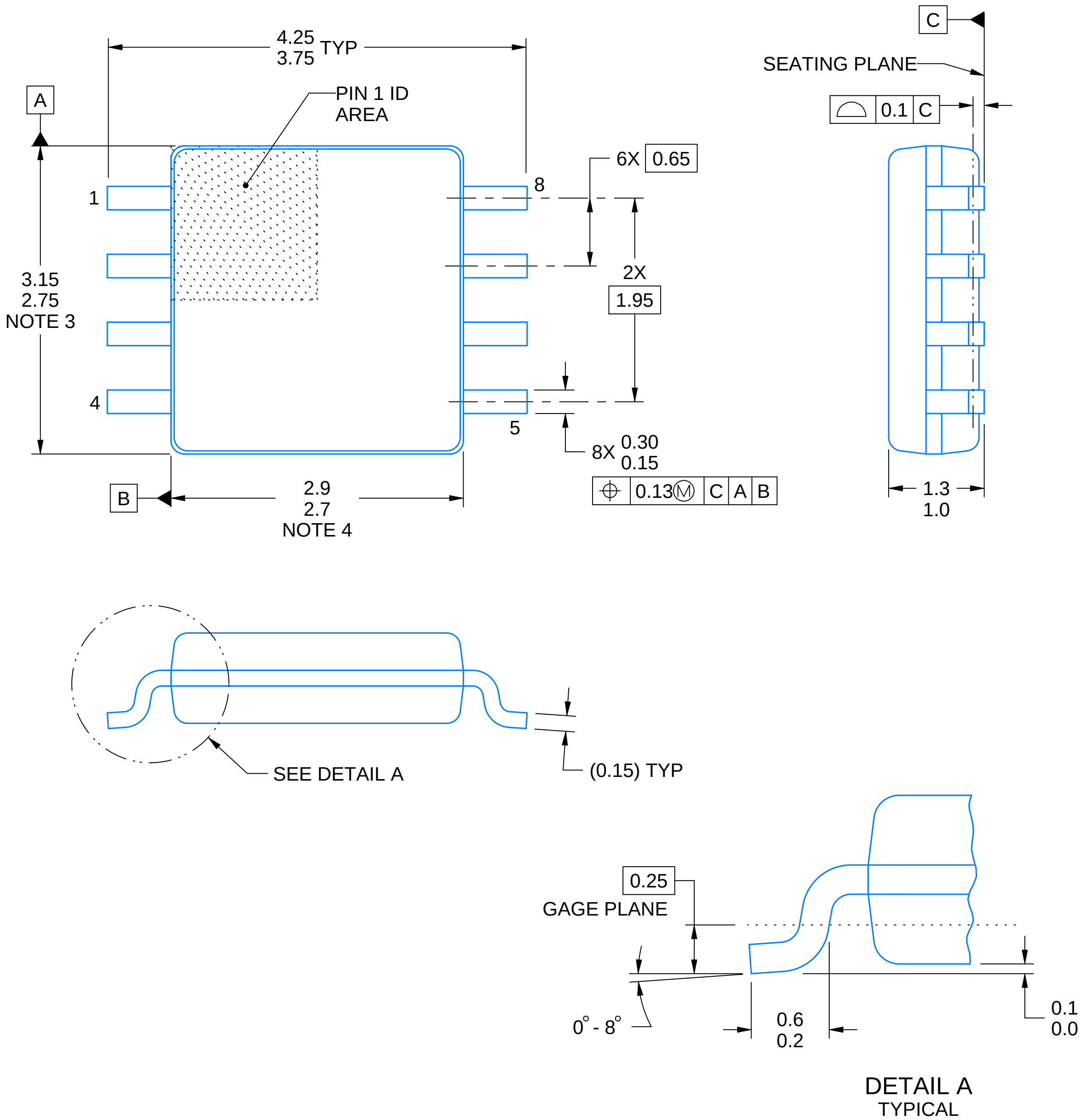


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 25X

4225266/A 09/2014

NOTES: (continued)

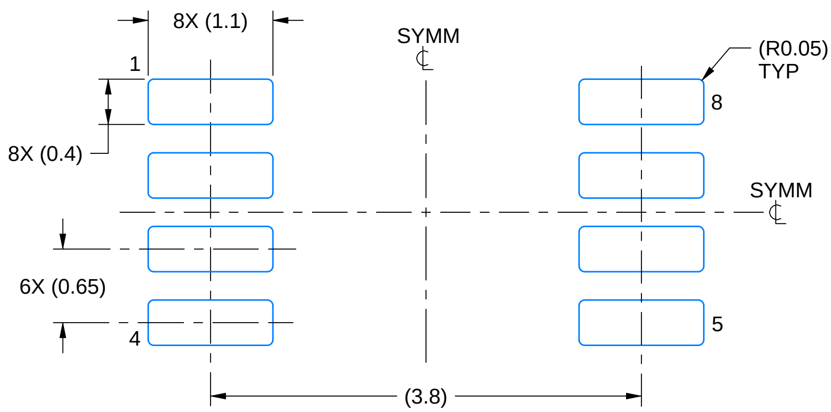
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.



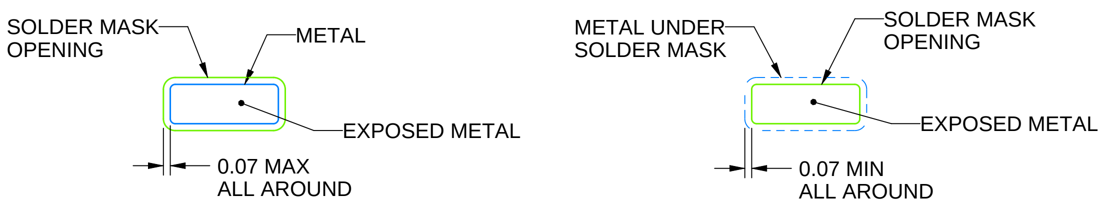
4220784/C 06/2021

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



NON SOLDER MASK
DEFINED

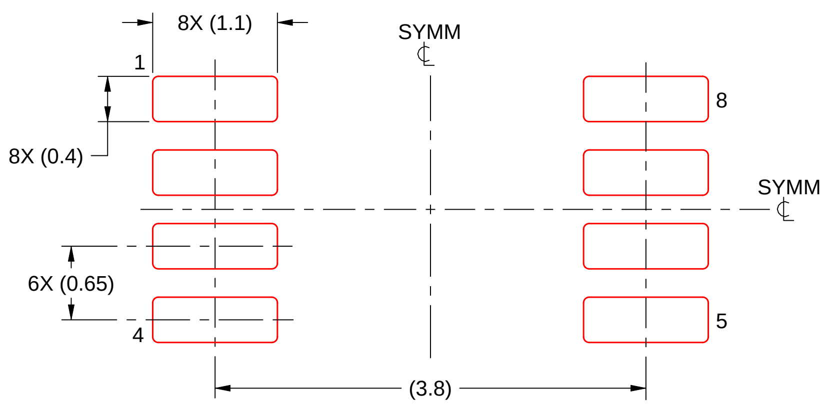
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220784/C 06/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

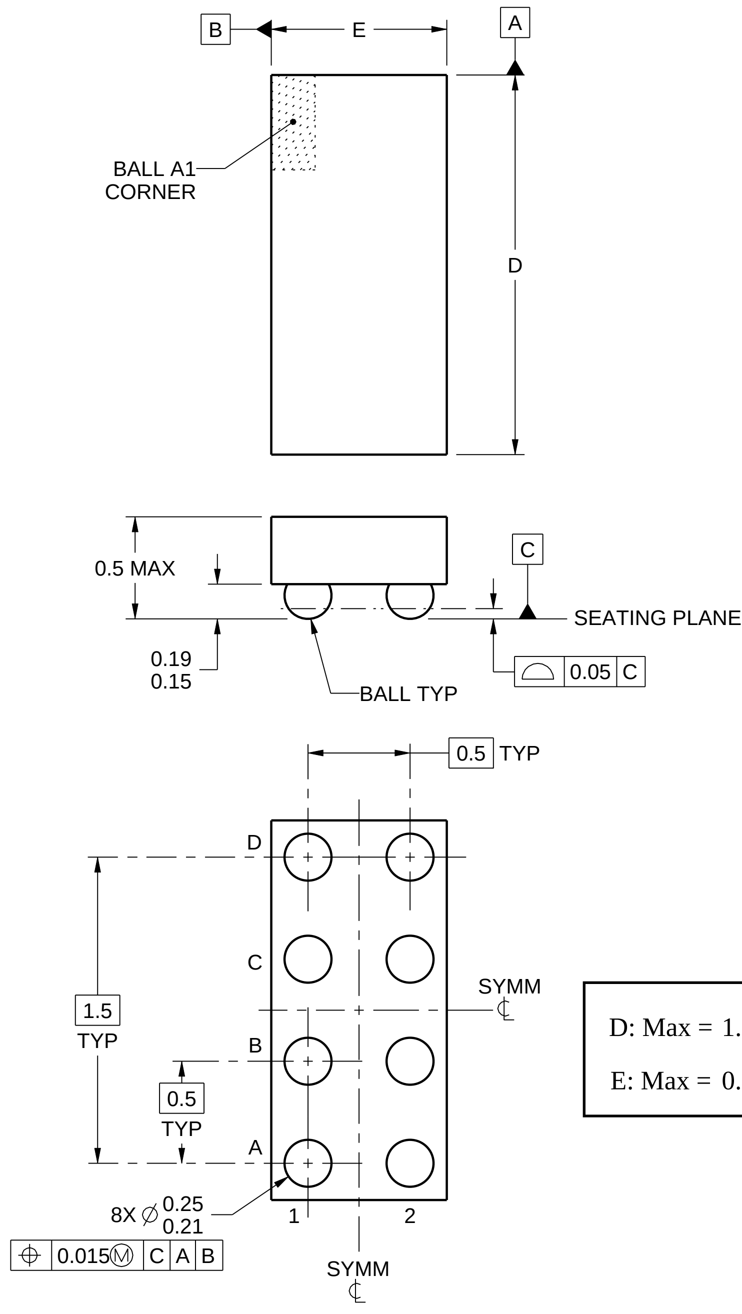


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4220784/C 06/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.



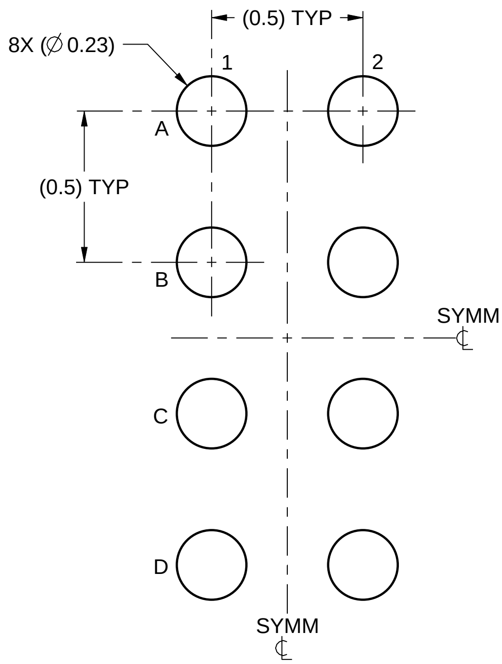
D: Max = 1.918 mm, Min =1.858 mm

E: Max = 0.918 mm, Min =0.858 mm

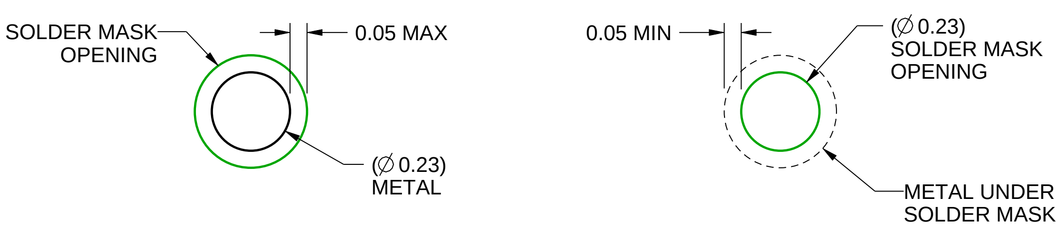
4223082/A 07/2016

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:40X



NON-SOLDER MASK DEFINED (PREFERRED)

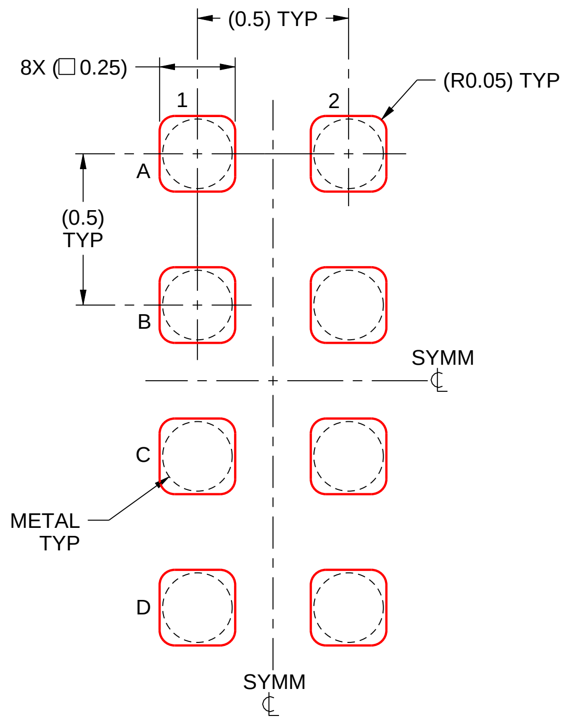
SOLDER MASK DEFINED

SOLDER MASK DETAILS
NOT TO SCALE

4223082/A 07/2016

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4223082/A 07/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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