

SNx4LV4053A Triple 2-Channel Analog Multiplexers or Demultiplexers

1 Features

- 1.65V to 5.5V V_{CC} operation
- Support mixed-mode voltage operation on all ports
- High on-off output-voltage ratio
- Low crosstalk between switches
- Individual switch controls
- Extremely low input current
- Latch-up performance exceeds 250mA per JESD 17
- ESD protection exceeds JESD 22
 - 2000V Human-Body Model (A114-A)
 - 1000V Charged-Device Model (C101)

2 Applications

- [Telecommunications](#)
- [Infotainment](#)
- Signal gating and isolation
- [Home appliances](#)
- Programmable logic circuits
- Modulation and demodulation

3 Description

These triple 2-channel CMOS analog multiplexers/demultiplexers are designed for 1.65V to 5.5V V_{CC} operation.

The SNx4LV4053A devices handle both analog and digital signals. Each channel permits signals with amplitudes up to 5.5V (peak) to be transmitted in either direction.

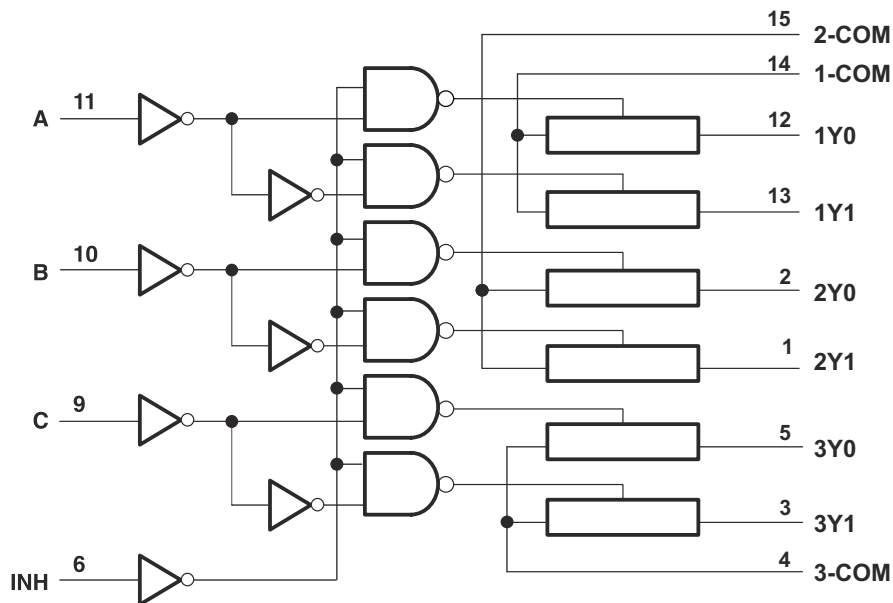
Applications include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾
SNx4LV4053A	D (SOIC, 16)	9.9mm × 6mm
	PW (TSSOP, 16)	5mm × 6.4mm
	RGY (VQFN, 16)	4mm × 3.5mm

(1) For more information, see [Section 11](#).

(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Functional Block Diagram



Table of Contents

1 Features	1	7.1 Functional Block Diagram.....	14
2 Applications	1	7.2 Device Functional Modes.....	14
3 Description	1	8 Application and Implementation	15
4 Pin Configuration and Functions	3	8.1 Application Information.....	15
5 Specifications	4	8.2 Typical Application.....	15
5.1 Absolute Maximum Ratings.....	4	8.3 Power Supply Recommendations.....	15
5.2 ESD Ratings.....	4	8.4 Layout.....	15
5.3 Thermal Information: SN74LV4053A.....	4	9 Device and Documentation Support	17
5.4 Recommended Operating Conditions.....	5	9.1 Receiving Notification of Documentation Updates....	17
5.5 Electrical Characteristics.....	5	9.2 Support Resources.....	17
5.6 Timing Characteristics $V_{CC} = 2.5V \pm 0.2V$	7	9.3 Trademarks.....	17
5.7 Timing Characteristics $V_{CC} = 3.3V \pm 0.3V$	7	9.4 Electrostatic Discharge Caution.....	17
5.8 Timing Characteristics $V_{CC} = 5V \pm 0.5V$	8	9.5 Glossary.....	17
5.9 AC Characteristics.....	8	10 Revision History	17
6 Parameter Measurement Information	10	11 Mechanical, Packaging, and Orderable Information	17
7 Detailed Description	14		

4 Pin Configuration and Functions

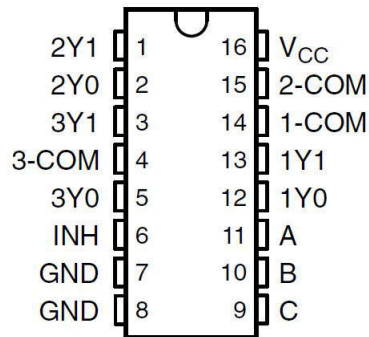


Figure 4-1. SN74LV4053A D or PW Packages, 16-Pin SOIC or TSSOP (Top View)

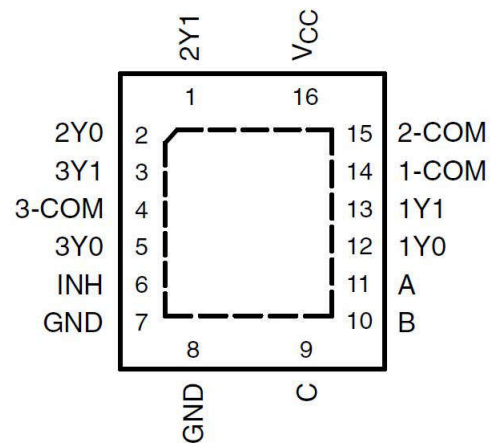


Figure 4-2. SN74LV4053A RGY, 16-Pin VQFN (Top View)

Table 4-1. Pin Functions

PIN		TYPE ⁽²⁾	DESCRIPTION
NAME	NO.		
2Y1	1	I ⁽¹⁾	Input to mux 2
2Y0	2	I ⁽¹⁾	Input to mux 2
3Y1	3	I ⁽¹⁾	Input to mux 3
3-COM	4	O ⁽¹⁾	Output of mux 3
3Y0	5	I ⁽¹⁾	Input to mux 3
INH	6	I	Enables the outputs of the device. Logic low level with turn the outputs on, high level will turn them off.
GND	7	-	Ground
GND	8	-	Ground
C	9	I	Selector line for outputs (see Section 7.2 for specific information)
B	10	I	Selector line for outputs (see Section 7.2 for specific information)
A	11	I	Selector line for outputs (see Section 7.2 for specific information)
1Y0	12	I ⁽¹⁾	Input to mux 1
1Y1	13	I ⁽¹⁾	Input to mux 1
1-COM	14	O ⁽¹⁾	Output of mux 1
2-COM	15	O ⁽¹⁾	Output of mux 2
V _{CC}	16	I	Device power input

- (1) These I/O descriptions represent the device when used as a multiplexer, when this device is operated as a demultiplexer pins 1Y0, 1Y1, 2Y0, 2Y1, 3Y0, 3Y1 may be considered outputs (O) and pins 1-COM, 2-COM, and 3-COM may be considered inputs (I).
- (2) I = input, O = output

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)^{(1) (3)}

		MIN	MAX	UNIT
V _{CC}	Supply voltage	-0.5	7.0	V
V _I	Logic input voltage range	-0.5	7.0	V
V _{IO}	Switch I/O voltage range ^{(2) (3)}	-0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < 0		mA
I _{IOK}	Switch IO diode clamp current	V _{IO} < 0 or V _{IO} > V _{CC}	50	mA
I _T	Switch continuous current	V _{IO} = 0 to V _{CC}	±25	mA
	Continuous current through V _{CC} or GND		±50	mA
T _J	Junction temperature		150	°C
T _{stg}	Storage temperature	-65	150	°C

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) Pins are diode-clamped to the power-supply rails. Over voltage signals must be voltage and current limited to maximum ratings.
- (3) This value is limited to 5.5V maximum

5.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/ JEDEC JS-001, all pins ⁽¹⁾	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	±1000	

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Thermal Information: SN74LV4053A

THERMAL METRIC ⁽¹⁾		SN74LV4053A			UNIT
		D (SOIC)	PW (TSSOP)	RGY (VQFN)	
		16 PINS	16 PINS	16 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	115.2	140.2	89.4	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	75.0	72.6	89.7	°C/W
R _{θJB}	Junction-to-board thermal resistance	76.6	98.7	65.4	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	31.3	13.4	25.0	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	75.7	97.3	65.2	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	N/A	48.9	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

5.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage	1 ⁽²⁾		5.5	V
V _{IH}	High-level input voltage, logic control inputs	V _{CC} = 1.65		5.5	V
		V _{CC} = 2V	1.5	5.5	
		V _{CC} = 2.3V to 2.7V	V _{CC} × 0.7	5.5	
		V _{CC} = 3V to 3.6V	V _{CC} × 0.7	5.5	
		V _{CC} = 4.5V to 5.5V	V _{CC} × 0.7	5.5	
V _{IL}	Low-level input voltage, logic control inputs	V _{CC} = 1.65	0	0.4	V
		V _{CC} = 2V	0	0.5	
		V _{CC} = 2.3V to 2.7V	0	V _{CC} × 0.3	
		V _{CC} = 3V to 3.6V	0	V _{CC} × 0.3	
		V _{CC} = 4.5V to 5.5V	0	V _{CC} × 0.3	
V _I	Logic control input voltage	0		5.5	V
V _{IO}	Switch input or output voltage	0		V _{CC}	V
Δt/ΔV	Logic input transition rise or fall rate	V _{CC} = 2.3V to 2.7V		200	ns/V
		V _{CC} = 3V to 3.6V		100	
		V _{CC} = 4.5V to 5.5V		20	
T _A	Ambient temperature	–40		125	°C

- (1) All unused inputs of the device must be held at V_{CC} or GND for proper device operation. Refer to TI application report *Implications of Slow or Floating CMOS Inputs*, SCBA004.
- (2) When using a V_{CC} of ≤1.2V, it is recommended to use these devices only for transmitting digital signals. When supply voltage is near 1.2V the analog switch ON resistance becomes very non-linear

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	Condition	T _A	V _{CC}	MIN	TYP	MAX	UNIT
r _{ON}	ON-state switch resistance	I _T = 2mA, V _I = V _{CC} or GND, V _{INH} = V _{IL}	25°C	1.65V	60	150	Ω
r _{ON}	ON-state switch resistance	I _T = 2mA, V _I = V _{CC} or GND, V _{INH} = V _{IL}	–40°C to 85°C	1.65V		225	Ω
r _{ON}	ON-state switch resistance	I _T = 2mA, V _I = V _{CC} or GND, V _{INH} = V _{IL}	–40°C to 125°C	1.65V		225	Ω
r _{ON}	ON-state switch resistance	I _T = 2mA, V _I = V _{CC} or GND, V _{INH} = V _{IL}	25°C	2.3V	38	180	Ω
			–40°C to 85°C		225		
			–40°C to 125°C		225		
			25°C	3V	30	150	Ω
			–40°C to 85°C		190		
			–40°C to 125°C		190		
			25°C	4.5V	22	75	Ω
			–40°C to 85°C		100		
			–40°C to 125°C		100		
r _{ON(p)}	Peak ON-state resistance	I _T = 2mA, V _I = GND to V _{CC} , V _{INH} = V _{IL}	25°C	1.65V	220	600	Ω

5.5 Electrical Characteristics (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		Condition	T _A	V _{CC}	MIN	TYP	MAX	UNIT
r _{ON(p)}	Peak ON-state resistance	I _T = 2mA, V _I = GND to V _{CC} , V _{INH} = V _{IL}	–40°C to 85°C	1.65V			700	Ω
r _{ON(p)}	Peak ON-state resistance	I _T = 2mA, V _I = GND to V _{CC} , V _{INH} = V _{IL}	–40°C to 125°C	1.65V			700	Ω
r _{ON(p)}	Peak ON-state resistance	I _T = 2mA, V _I = GND to V _{CC} , V _{INH} = V _{IL}	25°C	2.3V		113	500	Ω
			–40°C to 85°C			600		
			–40°C to 125°C			600		
			25°C	3V		54	180	Ω
			–40°C to 85°C			225		
			–40°C to 125°C			225		
			25°C	4.5V		31	100	Ω
			–40°C to 85°C			125		
			–40°C to 125°C			125		
Δr _{ON}	Difference in ON-state resistance between switches	I _T = 2mA, V _I = GND to V _{CC} , V _{INH} = V _{IL}	25°C	1.65V		3	40	Ω
Δr _{ON}	Difference in ON-state resistance between switches	I _T = 2mA, V _I = GND to V _{CC} , V _{INH} = V _{IL}	–40°C to 85°C	1.65V			50	Ω
Δr _{ON}	Difference in ON-state resistance between switches	I _T = 2mA, V _I = GND to V _{CC} , V _{INH} = V _{IL}	–40°C to 85°C	1.65V			50	Ω
Δr _{ON}	Difference in ON-state resistance between switches	I _T = 2mA, V _I = GND to V _{CC} , V _{INH} = V _{IL}	25°C	2.3V		2.1	30	Ω
			–40°C to 85°C			40		
			–40°C to 125°C			40		
			25°C	3V		1.4	20	Ω
			–40°C to 85°C			30		
			–40°C to 125°C			30		
			25°C	4.5V		1.3	15	Ω
			–40°C to 85°C			20		
			–40°C to 125°C			20		
I _{IH} I _{IL}	Control input current	V _I = 5.5V or GND	25°C	0 to 5.5V			0.1	μA
			–40°C to 85°C			1		
			–40°C to 125°C			2		
I _{S(off)}	OFF-state switch leakage current	V _I = V _{CC} and V _O = GND, or V _I = GND and V _O = V _{CC} , V _{INH} = V _{IH}	25°C	5.5V			0.1	μA
			–40°C to 85°C			1		
			–40°C to 125°C			2		
I _{S(on)}	ON-state switch leakage current	V _I = V _{CC} or GND, V _{INH} = V _{IL} (see Figure 6-3)	25°C	5.5V			0.1	μA
			–40°C to 85°C			1		
			–40°C to 125°C			2		
I _{CC}	Supply current	V _I = V _{CC} or GND V _{INH} = 0V	25°C	5.5V		0.01	μA	
			–40°C to 85°C			20		
			–40°C to 125°C			40		
C _{IC}	Control input capacitance	f = 10MHz	25°C	3.3V		2	pF	

5.5 Electrical Characteristics (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		Condition	T _A	V _{CC}	MIN	TYP	MAX	UNIT
C _{OS}	Switch terminal capacitance	f = 10MHz	25°C	3.3V		5		pF
C _{IS}	Common terminal capacitance	f = 10MHz	25°C	3.3V		23		pF
C _{OS(on)}	Common terminal ON-capacitance	f = 10MHz	25°C	3.3V		23		pF
C _F	Feedthrough capacitance	f = 10MHz	25°C	3.3V		0.5		pF
C _{PD}	Power dissipation capacitance	C _L = 50pF, f = 10MHz	25°C	3.3V		6		pF

5.6 Timing Characteristics V_{CC} = 2.5V ± 0.2V

PARAMETER		FROM (INPUT)	TO (OUTPUT)	CONDITIONS	T _A	MIN	TYP	MAX	UNIT
t _{PLH} t _{PHL}	Propagation delay time	COM or Yn	Yn or COM	C _L = 15pF	25°C		1.9	10	ns
					-40°C to 85°C			16	
					-40°C to 125°C			18	
t _{PZH} t _{PZL}	Enable delay time	INH	COM or Yn	C _L = 15pF	25°C		6.6	18	ns
					-40°C to 85°C			23	
					-40°C to 125°C			25	
t _{PHZ} t _{PLZ}	Disable delay time	INH	COM or Yn	C _L = 15pF	25°C		7.4	18	ns
					-40°C to 85°C			23	
					-40°C to 125°C			25	
t _{PLH} t _{PHL}	Propagation delay time	COM or Yn	Yn or COM	C _L = 50pF	25°C		3.8	12	ns
					-40°C to 85°C			18	
					-40°C to 125°C			20	
t _{PZH} t _{PZL}	Enable delay time	INH	COM or Yn	C _L = 50pF	25°C		7.8	28	ns
					-40°C to 85°C			35	
					-40°C to 125°C			35	
t _{PHZ} t _{PLZ}	Disable delay time	INH	COM or Yn	C _L = 50pF	25°C		11.5	28	ns
					-40°C to 85°C			35	
					-40°C to 125°C			35	

5.7 Timing Characteristics V_{CC} = 3.3V ± 0.3V

PARAMETER		FROM (INPUT)	TO (OUTPUT)	CONDITIONS	T _A	MIN	TYP	MAX	UNIT
t _{PLH} t _{PHL}	Propagation delay time	COM or Yn	Yn or COM	C _L = 15pF	25°C		1.2	6	ns
					-40°C to 85°C			10	
					-40°C to 125°C			12	
t _{PZH} t _{PZL}	Enable delay time	INH	COM or Yn	C _L = 15pF	25°C		4.7	12	ns
					-40°C to 85°C			15	
					-40°C to 125°C			18	
t _{PHZ} t _{PLZ}	Disable delay time	INH	COM or Yn	C _L = 15pF	25°C		5.7	12	ns
					-40°C to 85°C			15	
					-40°C to 125°C			18	

5.7 Timing Characteristics $V_{CC} = 3.3V \pm 0.3V$ (continued)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{PLH} t_{PHL}	Propagation delay time	COM or Yn	Yn or COM	$C_L = 50pF$	25°C		2.5	9	ns
					-40°C to 85°C			12	
					-40°C to 125°C			14	
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Yn	$C_L = 50pF$	25°C		5.5	20	ns
					-40°C to 85°C			25	
					-40°C to 125°C			25	
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Yn	$C_L = 50pF$	25°C		8.8	20	ns
					-40°C to 85°C			25	
					-40°C to 125°C			25	

5.8 Timing Characteristics $V_{CC} = 5V \pm 0.5V$

PARAMETER		FROM (INPUT)	TO (OUTPUT)	CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{PLH} t_{PHL}	Propagation delay time	COM or Yn	Yn or COM	$C_L = 15pF$	25°C		0.6	4	ns
					-40°C to 85°C			7	
					-40°C to 125°C			10	
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Yn	$C_L = 15pF$	25°C		3.5	8	ns
					-40°C to 85°C			10	
					-40°C to 125°C			12	
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Yn	$C_L = 15pF$	25°C		4.4	10	ns
					-40°C to 85°C			11	
					-40°C to 125°C			12	
t_{PLH} t_{PHL}	Propagation delay time	COM or Yn	Yn or COM	$C_L = 50pF$	25°C		1.5	6	ns
					-40°C to 85°C			8	
					-40°C to 125°C			10	
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Yn	$C_L = 50pF$	25°C		4	14	ns
					-40°C to 85°C			18	
					-40°C to 125°C			18	
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Yn	$C_L = 50pF$	25°C		6.2	14	ns
					-40°C to 85°C			18	
					-40°C to 125°C			18	

5.9 AC Characteristics

PARAMETER	FROM (INPUT)	TO (OUTPUT)	Device	CONDITIONS	MIN	TYP	MAX	UNIT
Frequency response (switch on)	COM or Yn	Yn or COM	SN74LV4053	$C_L = 50pF$, $R_L = 600\Omega$, $F_{in} = 1MHz$ (sine wave), (see Figure 6-6) (1)	$V_{CC} = 2.3V$		40	MHz
					$V_{CC} = 3V$		45	
					$V_{CC} = 4.5V$		60	
Charge Injection (control input to signal output)	INH	COM or Yn		$C_L = 50pF$, $R_L = 600\Omega$, $F_{in} = 1MHz$ (sine wave) (see Figure 6-8)	$V_{CC} = 2.3V$		20	mV
					$V_{CC} = 3V$		35	
					$V_{CC} = 4.5V$		60	

5.9 AC Characteristics (continued)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	Device	CONDITIONS	MIN	TYP	MAX	UNIT
Feedthrough attenuation (switch off)	COM or Yn	Yn or COM		C _L = 50pF, R _L = 600Ω, F _{in} = 1MHz (sine wave) (see Figure 6-9) (2)	V _{CC} = 2.3V		-45	dB
					V _{CC} = 3V		-45	
					V _{CC} = 4.5V		-45	
Crosstalk (between any switches)	COM or Yn	Yn or COM		C _L = 50pF, R _L = 600Ω, F _{in} = 1MHz (sine wave) (see Figure 6-7) (2)	V _{CC} = 2.3V		-45	dB
					V _{CC} = 3V		-45	
					V _{CC} = 4.5V		-45	
Sine-wave distortion	COM or Yn	Yn or COM		C _L = 50pF, R _L = 10kΩ, F _{in} = 1kHz (sine wave) (see Figure 6-9)	V _I = 2V _{p-p} , V _{CC} = 2.3V		0.1	%
					V _I = 2.5V _{p-p} , V _{CC} = 3V		0.1	
					V _I = 4V _{p-p} , V _{CC} = 4.5V		0.1	

6 Parameter Measurement Information

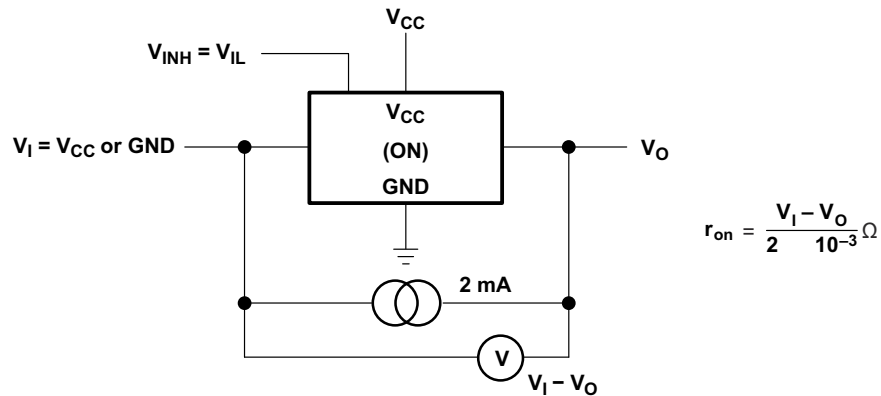
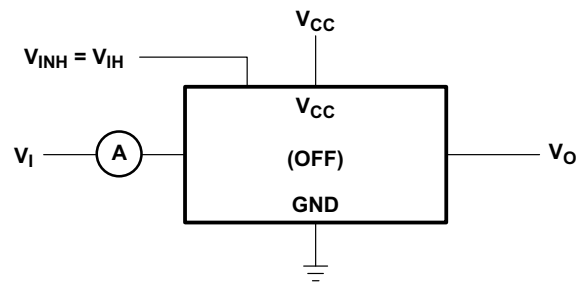


Figure 6-1. On-State Resistance Test Circuit



Condition 1: $V_I = 0, V_O = V_{CC}$
 Condition 2: $V_I = V_{CC}, V_O = 0$

Figure 6-2. Off-State Switch Leakage-Current Test Circuit

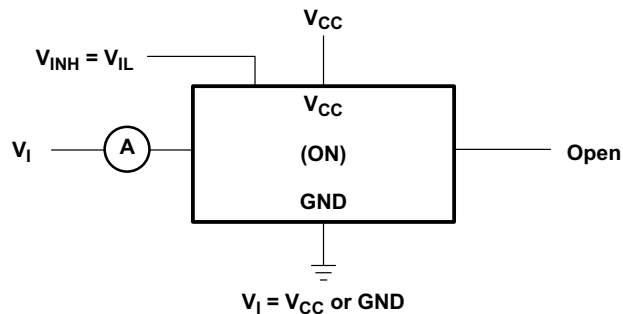


Figure 6-3. On-State Switch Leakage-Current Test Circuit

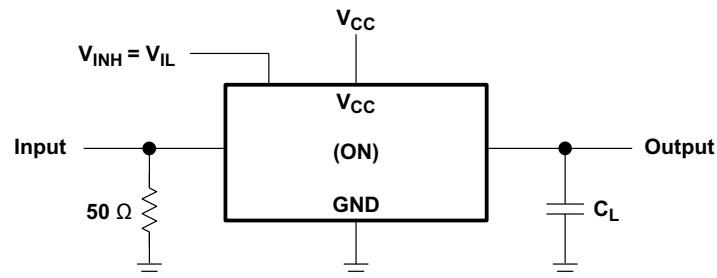
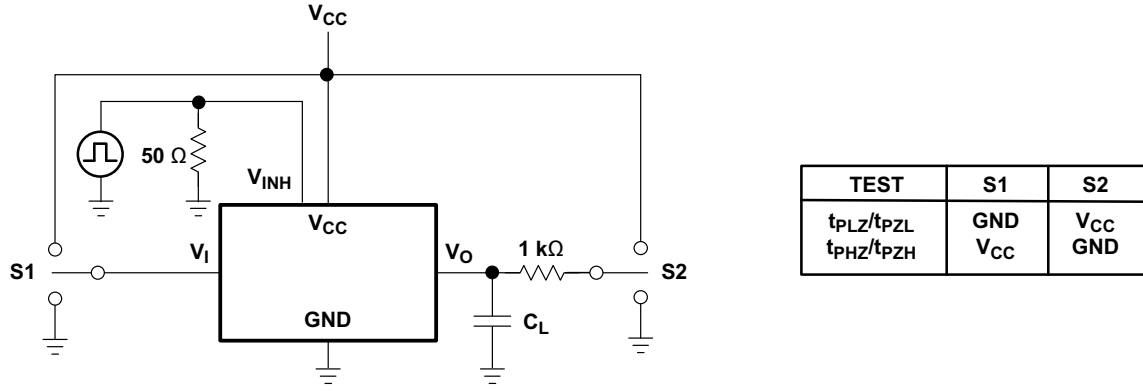
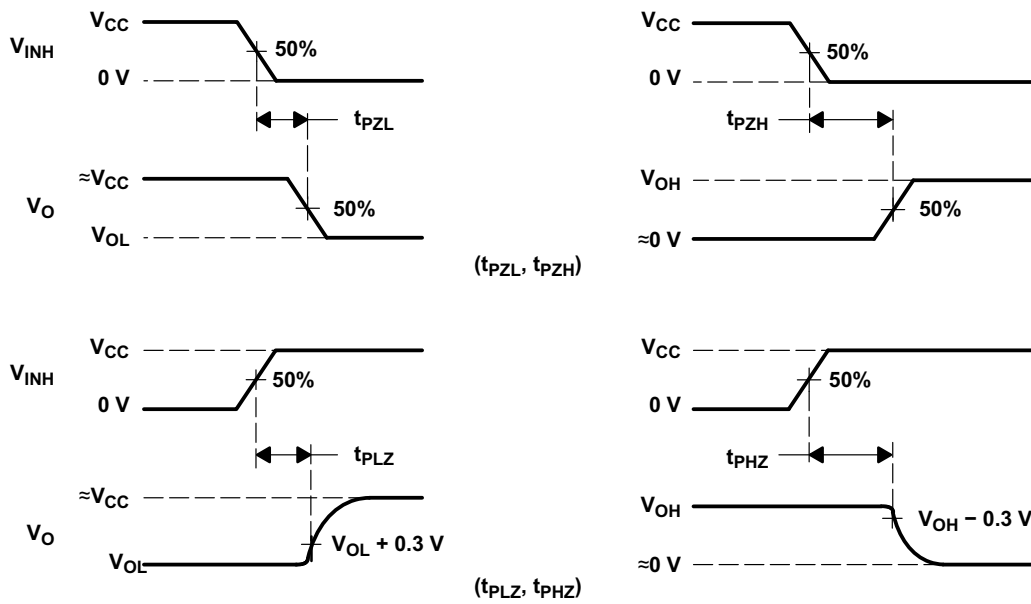


Figure 6-4. Propagation Delay Time, Signal Input to Signal Output

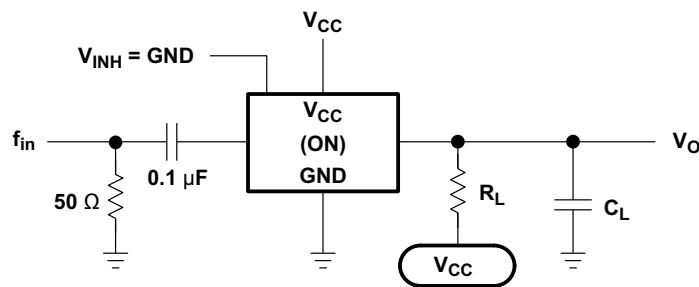


TEST CIRCUIT



VOLTAGE WAVEFORMS

Figure 6-5. Switching Time (t_{PZL} , t_{PLZ} , t_{PHZ} , t_{PHZ}), Control to Signal Output



NOTE A: f_{in} is a sine wave.

Figure 6-6. Frequency Response (Switch On)

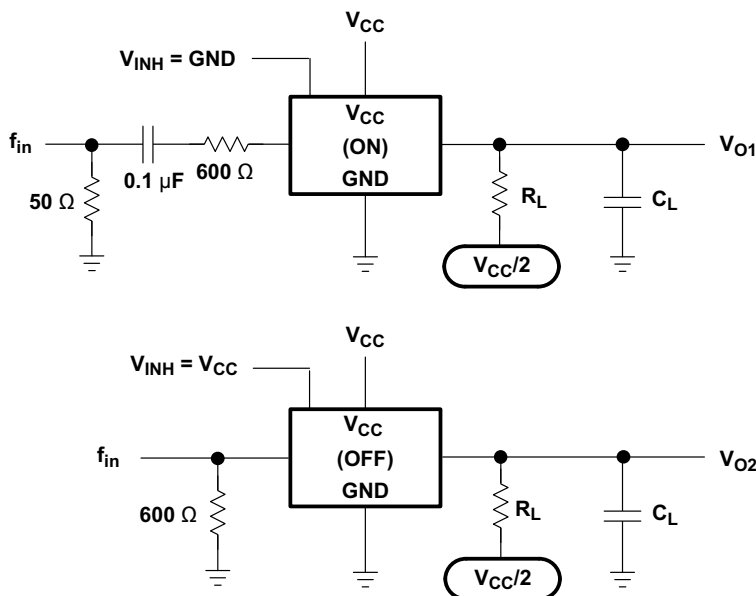


Figure 6-7. Crosstalk Between Any Two Switches

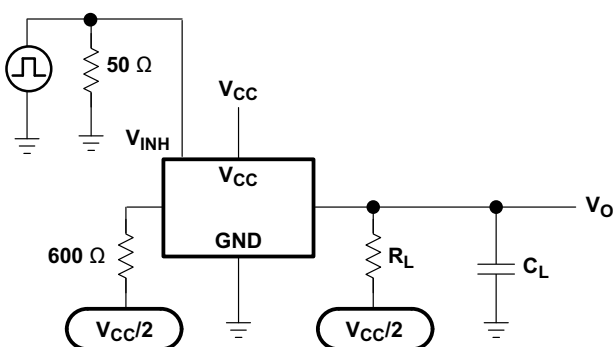


Figure 6-8. Crosstalk Between Control Input and Switch Output

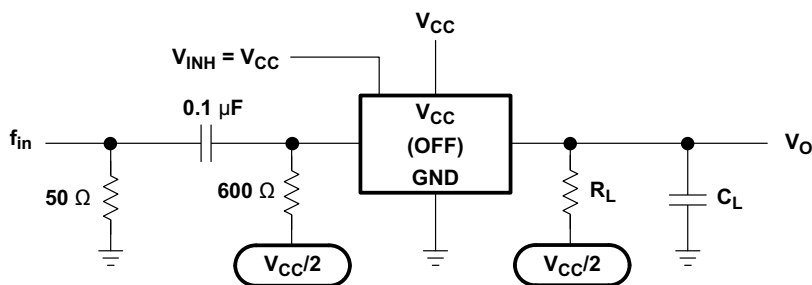


Figure 6-9. Feedthrough Attenuation (Switch Off)

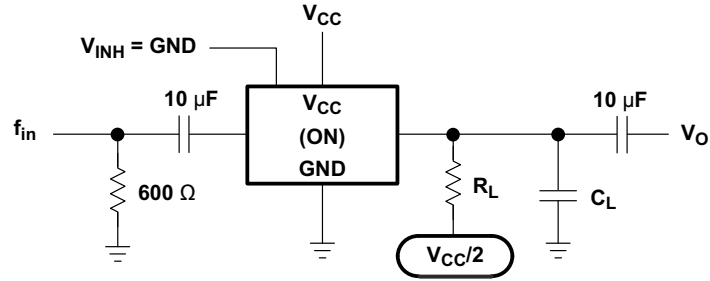
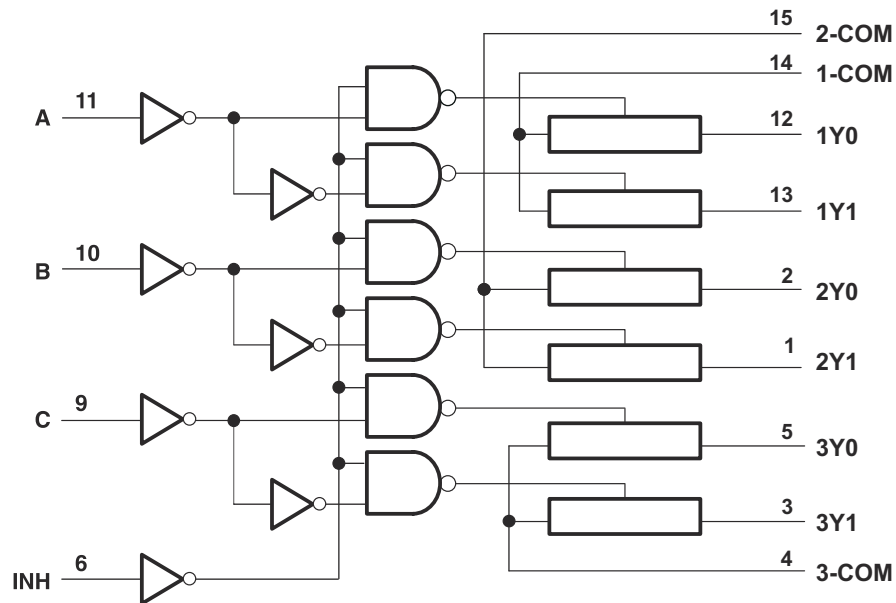


Figure 6-10. Sine-Wave Distortion

7 Detailed Description

7.1 Functional Block Diagram



7.2 Device Functional Modes

Function Table

INPUTS				ON CHANNEL
INH	C	B	A	
L	L	L	L	1Y0, 2Y0, 3Y0
L	L	L	H	1Y1, 2Y0, 3Y0
L	L	H	L	1Y0, 2Y1, 3Y0
L	L	H	H	1Y1, 2Y1, 3Y0
L	H	L	L	1Y0, 2Y0, 3Y1
L	H	L	H	1Y1, 2Y0, 3Y1
L	H	H	L	1Y0, 2Y1, 3Y1
L	H	H	H	1Y1, 2Y1, 3Y1
H	X	X	X	None

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

A multiplexer is used in applications where multiple signals share a resource. In the following example, several different sensors are connected to the analog-to-digital converter (ADC) of a microcontroller (MCU).

8.2 Typical Application

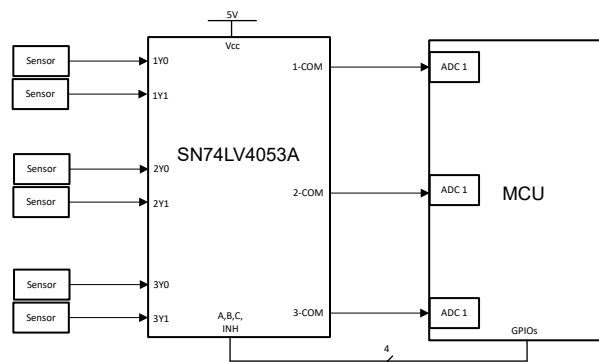


Figure 8-1. Typical Application Schematic

8.2.1 Design Requirements

Processing 8 different analog signals would normally require 8 separate ADCs, but the previous figure shows how to achieve this using only 2 ADCs and 3 GPIOs (general purpose input/outputs).

8.2.2 Detailed Design Procedure

To design with the SNx4LV4053A, a stable input voltage between 2V (see *Recommended Operating Conditions* for details) and 5.5V must be available. The characteristics of the signal that is being multiplexed so that no important information is lost due to timing or voltage level incompatibility with this device is another important design consideration.

8.3 Power Supply Recommendations

Most systems have a common 3.3V or 5V rail that may be used to supply the V_{CC} pin of this device. If this is not available, then a Switch-Mode-Power-Supply (SMPS) or a Linear Dropout Regulator (LDO) may be used to supply this device from a higher voltage rail.

8.4 Layout

8.4.1 Layout Guidelines

In general, it is best to keep signal lines as short and as straight as possible. Incorporation of microstrip or stripline techniques is also recommended when signal lines are greater than 1 inch in length. These traces must be designed with a characteristic impedance of either 50Ω or 75Ω, as required by the application. Be careful when placing this device too close to high voltage switching components, as they may cause interference.

8.4.2 Layout Example

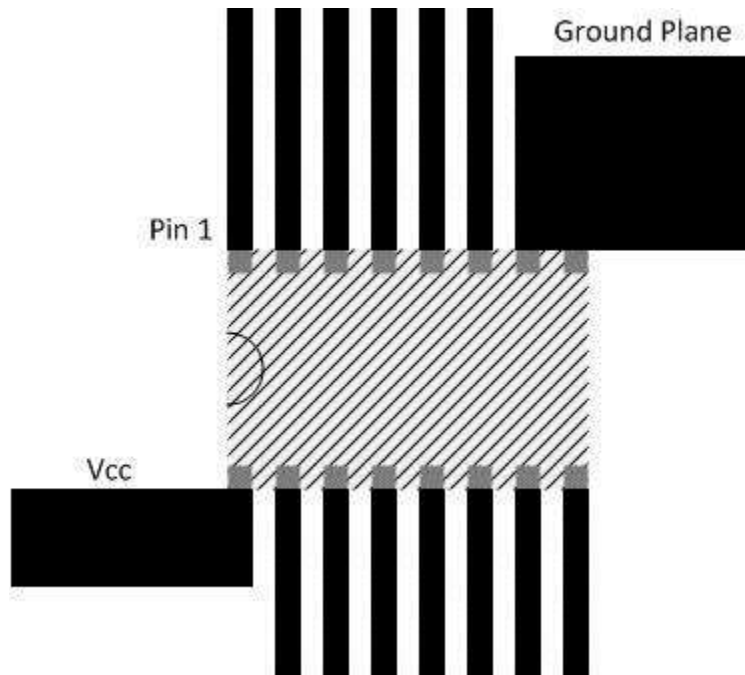


Figure 8-2. Layout Example Schematic

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

TI E2E™ [support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision K (April 2005) to Revision L (June 2024)	Page
• Changed the numbering format for tables, figures, and cross-references throughout the document	1
• Added new VIH and VIL Specifications at 1.65V Vcc.....	5
• Increased max ambient temperature max to 125C.....	5
• Added Ron, Ron Peak, and Delta Ron Specifications at 1.65V Vcc.....	5
• Added Ron, Ron Peak, and Delta Ron Specifications at 125C.....	5
• Added Timing Specifications at 125C.....	7

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LV4053ADBR	NRND	SSOP	DB	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW053A	
SN74LV4053ADGVR	NRND	TVSOP	DGV	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW053A	
SN74LV4053ADR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	LV4053A	Samples
SN74LV4053AN	NRND	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74LV4053AN	
SN74LV4053ANSR	NRND	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	74LV4053A	
SN74LV4053APWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	LW053A	Samples
SN74LV4053ARGYR	ACTIVE	VQFN	RGY	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LW053A	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LV4053A :

- Automotive : [SN74LV4053A-Q1](#)
- Enhanced Product : [SN74LV4053A-EP](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

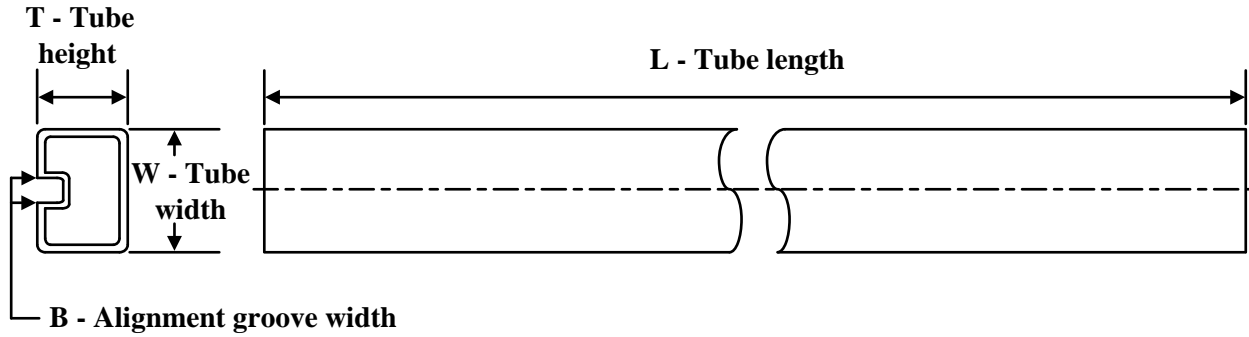

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV4053ADBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74LV4053ADGVR	TVSOP	DGV	16	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74LV4053ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74LV4053ANSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74LV4053APWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV4053APWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV4053APWT	TSSOP	PW	16	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV4053ARGYR	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV4053ADBR	SSOP	DB	16	2000	356.0	356.0	35.0
SN74LV4053ADGVR	TVSOP	DGV	16	2000	356.0	356.0	35.0
SN74LV4053ADR	SOIC	D	16	2500	340.5	336.1	32.0
SN74LV4053ANSR	SO	NS	16	2000	356.0	356.0	35.0
SN74LV4053APWR	TSSOP	PW	16	2000	356.0	356.0	35.0
SN74LV4053APWRG4	TSSOP	PW	16	2000	367.0	367.0	35.0
SN74LV4053APWT	TSSOP	PW	16	250	356.0	356.0	35.0
SN74LV4053ARGYR	VQFN	RGY	16	3000	367.0	367.0	35.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74LV4053AD	D	SOIC	16	40	507	8	3940	4.32
SN74LV4053ADE4	D	SOIC	16	40	507	8	3940	4.32
SN74LV4053AN	N	PDIP	16	25	506	13.97	11230	4.32
SN74LV4053AN	N	PDIP	16	25	506	13.97	11230	4.32
SN74LV4053APW	PW	TSSOP	16	90	530	10.2	3600	3.5

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

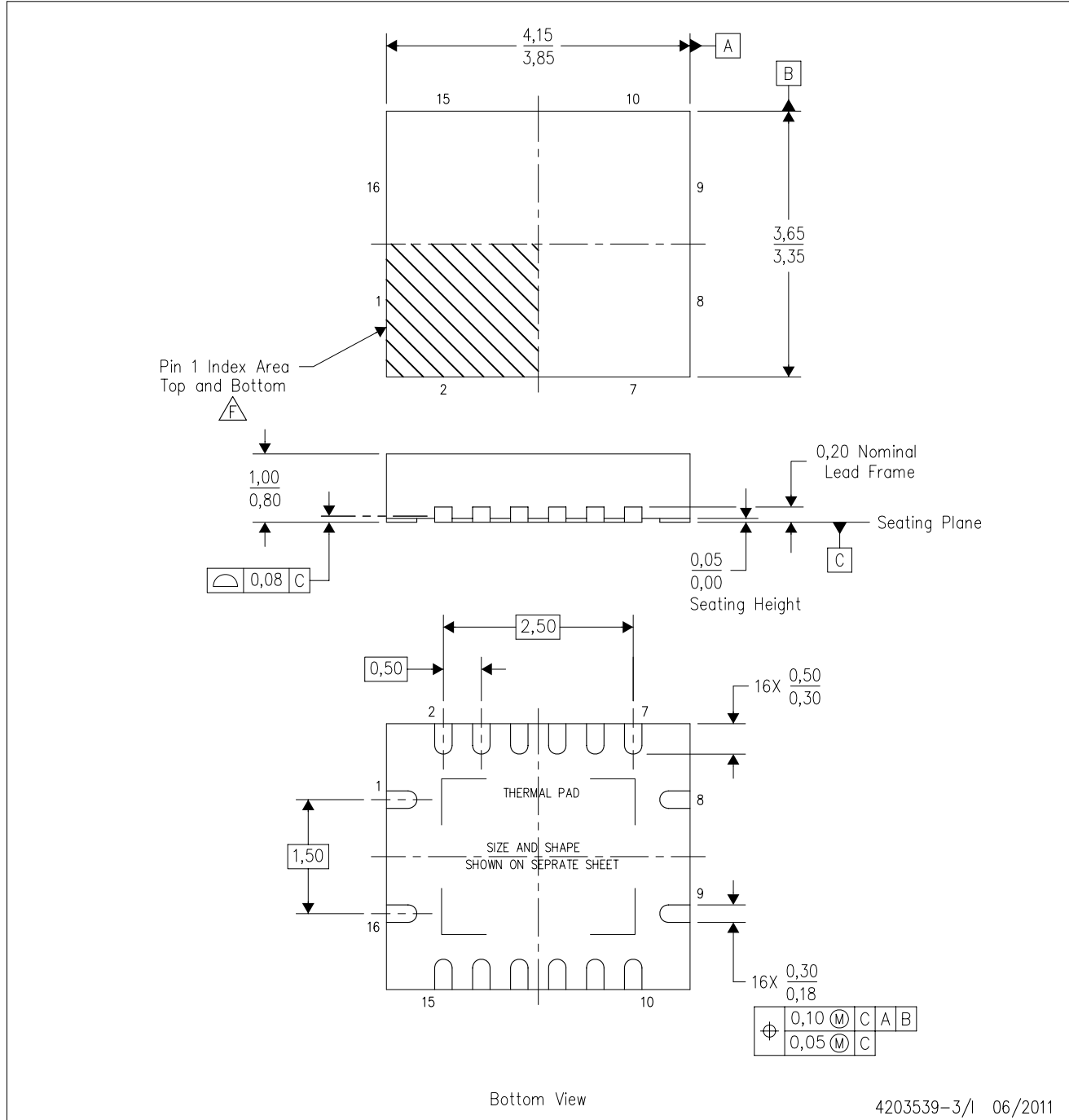
16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

RGY (R-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. QFN (Quad Flatpack No-Lead) package configuration.
 - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
 - G. Package complies to JEDEC MO-241 variation BA.

RGY (R-PVQFN-N16)

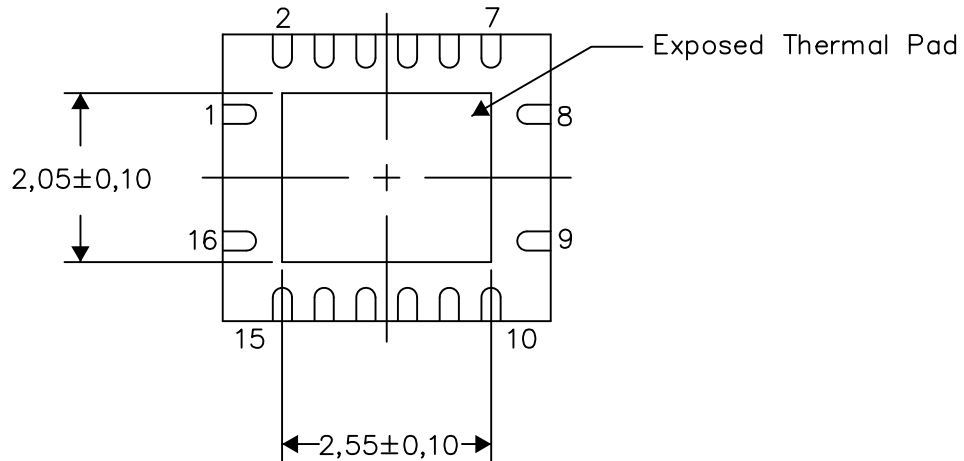
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

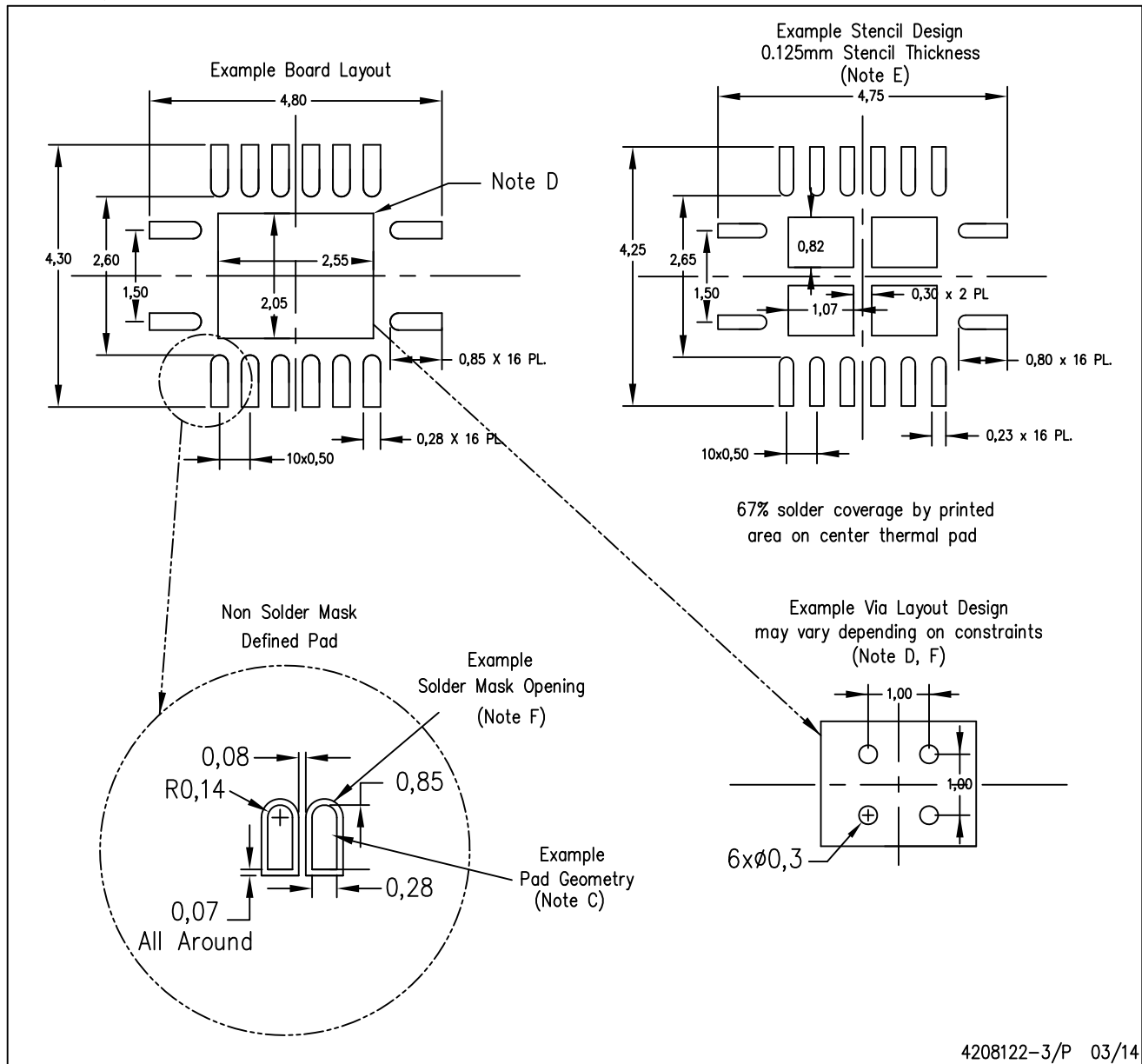
Exposed Thermal Pad Dimensions

4206353-3/P 03/14

NOTE: All linear dimensions are in millimeters

RGY (R-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



4208122-3/P 03/14

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

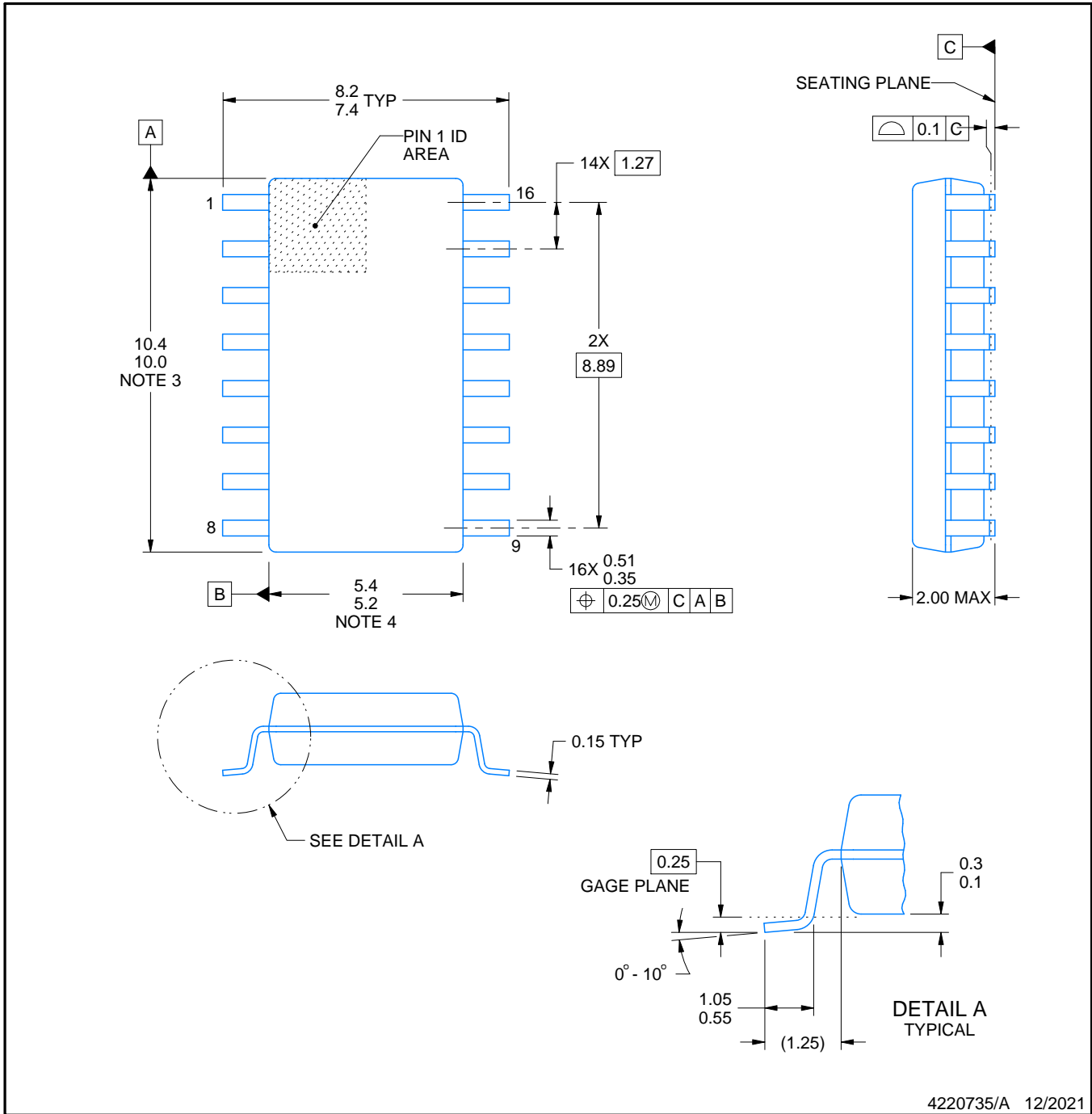


PACKAGE OUTLINE

NS0016A

SOP - 2.00 mm max height

SOP



4220735/A 12/2021

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

EXAMPLE BOARD LAYOUT

NS0016A

SOP - 2.00 mm max height

SOP



4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

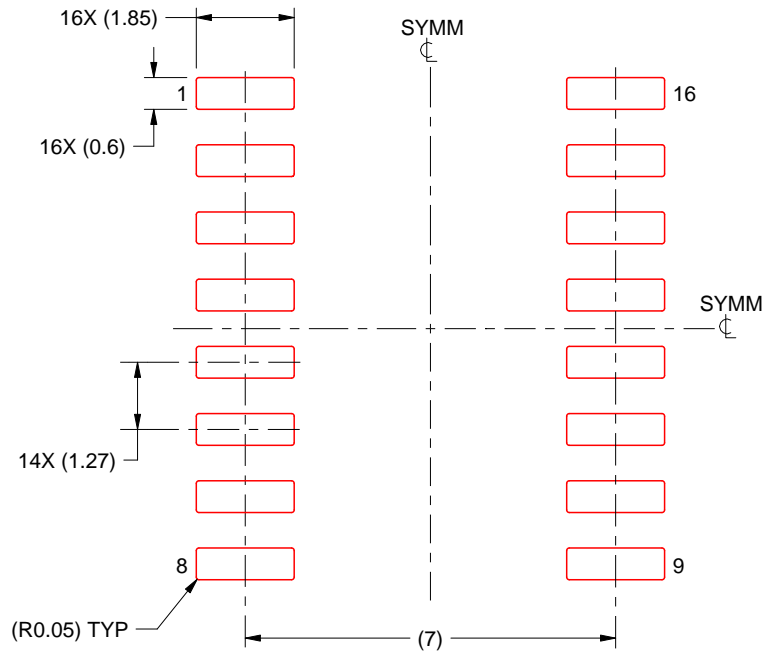
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

NS0016A

SOP - 2.00 mm max height

SOP



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

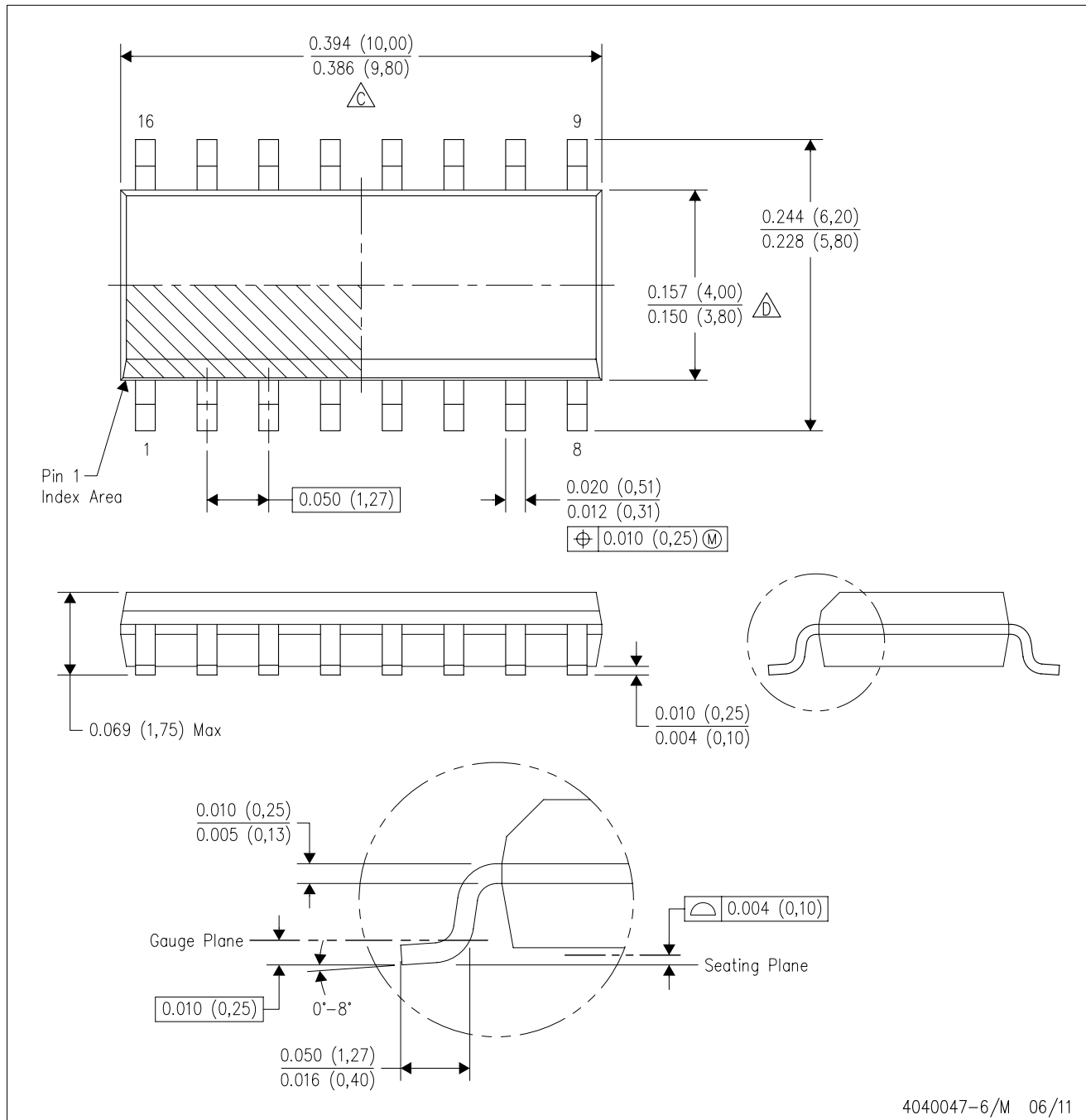
4220735/A 12/2021

NOTES: (continued)



7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

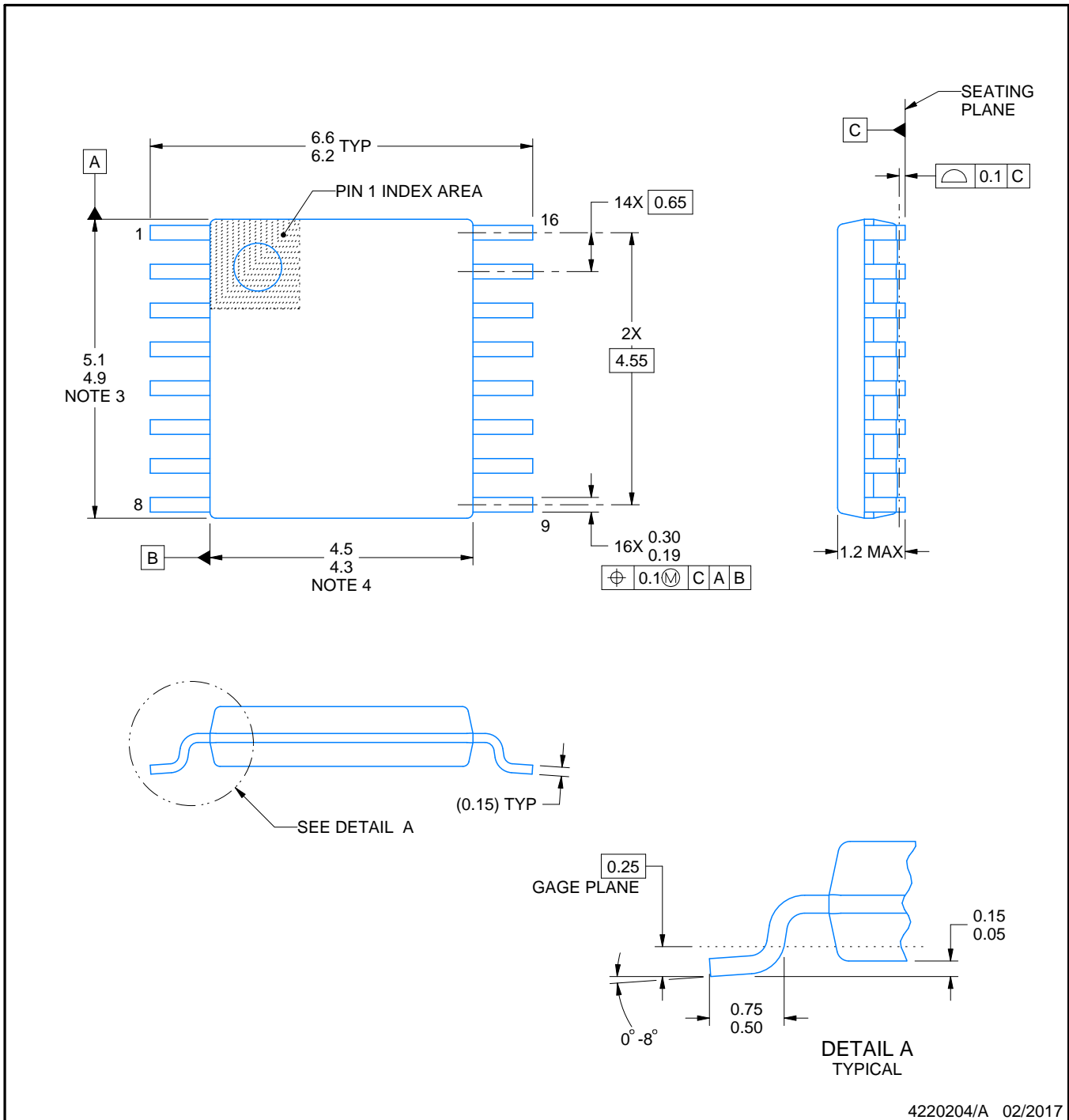
- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 -  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



4220204/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

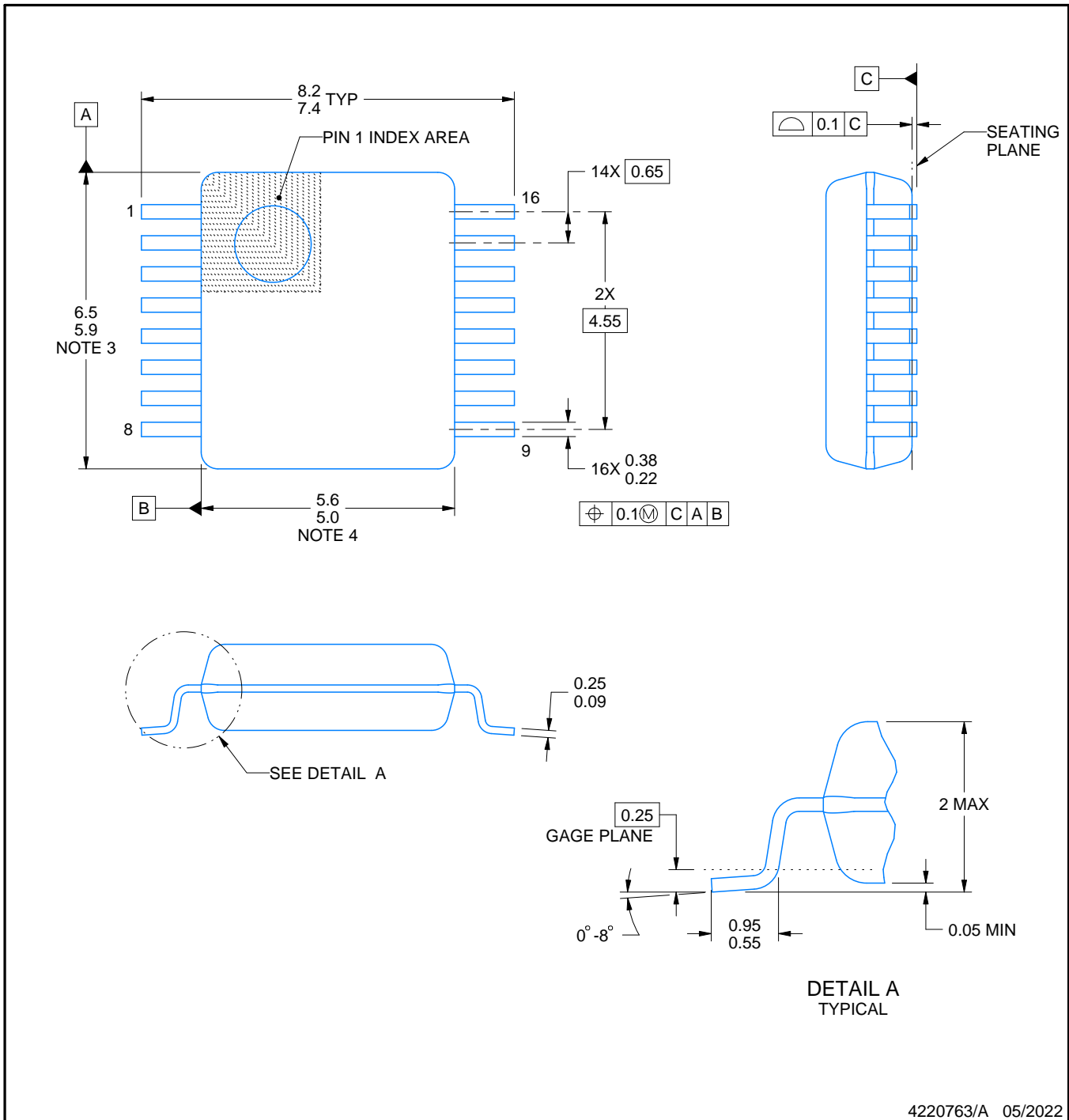
DB0016A



PACKAGE OUTLINE

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4220763/A 05/2022

NOTES:

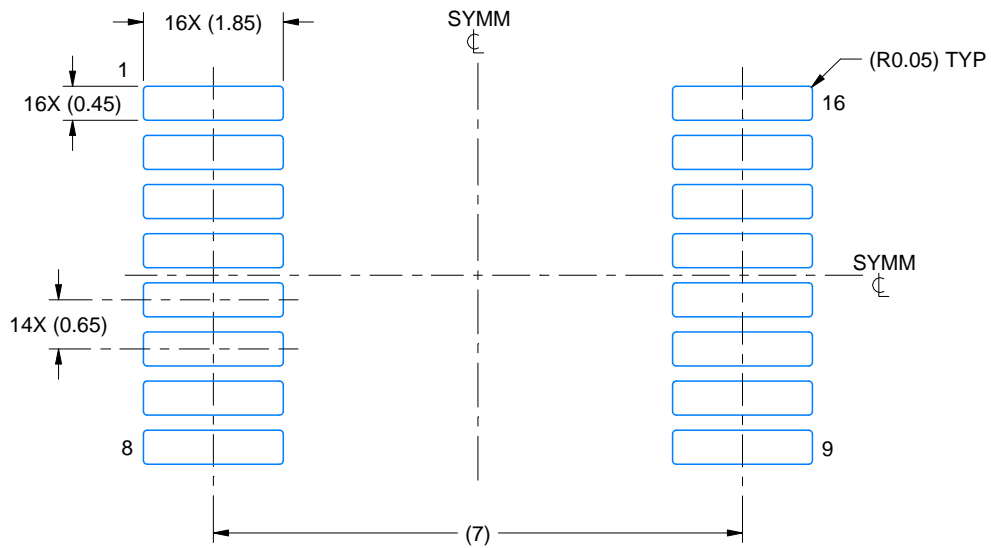
- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

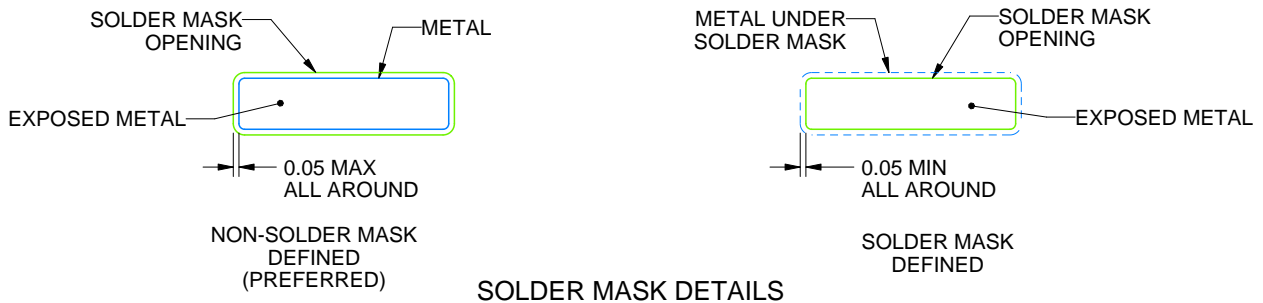
DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220763/A 05/2022

NOTES: (continued)

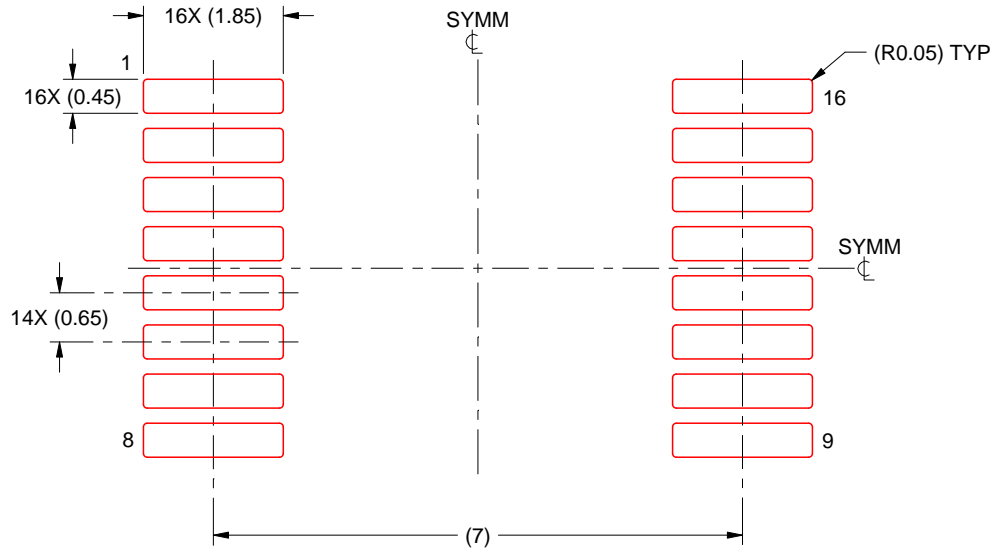
- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220763/A 05/2022

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

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