TLC555-Q1 Automotive LinCMOS™ Technology Timer

1 Features

- AEC-Q100 qualified for automotive applications:
  - Temperature grade 1: –40°C to +125°C, T_A
- Functional Safety-Capable
  - Documentation available to aid functional safety system design
- Very-low power consumption
  - 1mW (typical) at V_{DD} = 5V
- Capable of operation in astable mode
- CMOS output capable of swinging rail to rail
- High-output-current capability
  - Sink 100mA (typical)
  - Source 10mA (typical)
- Output fully compatible with CMOS, TTL, and MOS
- Low supply current reduces spikes during output transitions
- Single-supply operation from 2V to 15V
- Temperature range: –40°C to +125°C
- Functionally interchangeable with the NE555; has same pinout

2 Applications

- Precision timing
- Pulse generation
- Sequential timing
- Time delay generation
- Pulse width modulation
- Pulse position modulation
- Linear ramp generators
- Automotive lamp and LED lighting
- Telematics

3 Description

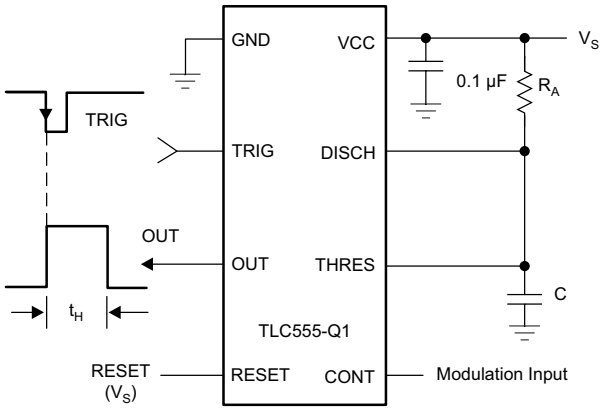
The TLC555-Q1 is a monolithic timing circuit fabricated using TI LinCMOS™ technology. The timer is fully compatible with CMOS, TTL, and MOS logic and operates at frequencies up to 2MHz. As a result of the high input impedance, this device supports smaller timing capacitors than capacitors used by the NE555. Thus, more accurate time delays and oscillations are possible. Power consumption is low across the full power-supply voltage range.

Like the NE555, the TLC555-Q1 has a trigger level equal to approximately one-third of the supply voltage, and a threshold level equal to approximately two-thirds of the supply voltage. These levels can be altered by using the control voltage pin (CONT). When the trigger input (TRIG) falls below the trigger level, the flip-flop is set, and the output goes high. If TRIG is greater than the trigger level and the threshold input (THRES) is greater than the threshold level, the flip-flop is reset and the output goes low. The reset input (RESET) can override all other inputs and is used to initiate a new timing cycle. If RESET is low, the flip-flop is reset and the output goes low. Whenever the output is low, a low-impedance path is provided between the discharge pin (DISCH) and GND. Tie all unused inputs to an appropriate logic level to prevent false triggering.

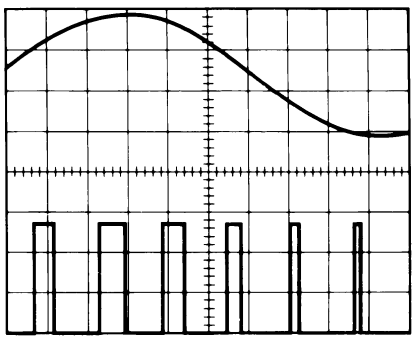
Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TLC555-Q1	SOIC (8)	4.9mm × 6.0mm

(1) For more information, see Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Pulse Width Modulator



Pulse Width Modulator Waveform:
Top Waveform - Modulation
Bottom Waveform - Output Voltage

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4 Pin Configuration and Functions

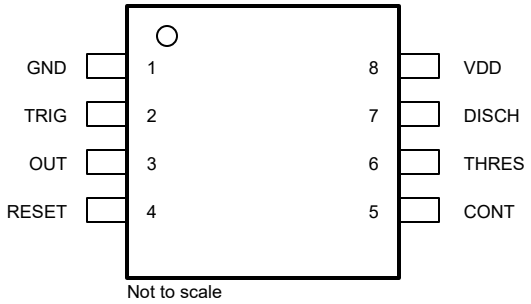


Figure 4-1. D Package, 8-Pin SOIC, (Top View)

Table 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
CONT	5	Input/Output	Controls comparator thresholds. Outputs 2/3 V_{DD}, allows bypass capacitor connection.
DISCH	7	Output	Open collector output to discharge timing capacitor
GND	1	—	Ground
OUT	3	Output	High current timer output signal
RESET	4	Input	Active low reset input forces output and discharge low
THRES	6	Input	End of timing input. THRES > CONT sets output low and discharge low.
TRIG	2	Input	Start of timing input. TRIG < ½ CONT sets output high and discharge open.
VDD	8	—	Input supply voltage, 2 V to 15 V

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{DD}	Supply voltage(2)			18	V
V_I	Input voltage, any input		–0.3	V_{DD}	V
	Sink current, discharge or output			150	mA
I_O	Source current, output			15	mA
	Continuous total power rating(3)	$T_A \le 25°C$		900	mW
		$T_A = 125°C$		180	
	Continuous total power dissipation derating factor(3), $T_A \ge 25°C$			7.2	mW/°C
T_A	Operating free-air temperature		–40	125	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network GND.
(3) See *Thermal Information*.

5.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)		±1000	V
		Charged-device model (CDM), per AEC Q100-011	All pins	±500	
			Corner pins (1, 4, 5, and 8)	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V_{DD}	Supply voltage	2	15	V
T_A	Operating free-air temperature	–40	125	°C

5.4 Thermal Information

THERMAL METRIC(1)		TLC555-Q1 D (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	138.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	78.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	87.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	23.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	86.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.5 Electrical Characteristics: V_{DD} = 5 V

V_{DD} = 5 V, at specified free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS (1)		MIN	TYP	MAX	UNIT
V_{IT}	Threshold voltage	25°C		2.8	3.3	3.8	V
		Full range		2.7		3.9	
I_{IT}	Threshold current	25°C			10		pA
		Full range			5000		
$V_{I(TRIG)}$	Trigger voltage	25°C		1.36	1.66	1.96	V
		Full range		1.26		2.06	
$I_{I(TRIG)}$	Trigger current	25°C			10		pA
		Full range			5000		
$V_{I(RESET)}$	Reset voltage	25°C		0.4	1.1	1.5	V
		Full range		0.3		1.8	
$I_{I(RESET)}$	Reset current	V_{RESET} = V_{DD}	25°C		10		pA
			Full range		5000		
		V_{RESET} = 0 V	25°C		5.9		µA
			Full range		6		
	Control voltage (open-circuit) as a percentage of supply voltage	Full range			66.7%		
	Discharge-switch on-state voltage	I_{OL} = 10 mA	25°C		0.14	0.5	V
			Full range			0.6	
	Discharge-switch off-state current	25°C			0.1		nA
		Full range			120		
V_{OH}	High-level output voltage	I_{OH} = –1 mA	25°C	4.1	4.8		V
			Full range	4.1			
V_{OL}	Low-level output voltage	I_{OL} = 8 mA	25°C		0.21	0.4	V
			Full range			0.6	
		I_{OL} = 5 mA	25°C		0.13	0.3	
			Full range			0.45	
		I_{OL} = 3.2 mA	25°C		0.08	0.3	
			Full range			0.4	
I_{DD}	Supply current(2)	25°C			180	350	µA
		Full range				700	

(1) Full-range T_A is –40°C to 125°C.
(2) These values apply for the expected operating configurations in which THRES is connected directly to DISCH or TRIG.

5.6 Electrical Characteristics: V_{DD} = 15 V

V_{DD} = 15 V, at specified free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS (1)		MIN	TYP	MAX	UNIT
V_{IT}	Threshold voltage	25°C		9.45	10	10.55	V
		Full range		9.35		10.65	
I_{IT}	Threshold current	25°C			10		pA
		Full range			5000		
$V_{I(TRIG)}$	Trigger voltage	25°C		4.65	5	5.35	V
		Full range		4.55		5.45	
$I_{I(TRIG)}$	Trigger current	25°C			10		pA
		Full range			5000		
$V_{I(RESET)}$	Reset voltage	25°C		0.4	1.1	1.5	V
		Full range		0.3		1.8	
$I_{I(RESET)}$	Reset current	V_{RESET} = V_{DD}	25°C		10		pA
			Full range		5000		
		V_{RESET} = 0 V	25°C		17.8		µA
			Full range		18		
	Control voltage (open-circuit) as a percentage of supply voltage	Full range			66.7%		
	Discharge-switch on-state voltage	I_{OL} = 100 mA	25°C		0.77	1.7	V
			Full range			1.8	
	Discharge switch off-state current	25°C			0.1		nA
		Full range			120		
V_{OH}	High-level output voltage	I_{OH} = –10 mA	25°C	12.5	14.2		V
			Full range	12.5			
		I_{OH} = –5 mA	25°C	13.5	14.6		
			Full range	13.5			
		I_{OH} = –1 mA	25°C	14.2	14.9		
			Full range	14.2			
V_{OL}	Low-level output voltage	I_{OL} = 100 mA	25°C		1.28	3.2	V
			Full range			3.8	
		I_{OL} = 50 mA	25°C		0.63	1	
			Full range			1.5	
		I_{OL} = 10 mA	25°C		0.12	0.3	
			Full range			0.45	
I_{DD}	Supply current(2)	25°C			360	600	µA
		Full range				1000	

(1) Full-range T_A is –40°C to 125°C.
(2) These values apply for the expected operating configurations in which THRES is connected directly to DISCH or TRIG.

5.7 Switching Characteristics

at V_{DD} = 5 V, T_A = 25°C (unless otherwise noted); characteristic values are specified by design, characterization, or both

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Supply voltage sensitivity of timing interval	V_{DD} = 5 V to 15 V, C_T = 0.1 µF R_A = R_B = 1 kΩ to 100 kΩ (1)		0.1	0.5	%/V
t_r	Output pulse rise time	R_L = 10 MΩ, C_L = 10 pF		20	75	ns
t_f	Output pulse fall time	R_L = 10 MΩ, C_L = 10 pF		15	60	ns
f_{max}	Maximum frequency in astable mode	R_A = 470 Ω, C_T = 200 pF R_B = 200 Ω (1)	1.2	2.1		MHz

(1) R_A, R_B, and C_T are as defined in Figure 5-1.

5.8 Typical Characteristics

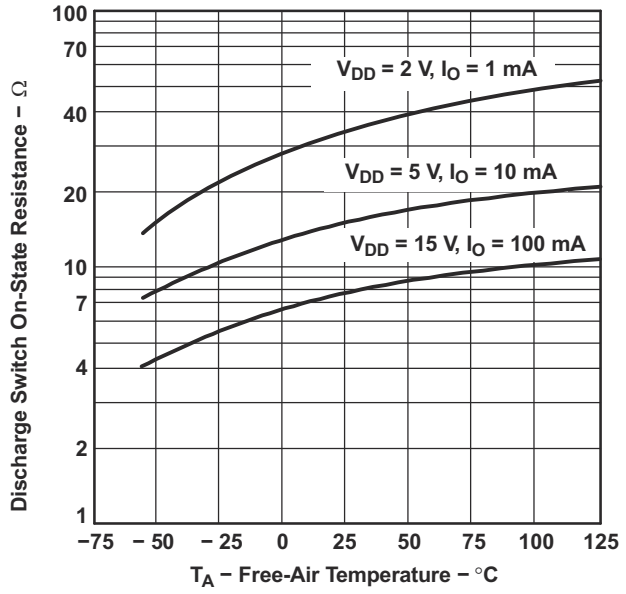
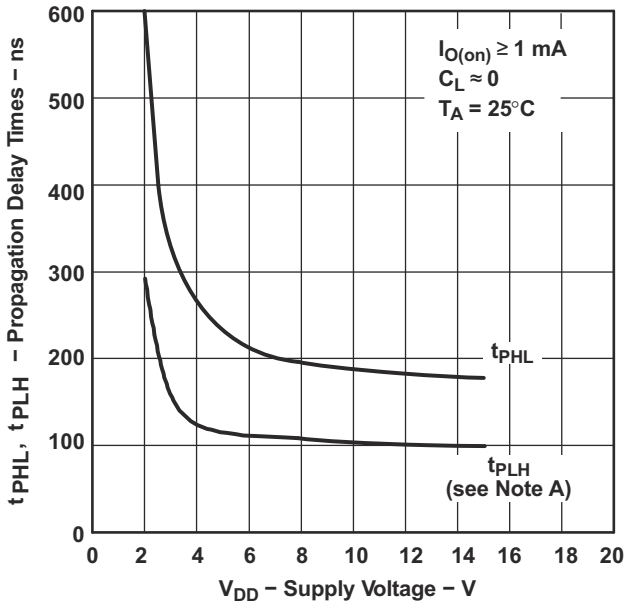


Figure 5-1. Discharge Switch ON-State Resistance vs Free-Air Temperature



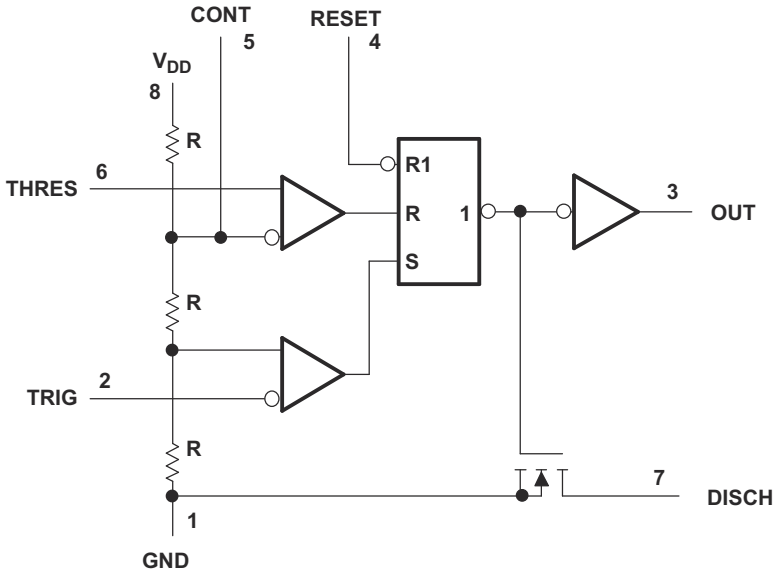
A. The effects of the load resistance on these values must be taken into account separately.

Figure 5-2. Propagation Delay Times to Discharge Output from Trigger and Threshold Shorted Together vs Supply Voltage

6 Detailed Description

6.1 Overview

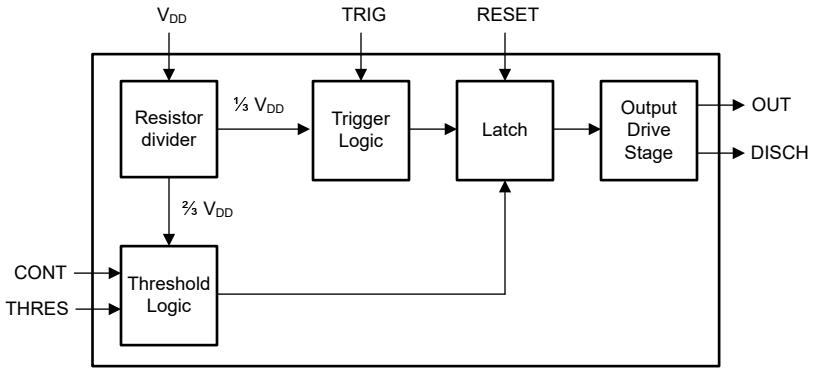
The TLC555-Q1 timer is used for general-purpose timing applications from 476 ns to hours or from < 1 MHz to 2.1 MHz. All inputs are level sensitive, and not edge-triggered.



Note: RESET can override TRIG, which can override THRES.

Figure 6-1. Simplified Schematic

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Monostable Operation

For monostable operation, Figure 6-2 shows how any of these timers can be connected. If the output is low, application of a negative-going pulse to the trigger (TRIG) sets the flip-flop ($\overline{Q}$ goes low), drives the output high, and turns off Q1. Capacitor C charges through R_A until the voltage across the capacitor reaches the threshold voltage of the threshold (THRES) input. If TRIG returns to a high level, the output of the threshold comparator resets the flip-flop ($\overline{Q}$ goes high), drives the output low, and discharges C through Q1.

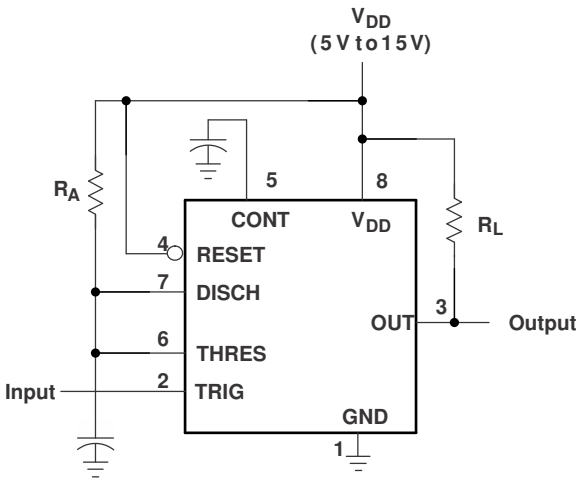


Figure 6-2. Circuit for Monostable Operation

Monostable operation is initiated when TRIG voltage falls below the trigger threshold. When initiated, the sequence ends only if TRIG is high for at least 10 µs before the end of the timing interval. When the trigger is grounded, the comparator storage time can be as long as 10 µs, which limits the minimum monostable pulse duration to 10 µs. Because of the threshold level and saturation voltage of Q1, the output pulse duration is approximately $t_w = 1.1R_AC$. Figure 6-3 is a plot of the time constant for various values of R_A and C. The threshold levels and charge rates are directly proportional to the supply voltage (V_{DD}). As a result, the timing interval is independent of the supply voltage if the supply voltage is constant during the time interval.

Applying a negative-going trigger pulse simultaneously to RESET and TRIG during the timing interval discharges C and reinitiates the cycle, commencing on the positive edge of the reset pulse. The output is held low as long as the reset pulse is low. To prevent false triggering, connect RESET to V_{DD} when RESET is not being used. If the RESET function is required and the pin is driven by external logic or a microcontroller, use a pullup resistor to V_{DD} (such as 10 kΩ) to prevent the RESET pin from floating. If the RESET function is not required, short the RESET pin directly to the V_{DD} pin.

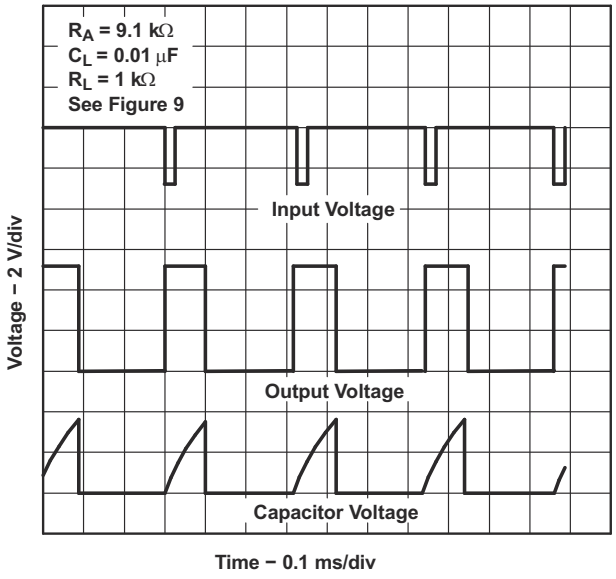


Figure 6-3. Typical Monostable Waveforms

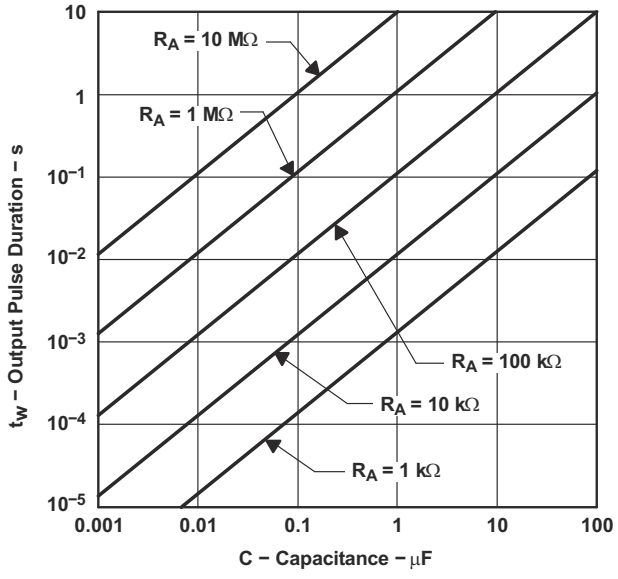
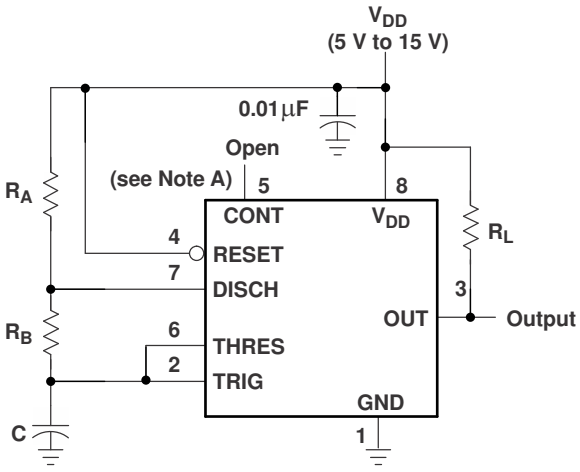


Figure 6-4. Output Pulse Duration vs Capacitance

6.3.2 Astable Operation

Figure 6-5 shows that adding a second resistor (R_B) to the circuit and connecting the trigger input to the threshold input causes the timer to self-trigger and run as a multivibrator. The C capacitor charges through R_A and R_B and then only discharges through R_B. As a result, the values of R_A and R_B control the duty cycle.

This astable connection results in the C capacitor charging and discharging between the threshold-voltage level (≈ 0.67 × V_{DD}) and the trigger-voltage level (≈ 0.33 × V_{DD}). As in the monostable circuit, charge and discharge times (and as a result, the frequency and duty cycle) are independent of the supply voltage.



A. Decoupling CONT voltage to ground with a capacitor can improve operation. This must be evaluated for individual applications.

Figure 6-5. Circuit for Astable Operation

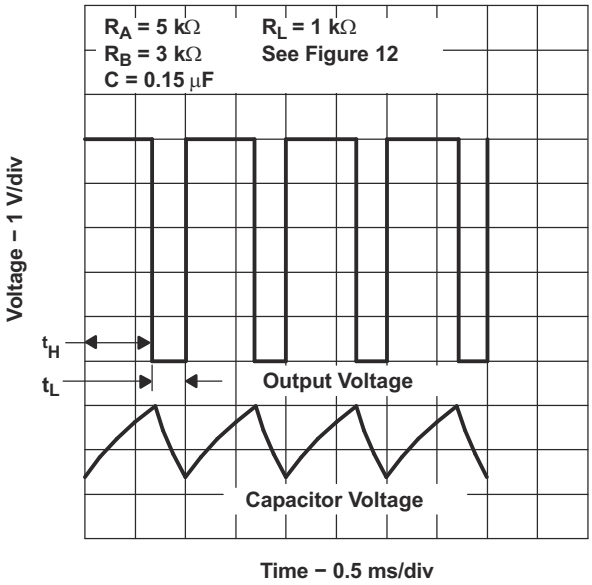


Figure 6-6. Typical Astable Waveforms

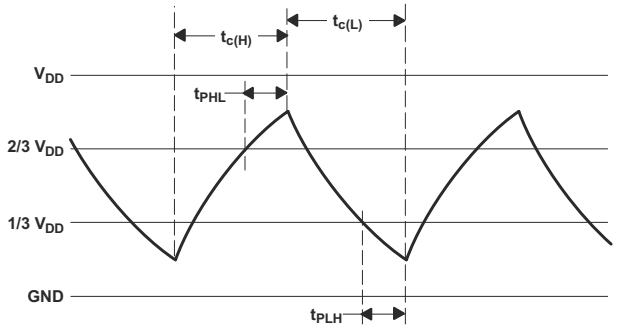


Figure 6-7. Trigger and Threshold Voltage Waveform

Figure 6-7 shows typical waveforms generated during astable operation. Calculate the output high-level duration (t_H) and low-level duration t_L for frequencies less than or equal to 100 kHz as follows:

$$t_H = 0.693(R_A + R_B)C \quad (1)$$

$$t_L = 0.693(R_B)C \quad (2)$$

Other useful relationships are shown as follows:

$$\text{period} = t_H + t_L = 0.693(R_A + 2R_B)C \quad (3)$$

$$\text{frequency} \approx \frac{1.44}{(R_A + 2R_B)C} \quad (4)$$

$$\text{Output driver duty cycle} = \frac{t_L}{t_H + t_L} = \frac{R_B}{R_A + 2R_B} \quad (5)$$

$$\text{Output waveform duty cycle} = \frac{t_H}{t_H + t_L} = 1 - \frac{R_B}{R_A + 2R_B} \quad (6)$$

$$\text{Low-to-high ratio} = \frac{t_L}{t_H} = \frac{R_B}{R_A + R_B} \quad (7)$$

Equation 1 to Equation 7 do not account for any propagation delay times from the TRIG and THRES inputs to DISCH output. These delay times add directly to the period and overcharge the capacitor, which creates differences between calculated and actual values that increase with frequency. In addition, the internal on-state resistance r_{on} during discharge adds to R_B to provide another source of timing error in the calculation when R_B is very low. The following equations provide better agreement with measured values. The formulas in Equation 8 represent the actual low and high times when used at higher frequencies (beyond 100 kHz) because propagation delay and discharge on resistance is added to the formulas. The value of C_T includes both the nominal or deliberate timing capacitance, as well as parasitic capacitance on the PCB. Decoupling capacitance on CONT also affects the duty cycle, with an error contribution that depends on the capacitor leakage resistance. For additional discussion, see the *Design low-duty-cycle timer circuits* article.

$$t_{c(H)} = C_T (R_A + R_B) \ln\left[3 - \exp\left(\frac{-t_{PLH}}{C_T(R_B + r_{on})}\right)\right] + t_{PHL}$$

$$t_{c(L)} = C_T (R_B + r_{on}) \ln\left[3 - \exp\left(\frac{-t_{PHL}}{C_T(R_A + R_B)}\right)\right] + t_{PLH} \quad (8)$$

These equations and those given earlier are similar in that a time constant is multiplied by the logarithm of a number or function. The limit values of the logarithmic terms must be between ln(2) at low frequencies, and ln(3) at extremely high frequencies. For a duty cycle close to 50%, an appropriate constant for the logarithmic terms can be substituted with good results. Output waveform duty cycles less than 50% require that $t_{c(H)} / t_{c(L)} < 1$ and possibly that $R_A \leq r_{on}$. These conditions can be difficult to obtain. Figure 6-8 shows the nominal free-running frequency associated with various combinations of C_T and $R_A + 2 \times R_B$.

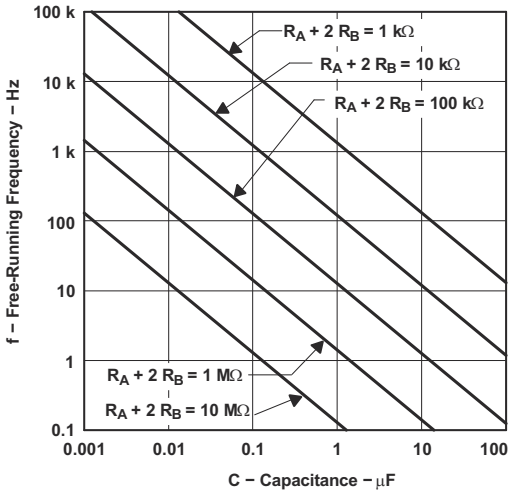


Figure 6-8. Free-Running Frequency

6.3.3 Frequency Divider

By adjusting the length of the timing cycle, the basic circuit of the TLC555-Q1 can operate as a frequency divider. Figure 6-9 shows a divide-by-three circuit that reinforces that re-triggering cannot occur during the timing cycle.

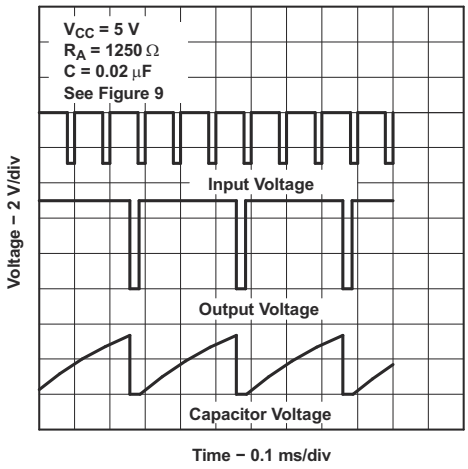


Figure 6-9. Divide-by-Three Circuit Waveforms

6.4 Device Functional Modes

Table 6-1 lists the device functional modes. For a valid reset voltage condition, use an external pullup resistor to V_{DD} (if using the RESET functionality), or short the RESET pin directly to V_{DD} (if the RESET functionality is not used).

Table 6-1. Function Table

RESET	TRIGGER VOLTAGE(1)	THRESHOLD VOLTAGE(1)	OUTPUT	DISCHARGE SWITCH
Low	Irrelevant	Irrelevant	Low	On
High	< 1/3 V_{DD}	Irrelevant	High	Off
High	> 1/3 V_{DD}	> 2/3 V_{DD}	Low	On
High	> 1/3 V_{DD}	< 2/3 V_{DD}	As previously established	

(1) Voltage levels shown are nominal.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The TLC555-Q1 timer device uses resistor and capacitor charging delay to provide a programmable time delay or operating frequency. The following section presents a simplified discussion of the design process.

7.2 Typical Applications

7.2.1 Missing-Pulse Detector

The circuit shown in Figure 7-1 can detect a missing pulse or abnormally long spacing between consecutive pulses in a train of pulses. The timing interval of the mono-stable circuit is re-triggered continuously by the input pulse train if the pulse spacing is less than the timing interval. A longer pulse spacing, missing pulse, or terminated pulse train permits the timing interval to be completed, which generates an output pulse as shown in Figure 7-2.

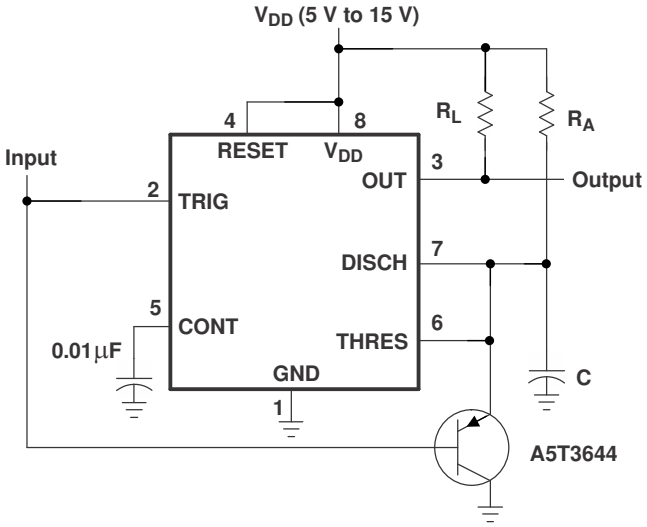


Figure 7-1. Circuit for Missing-Pulse Detector

7.2.1.1 Design Requirements

Input fault (missing pulses) must be input high. Input stuck low is not detected because timing capacitor (C) remains discharged.

7.2.1.2 Detailed Design Procedure

Select R_A and C so that $R_A \times C$ > [maximum normal input high time]. R_L improves V_{OH}, but is not required for TTL compatibility.

7.2.1.3 Application Curve

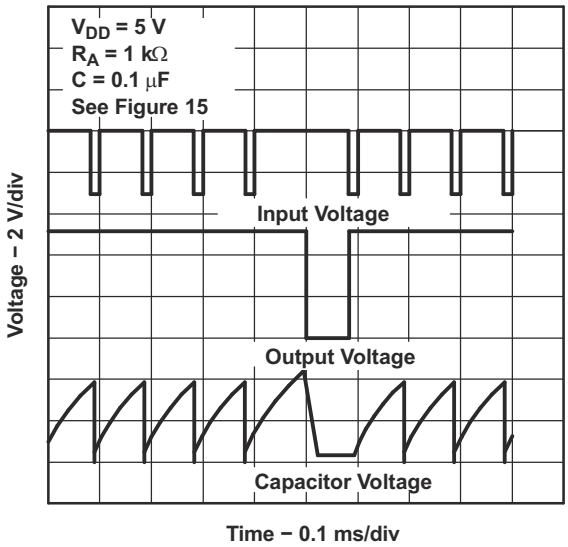
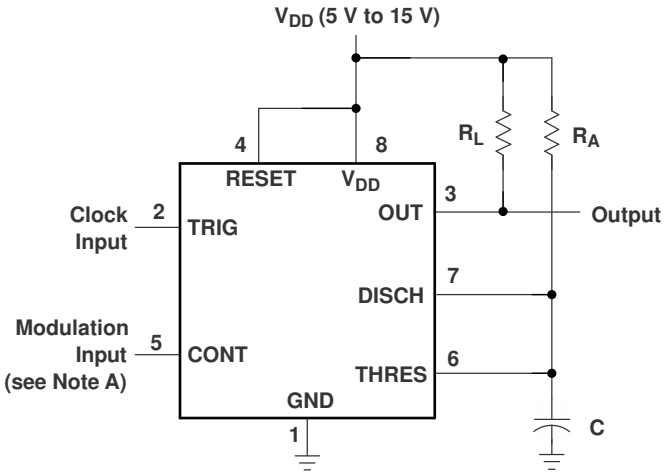


Figure 7-2. Completed Timing Waveforms for Missing-Pulse Detector

7.2.2 Pulse-Width Modulation

The operation of the timer can be modified by modulating the internal threshold and trigger voltages by applying an external voltage (or current) to CONT. Figure 7-3 shows a circuit for pulse-width modulation. A continuous input pulse train triggers the mono-stable circuit, and a control signal modulates the threshold voltage. Figure 7-4 shows the resulting output pulse-width modulation. While a sine-wave modulation signal is shown, any wave shape can be used.



A. The modulating signal can be direct or capacitively coupled to CONT. For direct coupling, the effects of modulation source voltage and impedance on the bias of the timer must be considered.

Figure 7-3. Circuit for Pulse-Width Modulation

7.2.2.1 Design Requirements

Clock input must have V_{OL} and V_{OH} levels that are less than and greater than 1/3 VDD. Modulation input can vary from ground to VDD. The application must be tolerant of a nonlinear transfer function; the relationship between modulation input and pulse width is not linear because the capacitor charge is based RC on an negative exponential curve.

7.2.2.2 Detailed Design Procedure

Select R_A and C so that $R_A \times C = 1/4$ [clock input period]. R_L improves V_{OH}, but is not required for TTL compatibility.

7.2.2.3 Application Curve

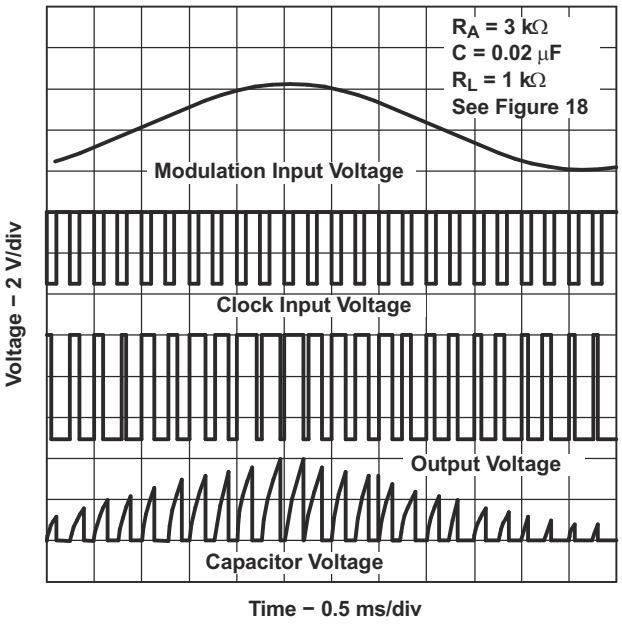
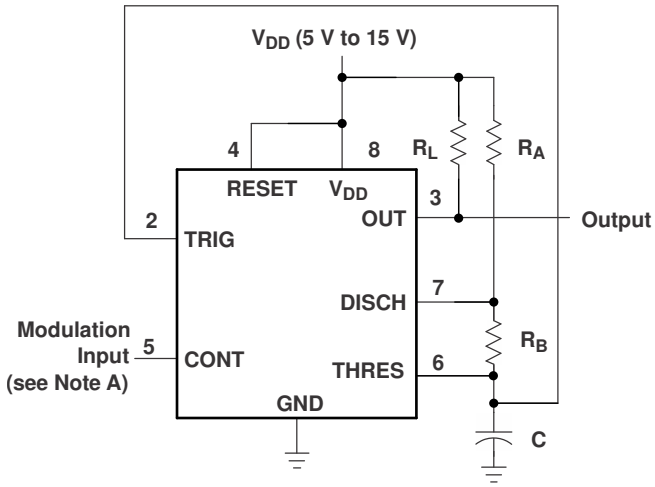


Figure 7-4. Pulse-Width-Modulation Waveforms

7.2.3 Pulse-Position Modulation

As shown in Figure 7-5, any of these timers can be used as a pulse-position modulator. This application modulates the threshold voltage and the time delay of a free-running oscillator. Figure 7-6 shows a triangular-wave modulation signal for this type of circuit; however, any wave shape can be used.



A. The modulating signal can be direct or capacitively coupled to CONT. For direct coupling, the effects of modulation source voltage and impedance on the bias of the timer must be considered.

Figure 7-5. Circuit for Pulse-Position Modulation

7.2.3.1 Design Requirements

Both DC and AC coupled modulation inputs change the upper and lower voltage thresholds for the timing capacitor. Both frequency and duty cycle vary with the modulation voltage.

7.2.3.2 Detailed Design Procedure

The nominal output frequency and duty cycle can be determined using formulas in *Section 6.3.2*. R_L improves V_{OH}, but is not required for TTL compatibility.

7.2.3.3 Application Curve

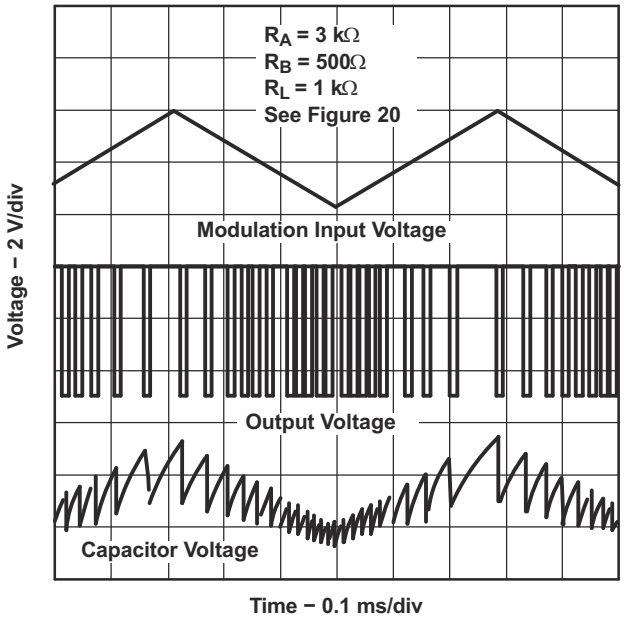
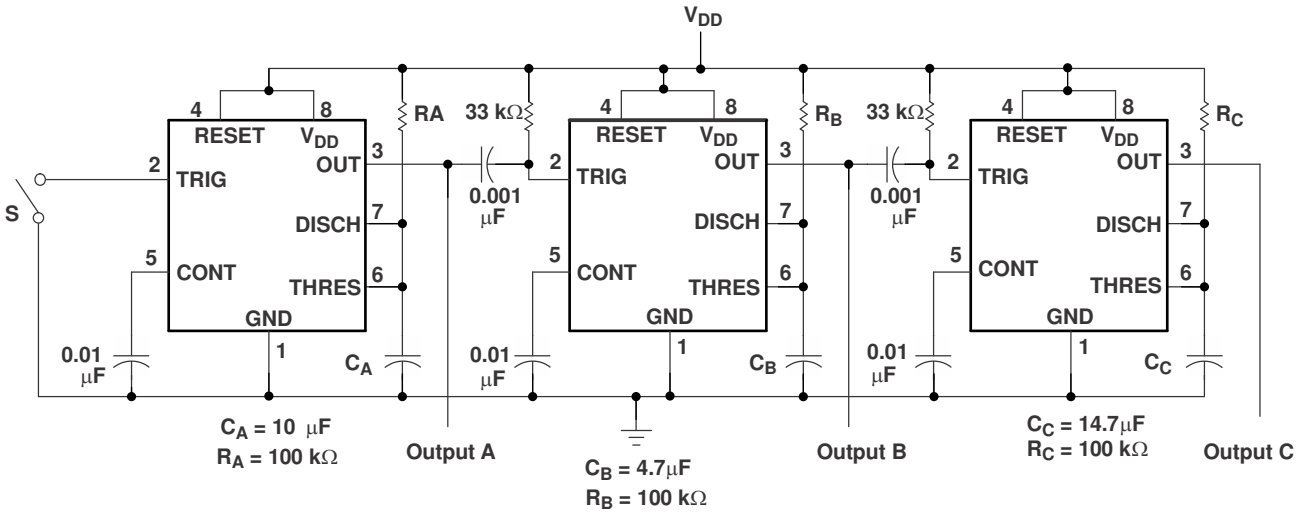


Figure 7-6. Pulse-Position-Modulation Waveforms

7.2.4 Sequential Timer

Many applications (such as computers) require signals for initializing conditions during start-up. Other applications (such as test equipment) require activation of test signals in sequence. These timing circuits can connect to provide sequential control. The timers can be used in various combinations of a-stable or mono-stable circuit connections with or without modulation for extremely flexible waveform control. Figure 7-7 shows a sequencer circuit with possible applications in many systems; Figure 7-8 shows the output waveforms.



NOTE A: S closes momentarily at t = 0.

Figure 7-7. Sequential Timer Circuit

7.2.4.1 Design Requirements

The sequential timer application chains together multiple mono-stable timers. The joining components are 33-kΩ resistors and 0.001-µF capacitors. The output high to low edge passes a 10-µs start pulse to the next mono-stable.

7.2.4.2 Detailed Design Procedure

The timing resistors and capacitors can be selected using this formula: $t_w = 1.1 \times R \times C$.

7.2.4.3 Application Curve

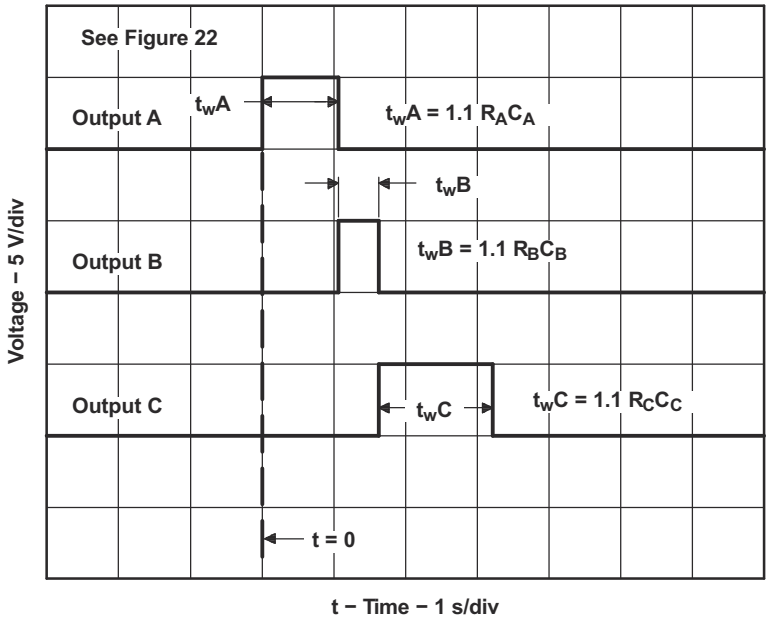


Figure 7-8. Sequential Timer Waveforms

7.3 Power Supply Recommendations

The TLC555-Q1 requires a voltage supply within 4.5 V to 15 V. Adequate power supply bypassing is required to protect associated circuitry. The minimum recommended value is 0.1 µF in parallel with a 1-µF electrolytic. Place the bypass capacitors as close as possible to the TLC555-Q1 and minimize the trace length.

7.4 Layout

7.4.1 Layout Guidelines

Standard PCB rules apply to routing the TLC555-Q1. The 0.1 µF in parallel with a 1-µF electrolytic capacitor must be as close as possible to the TLC555-Q1. The capacitor used for the time delay must be placed as close to the discharge pin. A ground plane on the bottom layer can provide better noise immunity and signal integrity.

7.4.2 Layout Example

Figure 7-9 shows the basic layout for various applications.

- C1 – based on time delay calculations
- C2 – 0.01-µF bypass capacitor for control voltage pin
- C3 – 0.1-µF bypass ceramic capacitor
- C4 – 1-µF electrolytic bypass capacitor
- R1 – based on time delay calculations

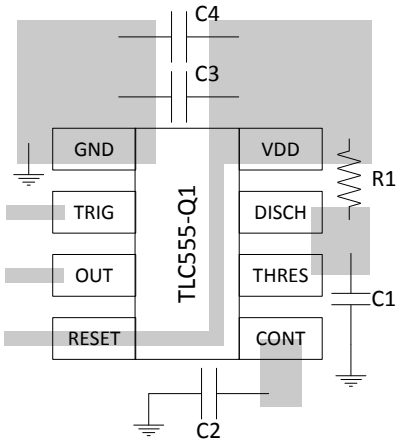


Figure 7-9. Recommended Layout

8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *TLC555-Q1 Used as a Positive and Negative Charge Pump* application note
- Texas Instruments, *EMC Compatible Automotive LED Rear Lamp With Sequential-Turn Animation Reference Design*

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (May 2015) to Revision C (April 2024)	Page
• Added reference to functional safety documentation in *Features*	1
• Deleted *Description (continued)* section	1
• Updated *Package Information* table	1
• Deleted *Dissipation Ratings* and moved continuous total power dissipation specifications to *Absolute Maximum Ratings*	3
• Changed continuous total power dissipation power rating from 725mW to 900mW at $T_A \leq 25°C$ and from 145mW to 180mW at $T_A = 125°C$, and changed derating factor $T_A = 25°C$ from 5.8mW/°C to 7.2mW/°C, in *Absolute Maximum Ratings*	3
• Updated thermal resistance and characterization parameter values in *Thermal Information*	3
• Changed reset current ($I_{I(RESET)}$) test conditions to $V_{RESET} = V_{DD}$ in both *Electrical Characteristics* tables	4
• Added new reset current ($I_{I(RESET)}$) typical values for test condition $V_{RESET} = 0V$ to both *Electrical Characteristics* tables	4
• Changed supply current typical value from 170 µA to 180 µA in *Electrical Characteristics: V_{DD} = 5 V*	4

- Changed title of *Operating Characteristics* table to *Switching Characteristics* and clarified that values are specified by design or characterization ... 6
- Deleted initial error of timing interval specification in *Switching Characteristics* ... 6
- Added text regarding input type to *Overview* ... 7
- Changed functional block diagram to simplified schematic and moved to *Overview* ... 7
- Added new *Functional Block Diagram* ... 7
- Added guidance for RESET pin pullup resistance in *Monostable Operation* ... 7
- Changed V_{CC} to V_{DD} in *Monostable Operation* ... 7
- Added clarity regarding nominal operating frequency and parasitic terms in *Astable Operation* ... 9
- Changed V_{CC} to V_{DD} in *Astable Operation* ... 9
- Deleted Figure 11, *Equivalent Schematic*, and added guidance concerning the RESET pin in *Device Functional Modes* ... 12
- Changed V_{CC} to V_{DD} in Table 6-1, *Function Table* ... 12
- Added references to application note and reference design in *Documentation Support* section ... 19

Changes from Revision A (October 2012) to Revision B (May 2015) **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document ... 1
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Revision * (October 2006) to Revision A (October 2012) **Page**

- Added AEC-Q100 qualifying text to *Features* section ... 1
- Updated data sheet text to the latest documentation and translation standards ... 1
- Updated next-to-last paragraph in *Description* and *Ordering Information* sections ... 1
- In the 5-V and 15-V Electrical Characteristics tables, changed all "MAX" entries in the T_A column to "Full range" ... 4
- Deleted the last Electrical Characteristics table, which contained only redundant data ... 6

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC555QDRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL555Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

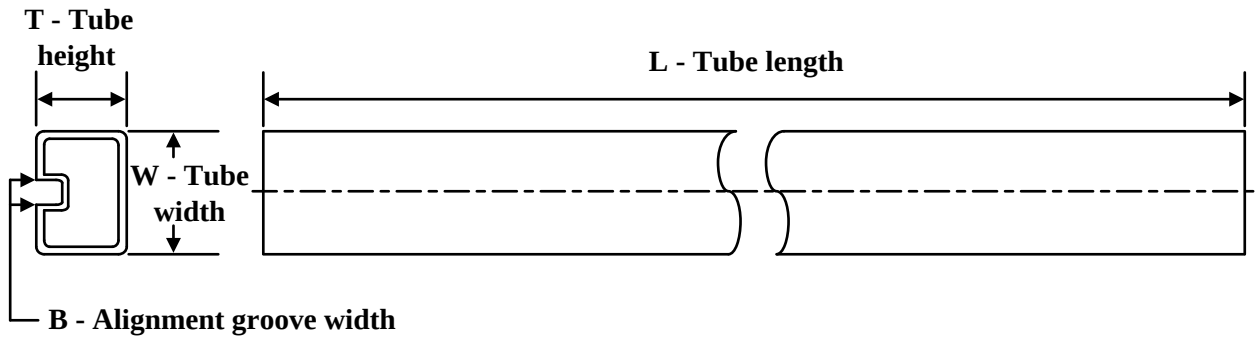
OTHER QUALIFIED VERSIONS OF TLC555-Q1 :

- Catalog : TLC555
- Military : TLC555M

NOTE: Qualified Version Definitions:

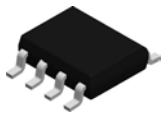
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TLC555QDRQ1	D	SOIC	8	2500	506.6	8	3940	4.32

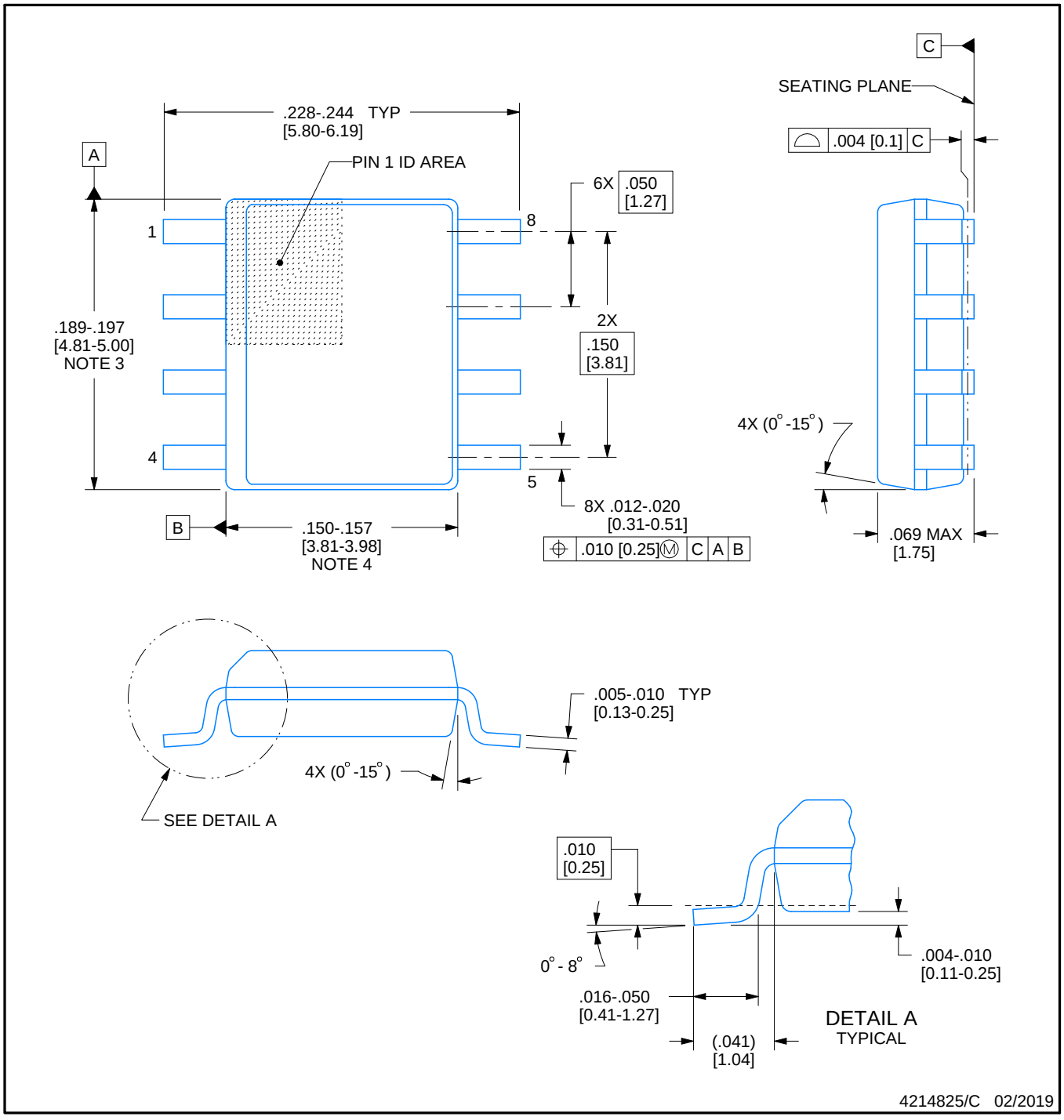


PACKAGE OUTLINE

D0008A

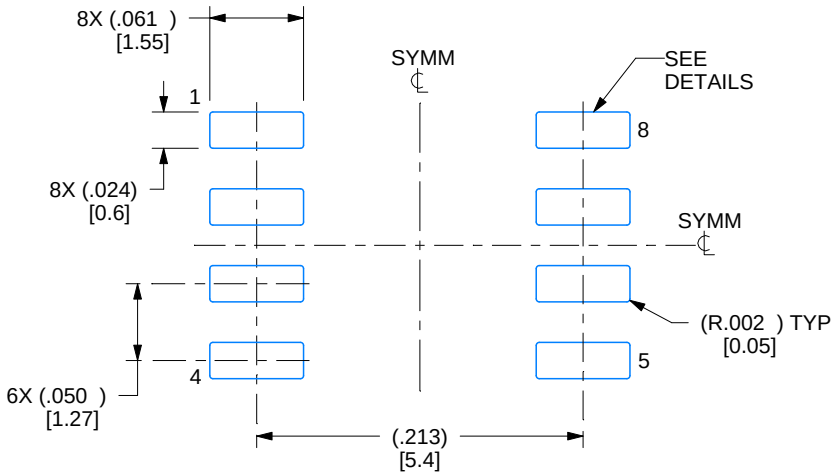
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

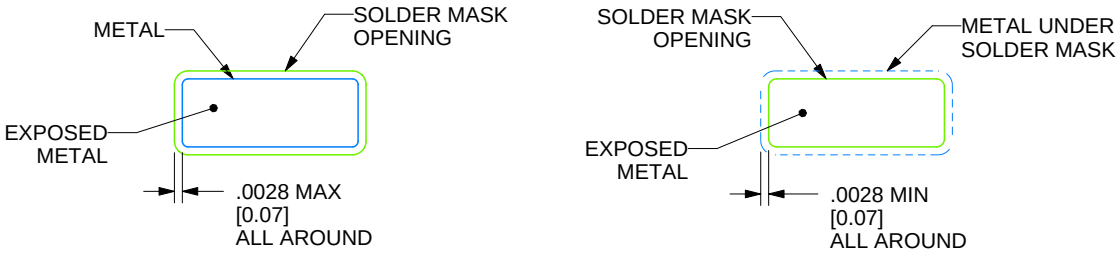


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

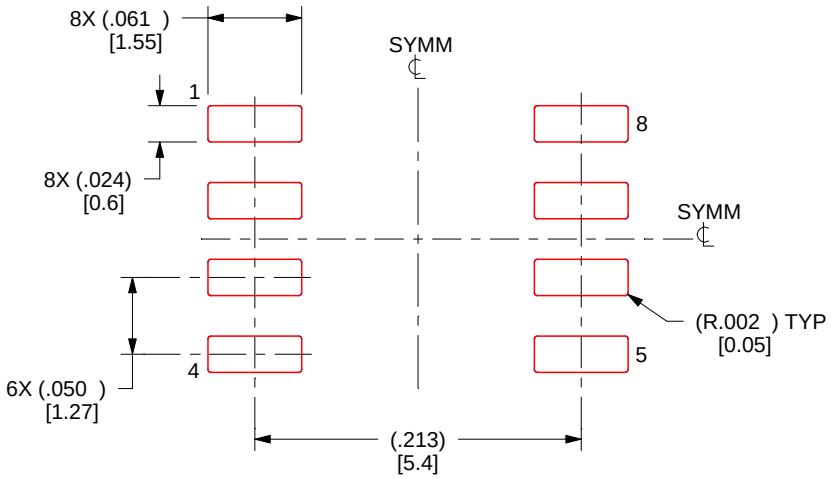
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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