TPD2E2U06 Dual-Channel High-Speed ESD Protection Device

1 Features

- IEC 61000-4-2 Level 4
  - ±25 kV (Contact discharge)
  - ±30 kV (Air-gap discharge)
- IEC 61000-4-5 Surge protection
  - 5.5-A Peak pulse current (8/20 µs Pulse)
- IO Capacitance 1.5 pF (Typ)
- DC Breakdown voltage 6.5 V (Min)
- Ultra-Low leakage current 10 nA (Max)
- Low ESD clamping voltage
- Industrial temperature range: –40°C to +125°C
- Small easy-to-route DRL and DCK package

2 Applications

- End Equipment
  - Set Top Box
  - Notebook
  - Server
  - Electronic Point of Sale (EPOS)
- Interfaces
  - USB 2.0
  - Ethernet
  - MIPI Bus
  - LVDS
  - I2C

3 Description

The TPD2E2U06 is a dual-channel low capacitance TVS diode ESD protection device. The device offers ±25-kV contact and ±30-kV air-gap ESD protection in accordance with the IEC 61000-4-2 standard. The 1.5-pF line capacitance of the TPD2E2U06 makes the device suitable for a wide range of applications. Typical application interfaces are USB 2.0, LVDS, and I^{2}C™.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPD2E2U06DRL	SOT (5)	1.60 mm × 1.20 mm
TPD2E2U06DCK	SC70 (3)	2.0 mm × 1.25 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic

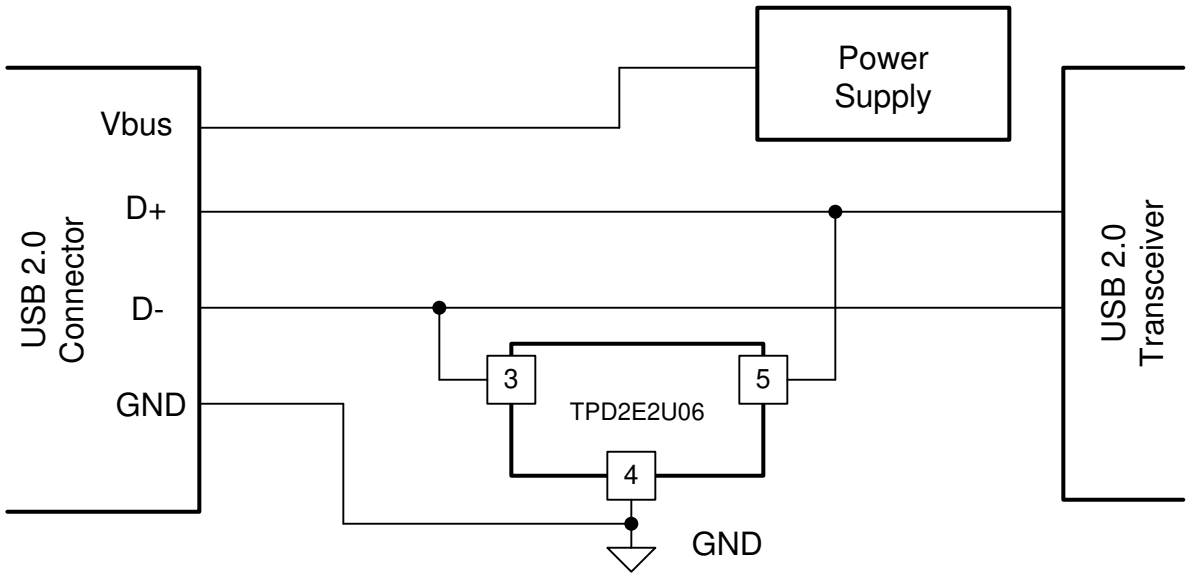


Table of Contents

4 Revision History

Changes from Revision B (May 2015) to Revision C **Page**

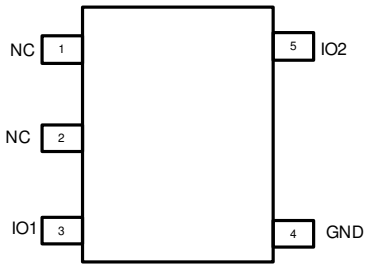
- Added DCK Package to the Pin Configuration and Functions section ... 3
- Added DCK Package to the Electrical Characteristics table ... 4

Changes from Revision A (June 2013) to Revision B **Page**

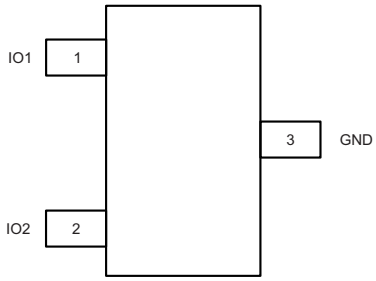
- Added ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section. ... 1

5 Pin Configuration and Functions

DRL Package
5-Pin SOT
Top View



DCK Package
3-Pin SC70
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	DRL	DCK		
IO1	3	1	I/O	The IO1 and IO2 pins are an ESD protected channel. Connect these pins to the data line as close to the connector as possible.
IO2	5	2	I/O	
NC	1, 2	—	-	This pin is not connected and is left floating, grounded, or connected to VCC.
GND	4	3	G	The GND (ground) pin is connected to ground.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
I_{PP}	Peak pulse current (tp = 8/20 μs)		5.5 (1)	A
P_{PP}	Peak pulse power (tp = 8/20 μs) DRL package		85 (1)	W
P_{PP}	Peak pulse power (tp = 8/20 μs) DCK package		75 (1)	W
	Operating temperature	–40	125	°C
	Storage temperature	–65	155	°C

(1) Measured at 25°C.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1500	
		EC 61000-4-2 contact	±25000	
		EC 61000-4-2 air-gap	±30000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IO}	Input Pin Voltage	0		5.5	V
T_A	Operating Free Air Temperature	-40		125	°C

6.4 Thermal Information

THERMAL METRIC (1)		TPD2E2U06		UNIT
		DRL	DCK	
		5 PINS	3 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	286.8	308.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	130.7	170.7	
$R_{\theta JB}$	Junction-to-board thermal resistance	104.8	89.2	
ψ_{JT}	Junction-to-top characterization parameter	25.6	34.2	
ψ_{JB}	Junction-to-board characterization parameter	104.3	88.6	

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage	I_{IO} < 10 µA			5.5	V
V_{CLAMP}	IO to GND	I_{PP} = 1 A, TLP (1)		9.7		V
		I_{PP} = 5 A, TLP (1)		12.4		
V_{CLAMP}	GND to IO	I_{PP} = 1 A, TLP (1)		1.9		V
		I_{PP} = 5 A, TLP (1)		4		
R_{DYN}	Dynamic resistance DRL package	IO to GND (2)		0.5		Ω
R_{DYN}	Dynamic resistance DRL package	GND to IO (2)		0.25		Ω
R_{DYN}	Dynamic resistance DCK package	IO to GND (2)		0.6		Ω
R_{DYN}	Dynamic resistance DCK package	GND to IO (2)		0.4		Ω
CL	Line capacitance	f = 1 MHz, V_{BIAS} = 2.5 V (3)		1.5	1.9	pF
C_{CROSS}	Channel-to-channel input capacitance	Pin 4 = 0 V, f = 1 MHz, V_{BIAS} = 2.5 V, between channel pins (3)		0.02	0.03	pF

(1) Transmission Line Pulse with 10-ns rise time, 100-ns width.
(2) Extraction of R_{DYN} Using least squares fit of TLP characteristics between I = 20 A and I = 30 A.
(3) Measured at 25°C.

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\Delta_{CIO-TO-GND}$	Variation of channel input capacitance	Pin 4 = 0 V, f = 1 MHz, V_{BIAS} = 2.5 V, channel_x pin to GND – channel_y pin to GND(3)		0.03	0.1	pF
V_{BR}	Break-down voltage	I_{IO} = 1 mA	6.5		8.5	V
I_{LEAK}	Leakage current	V_{IO} = 2.5 V		1	10	nA

6.6 Typical Characteristics

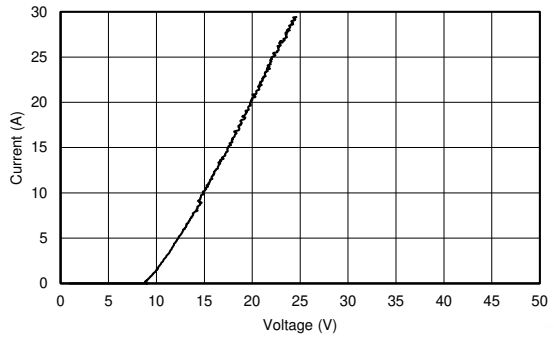


Figure 1. TLP, Data to GND

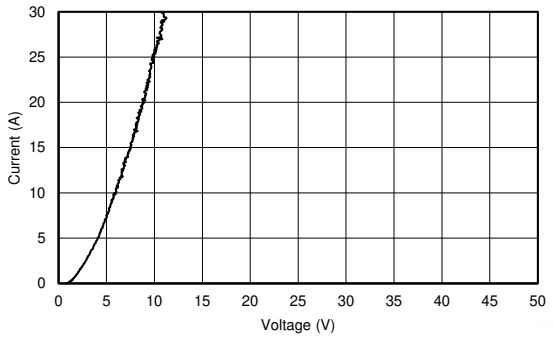


Figure 2. TLP, GND to Data

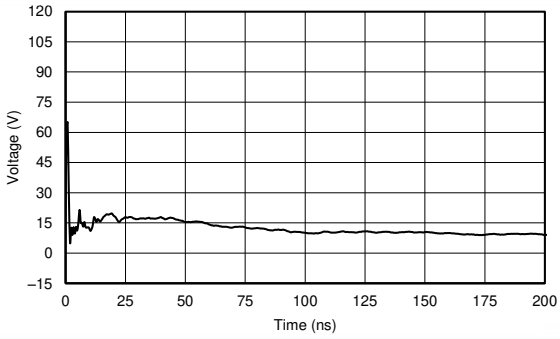


Figure 3. IEC 61000-4-2 Clamping Voltage, +8 kV Contact

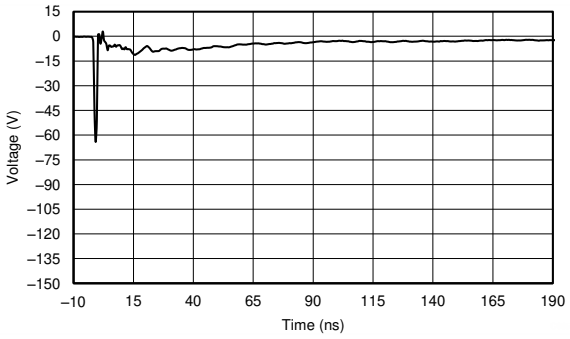
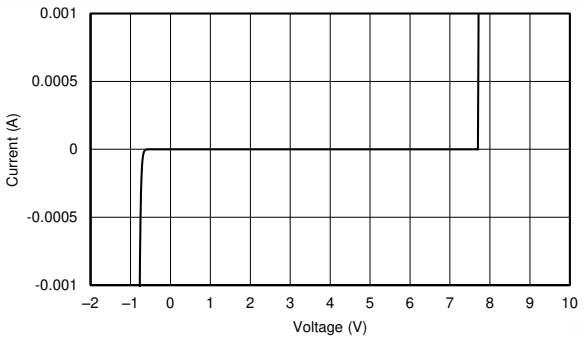
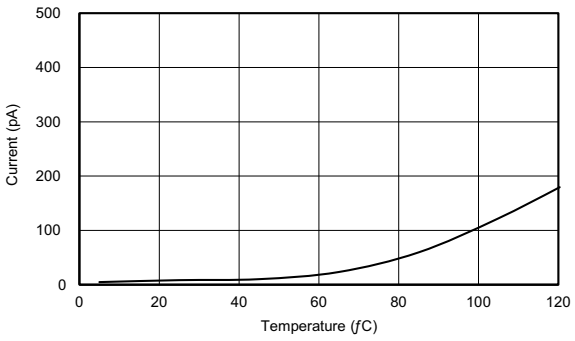


Figure 4. IEC 61000-4-2 Clamping Voltage, –8 kV Contact



T_A = 25°C

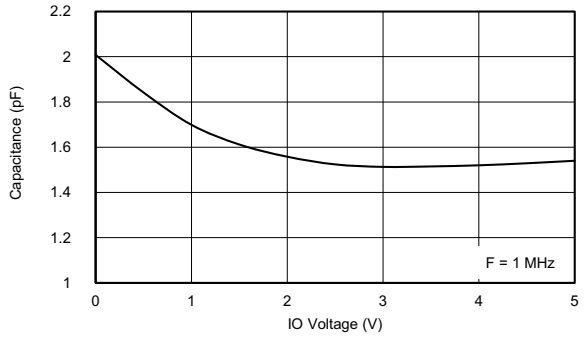
Figure 5. IV Curve



V_{IN} 2.5 V

Figure 6. I_{LEAK} vs Temperature

Typical Characteristics (continued)



f = 1 MHz

Figure 7. Capacitance Across V_{BIAS}

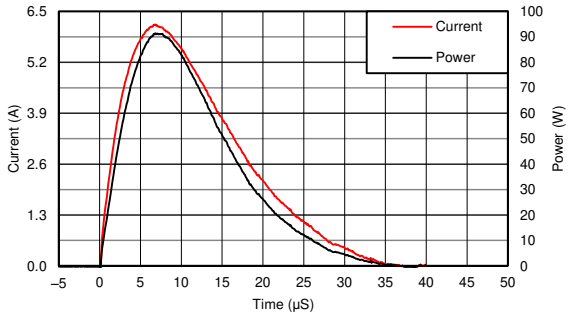


Figure 8. Surge Curve (tp = 8/20 µs) IO to GND

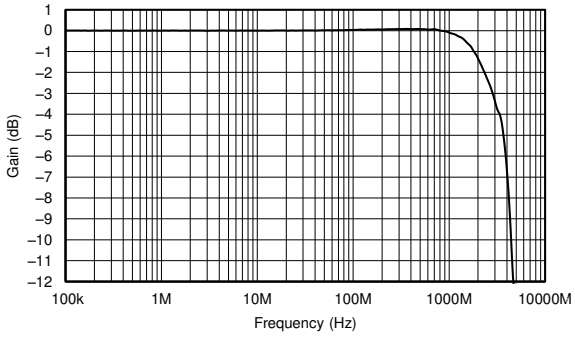


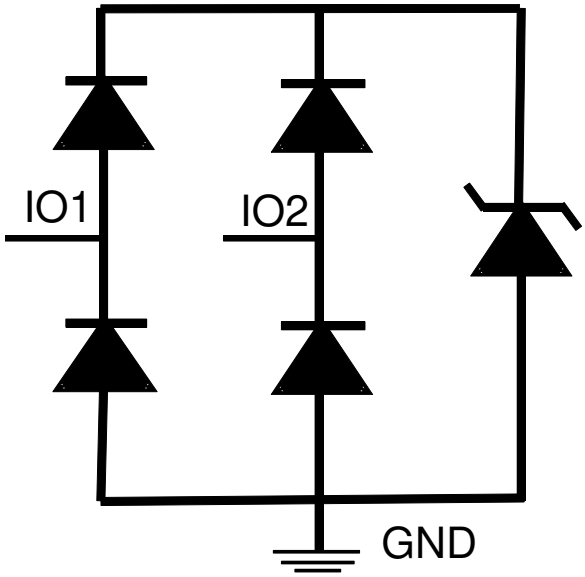
Figure 9. Insertion Loss

7 Detailed Description

7.1 Overview

The TPD2E2U06 is a dual-channel low capacitance TVS diode ESD protection device. The device offers ±25-kV contact and ±30-kV air-gap ESD protection in accordance with the IEC 61000-4-2 standard. The 1.5-pF line capacitance of the TPD2E2U06 makes the device suitable for a wide range of applications. Typical application interfaces are USB 2.0, LVDS, and I2C.

7.2 Functional Block Diagram



7.3 Feature Description

The TPD2E2U06 is a dual-channel low capacitance TVS diode ESD protection device. The device offers ±25-kV contact and ±30-kV air-gap ESD protection in accordance with the IEC 61000-4-2 standard. The 1.5-pF line capacitance of the TPD2E2U06 makes the device suitable for a wide range of applications. Typical application interfaces are USB 2.0, LVDS, and I2C.

7.3.1 IEC 61000-4-2 Level 4

The I/O pins can withstand ESD events up to ±25-kV contact and ±30-kV air. An ESD/surge clamp diverts the current to ground.

7.3.2 IO Capacitance

The capacitance between each I/O pin to ground is 1.5 pF. These capacitances support data rates in excess of 1.5 Gbps.

7.3.3 DC Breakdown Voltage

The DC breakdown voltage of each I/O pin is a minimum of 6.5 V. This ensures that sensitive equipment is protected from surges above the reverse standoff voltage of 5.5 V.

7.3.4 Ultra-Low Leakage Current

The I/O pins feature an ultra-low leakage current of 10 nA (Max) with a bias of 2.5 V.

7.3.5 Low ESD Clamping Voltage

The I/O pins feature an ESD clamp that is capable of clamping the voltage to 9.7 V (I_{PP} = 1 A).

Feature Description (continued)

7.3.6 Industrial Temperature Range

This device is designed to operate from –40°C to 125°C.

7.3.7 Small Easy-to-Route Package

The layout of this device makes it simple and easy to add protection to an existing layout. The packages offers flow-through routing, requiring minimal modification to an existing layout.

7.4 Device Functional Modes

TPD2E2U06 is a passive integrated circuit that triggers when voltages are above V_{BR} or below the lower diodes V_f (–0.6 V). During ESD events, voltages as high as ±30 kV (air) can be directed to ground via the internal diode network. Once the voltages on the protected line fall below the trigger levels of TPD2E2U06 (usually within 10's of nano-seconds) the device reverts to passive.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

TPD2E2U06 is a diode type TVS which is typically used to provide a path to ground for dissipating ESD events on hi-speed signal lines between a human interface connector and a system. As the current from ESD passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low R_{DYN} of the triggered TVS holds this voltage, V_{CLAMP}, to a safe level for the protected IC.

8.2 Typical Application

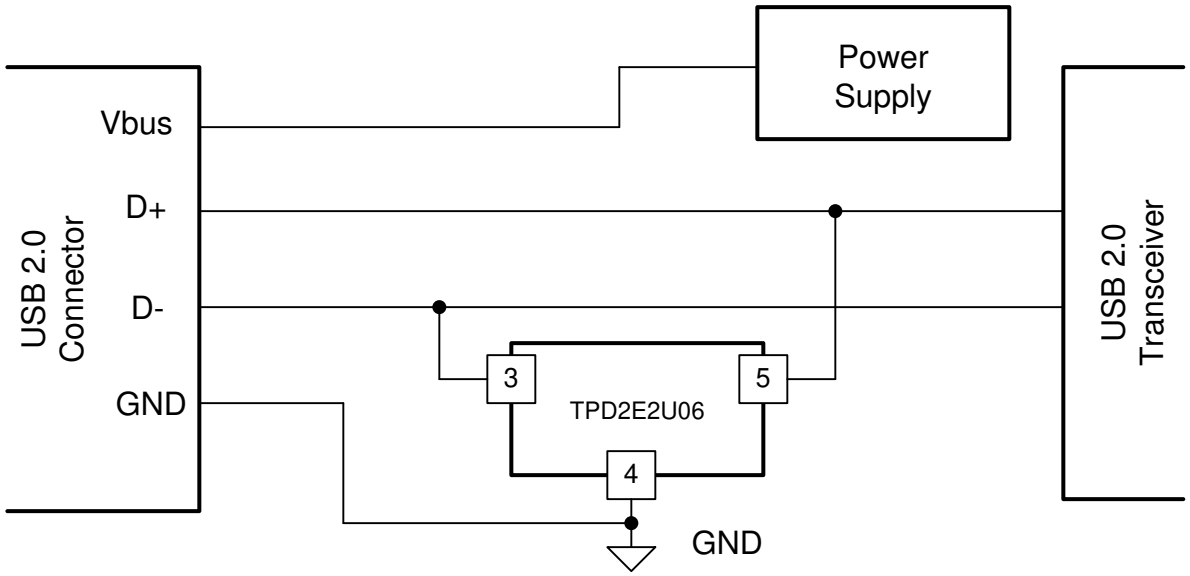


Figure 10. Typical USB Application Diagram

8.2.1 Design Requirements

For this design example, one TPD2E2U06 device will be used in a USB 2.0 application. This will provide complete port protection.

Given the USB 2.0 application, the following parameters are known.

DESIGN PARAMETER	VALUE
Signal range on Pins 3 or 5	0 V to 3.3 V
Operating Frequency	240 MHz

8.2.2 Detailed Design Procedure

To begin the design process, some parameters must be decided upon; the designer needs to know the following:

- Signal range of all the protected lines
- Operating frequency

8.2.2.1 Signal Range

The TPD2E2U06 has 2 identical protection channels for signal lines. The symmetry of the device provides flexibility when selecting which of the 2 I/O channels will protect which signal lines. Any I/O will support a signal range of 0 to 5.5 V.

8.2.2.2 Operating Frequency

The TPD2E2U06 has a capacitance of 1.5 pF (Typ), supporting USB 2.0 data rates.

8.2.3 Application Curves

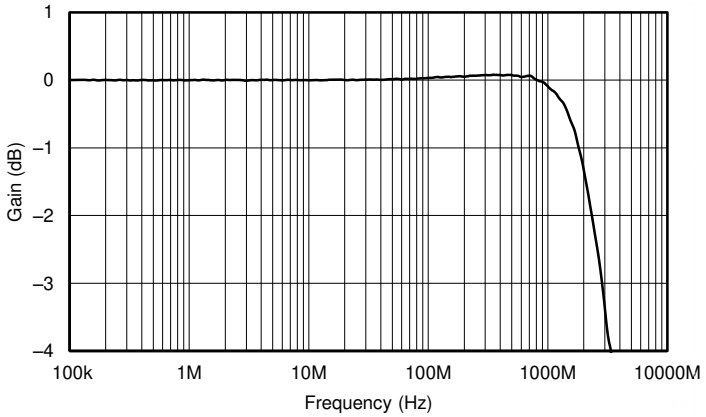


Figure 11. Insertion Loss Graph

9 Power Supply Recommendations

This device is a passive ESD protection device and there is no need to power it. Care should be taken to make sure that the maximum voltage specifications for each line are not violated.

10 Layout

10.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer needs to minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.

10.2 Layout Example

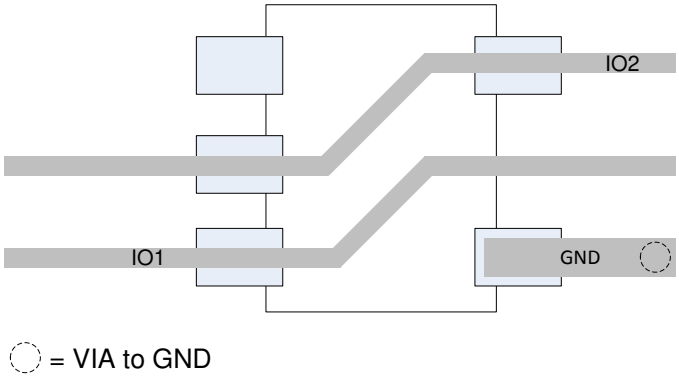


Figure 12. Routing with DRL Package

11 Device and Documentation Support

11.1 Trademarks

E2E is a trademark of Texas Instruments.
I^2C is a trademark of NXP Semiconductors.
All other trademarks are the property of their respective owners.

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPD2E2U06DCKR	ACTIVE	SC70	DCK	3	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	1GH	Samples
TPD2E2U06DRLR	ACTIVE	SOT-5X3	DRL	5	4000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DT	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TPD2E2U06 :

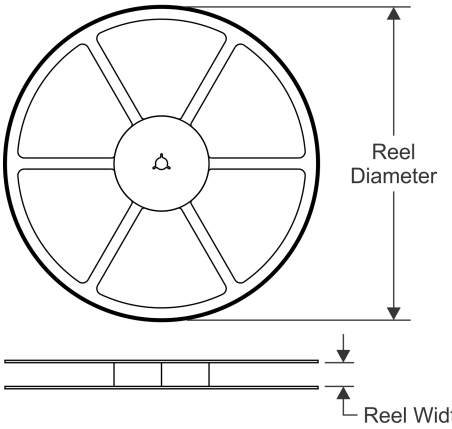
- Automotive : TPD2E2U06-Q1

NOTE: Qualified Version Definitions:

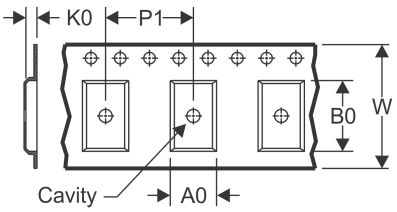
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

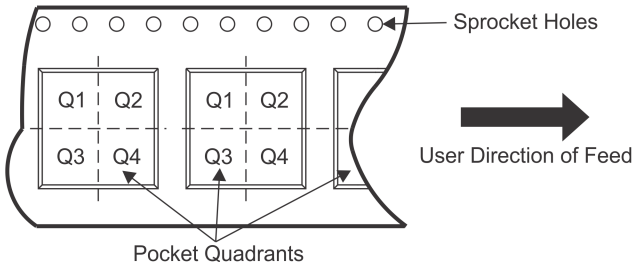


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

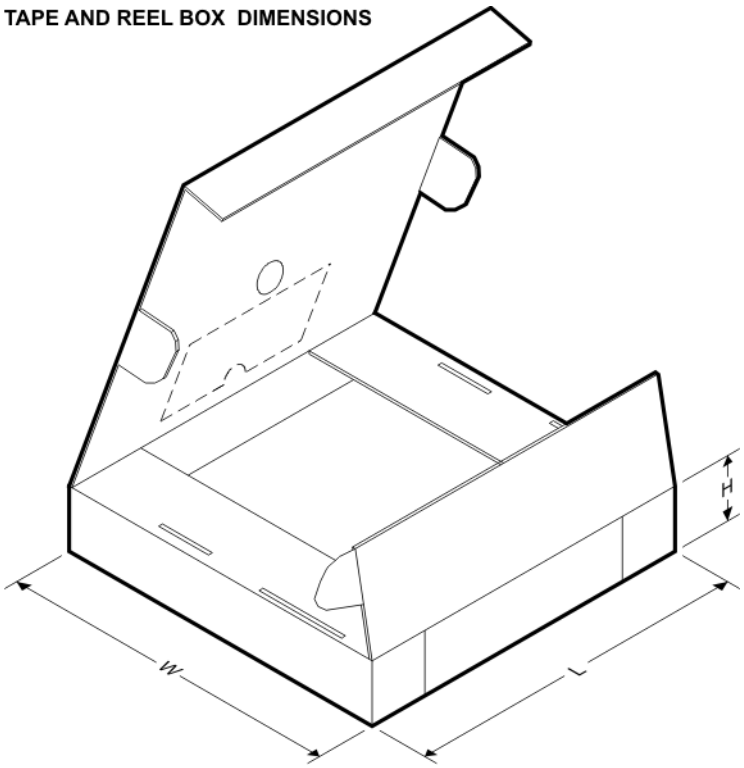
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD2E2U06DCKR	SC70	DCK	3	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TPD2E2U06DRLR	SOT-5X3	DRL	5	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

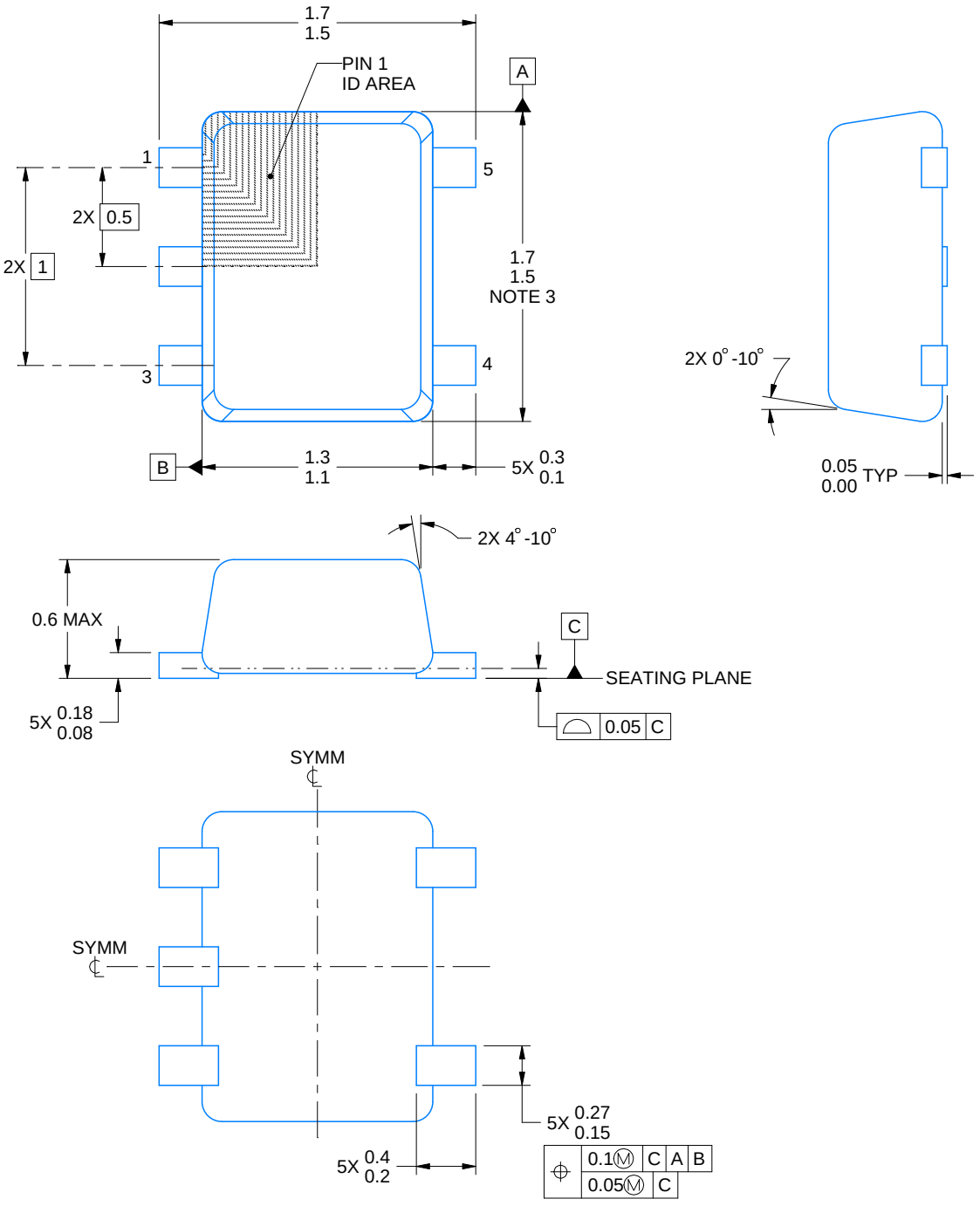
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD2E2U06DCKR	SC70	DCK	3	3000	180.0	180.0	18.0
TPD2E2U06DRLR	SOT-5X3	DRL	5	4000	183.0	183.0	20.0

PACKAGE OUTLINE

DRL0005A

SOT - 0.6 mm max height

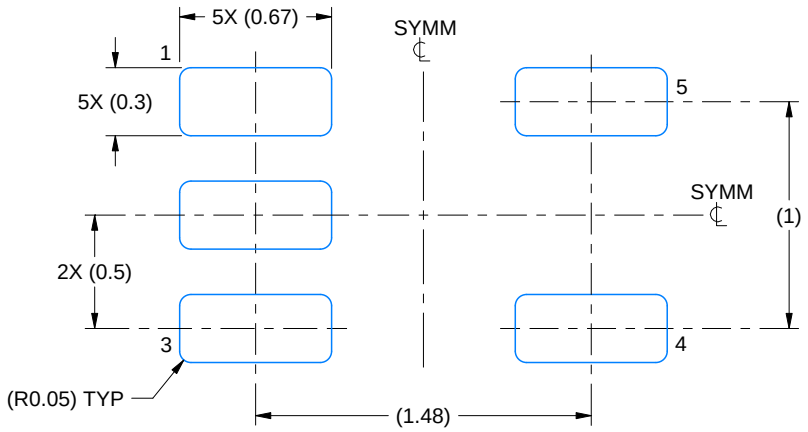
PLASTIC SMALL OUTLINE



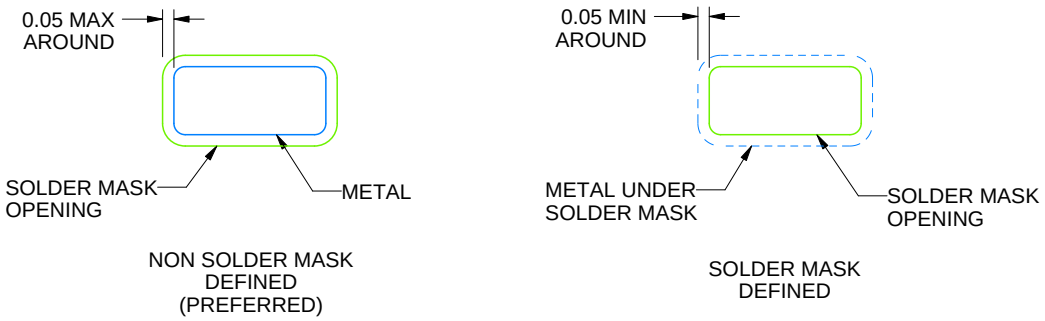
4220753/D 07/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD-1



LAND PATTERN EXAMPLE
SCALE:30X

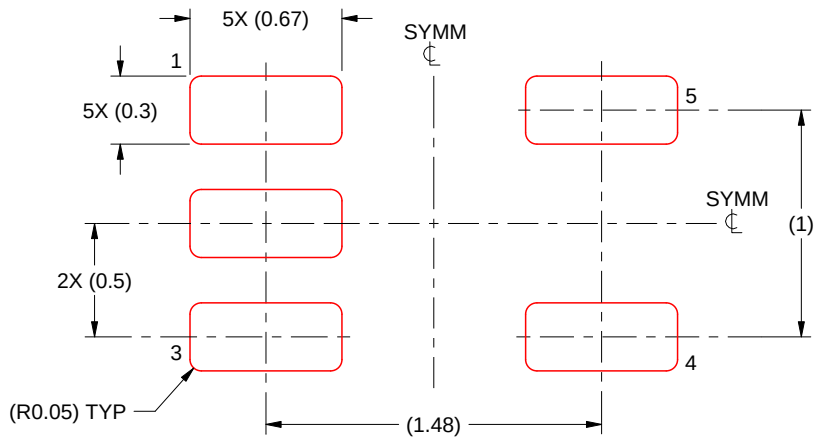


SOLDERMASK DETAILS

4220753/D 07/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4220753/D 07/2024

NOTES: (continued)

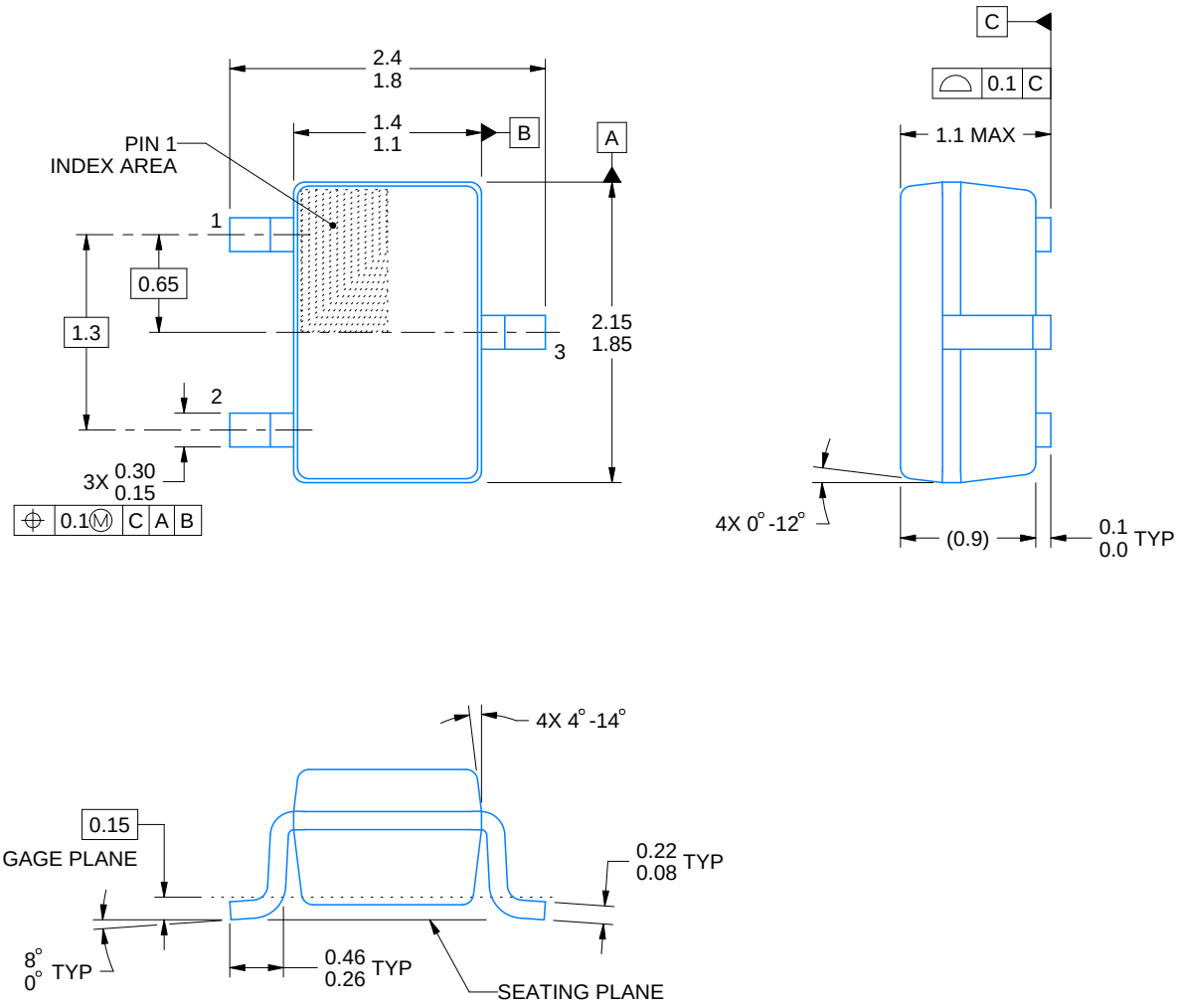
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DCK0003A

SOT-SC70 - 1.1 max height

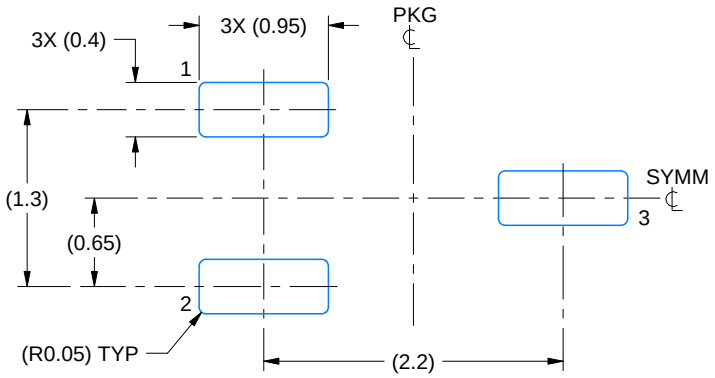
SMALL OUTLINE TRANSISTOR SC70



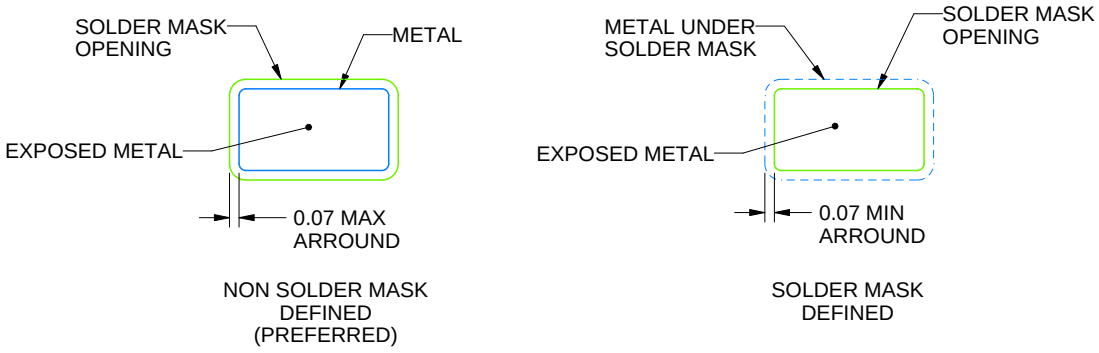
4220745/E 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

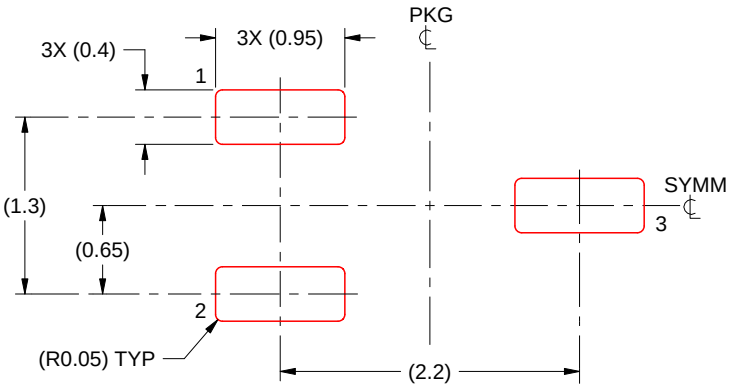


SOLDER MASK DETAILS

4220745/E 08/2024

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4220745/E 08/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265