Compact LCD Bias IC with LDO, VCOM Buffer and Reset Function

FEATURES

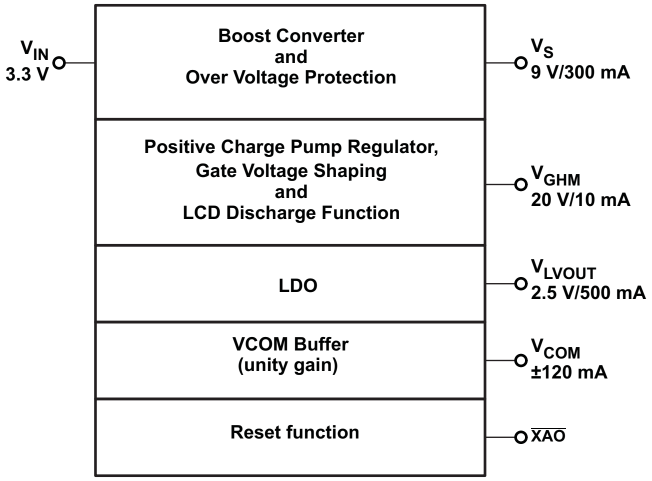
- **2.5V to 6.0V Input Voltage Range**
- **Up to 16.5V Boost Converter With 2A Switch Current**
- **650kHz/1.2MHz Selectable Switching Frequency**
- **Adjustable Soft-Start for the Boost Converter**
- **500mA LDO**
- **Reset Function ($\overline{\text{XAO}}$ Signal)**
- **Regulated VGH**
- **Gate Voltage Shaping**
- **VCOM Buffer**
- **LCD Discharge Function**
- **Overvoltage Protection**
- **Thermal Shutdown**
- **Undervoltage Lockout**
- **24-Pin 4×4mm QFN Package**

APPLICATIONS

- **Notebook PC**
- **Monitor**

DESCRIPTION

The TPS65146 offers a very compact power supply solution designed to supply the LCD bias voltages required by TFT (Thin Film Transistor) LCD panels running from a typical 3.3 V or 5 V supply rail. The device integrates a step-up converter for V_S (Source Driver voltage), a positive charge pump regulator for V_{GH} (Gate Driver High voltage), a logic voltage rail using an integrated LDO and a VCOM buffer driving the LCD backplane. In addition to that, a gate voltage shaping block is integrated for V_{GH}, modulating the signal (into V_{GHM}) with high flexibility by using a logic input VFLK and an external discharge resistor connected to RE pin. Also, an external discrete negative charge pump can be set using the boost converter of the TPS65146 to generate V_{GL} (Gate Driver Low voltage). The integrated reset function together with the LCD discharge function available in the TPS65146 provide the signals enabling the discharge of the LCD TFT pixels when powering-off. The device includes safety features like overvoltage protection (OVP), as well as thermal shutdown.


VIN 3.3 V
Boost Converter and Over Voltage Protection
Positive Charge Pump Regulator, Gate Voltage Shaping and LCD Discharge Function
LDO
VCOM Buffer (unity gain)
Reset function
VS 9 V/300 mA
VGHM 20 V/10 mA
VLVOUT 2.5 V/500 mA
VCOM ±120 mA
XAO

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION(1)

T_A	ORDERING	PACKAGE	PACKAGE MARKING
–40°C to 85°C	TPS65146RGER	24-pin QFN	CEZ

(1) The RGE package is available taped an reeled. For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

	VALUE	UNIT
Input voltage range VIN, LVIN (2)	–0.3 to 6.5	V
Voltage range on pins FB, SS, FREQ, COMP, ADJ, LVOUT, $\overline{\text{XAO}}$, FBP, VDPM, VFLK, VDET, CDET (2)	–0.3 to 6.5	V
Voltage on pin SW, OPI, OPO, SUP, DRVP (2)	-0.3 to 20	V
Input voltage on VGH, VGHM, RE (2)	-0.3 to 35	V
ESD rating HBM	2	kV
ESD rating MM	200	V
ESD rating CDM	500	V
Continuous power dissipation	See Dissipation Rating Table	
Storage temperature range	–65 to 150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

DISSIPATION RATINGS(1)(2)

PACKAGE	$R_{\theta JA}$	T_A ≤25°C POWER RATING	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
QFN	30°C/W	3.3 W	1.8 W	1.3 W

(1) $P_D = (T_J - T_A)/R_{\theta JA.}$
(2) $R_{\theta JA.}$ given for High-K PCB board.

RECOMMENDED OPERATING CONDITIONS(1)(2)

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
V_{IN}, V_{LVIN}	Input voltage range, with $V_{LVIN} \le V_{IN}$	2.5		6.0	V
T_A	Operating ambient temperature	–40		85	°C
T_J	Operating junction temperature	–40		125	°C

(1) Maximum output voltage limited by the Overvoltage Protection and not the maximum Power Switch rating.
(2) Refer to application section for further information

ELECTRICAL CHARACTERISTICS

V_{IN} = V_{LVIN} = 3.3 V, V_S = V_{SUP} = 9 V, V_{LVOUT} = 2.5 V, V_{GH} = 20 V, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
V_{IN}	Input voltage range		2.5		6.0	V
I_{QIN}	Operating quiescent current into VIN	Device not switching, V_{FB} = 1.240 V + 3%		0.17	0.5	mA
I_{QLVIN}	Operating quiescent current into LVIN	V_{ADJ} = 1.240 V, V_{LVOUT} = open, no load		25	45	µA
I_{QVGH}	Operating quiescent current into VGH	VFLK = GND		22	40	µA
I_{QSUP}	Operating quiescent current into SUP	Device not switching, V_{FB} = 1.240 V + 3%		1.8		mA
I_{SDVIN}	Shutdown current into VIN	V_{IN} = 1.8 V, V_S = GND		20	33	µA
I_{SDVGH}	Shutdown current into VGH	V_{IN} = 1.8 V, V_{GH} = 32 V		30	50	µA
I_{SDLVIN}	Shutdown current into LVIN	V_{IN} = 1.8 V, V_{LVOUT} = open		0.1	2	µA
I_{SDSUP}	Shutdown current into SUP	V_{IN} = 1.8 V, V_{SUP} = 16.5 V		3	5	µA
V_{UVLO}	Under-voltage lockout threshold	V_{IN} falling	2.0		2.2	V
		V_{IN} rising			2.3	
T_{SD}	Thermal shutdown	Temperature rising		150		°C
T_{SDHYS}	Thermal shutdown hysteresis			14		°C
LOGIC SIGNALS FREQ, VFLK						
I_{LEAK}	Input leakage current	VFLK = 6.0 V, FREQ = GND			0.1	µA
V_{IH}	Logic high input voltage	V_{IN} = 2.5 V to 6 V	2			V
V_{IL}	Logic low input voltage	V_{IN} = 2.5 V to 6 V			0.5	V
BOOST CONVERTER						
V_S	Output voltage boost converter(1)		7		16.5	V
V_{OVP}	Overvoltage protection	V_S rising	16.9	18	19	V
V_{FB}	Feedback regulation voltage	T_A = -40°C to 85°C	1.226	1.240	1.254	V
		T_A = 25°C	1.230	1.240	1.250	
I_{FB}	Feedback input bias current	V_{FB} = 1.240V			0.1	µA
gm	Transconductiance error amplifier gain			115		µA/V
$R_{DS(ON)}$	N-channel MOSFET on-resistance	V_{IN} = V_{GS} = 5 V, I_{SW} = current limit		0.13	0.38	Ω
		V_{IN} = V_{GS} = 3.3 V, I_{SW} = current limit		0.15	0.44	
I_{LEAK_SW}	SW leakage current	V_{IN} = 1.8 V, V_{SW} = 17 V			30	µA
I_{LIM}	N-Channel MOSFET current limit		2.0	2.5	3.0	A
I_{SS}	Softstart current	V_{SS} = 1.240 V		4		µA
f_{osc}	Switching frequency	FREQ = high	0.9	1.2	1.5	MHz
		FREQ = low	470	625	780	kHZ
I_{FREQ}	FREQ sink current	FREQ = 3.3 V		4		µA
	Line regulation	V_{IN} = 2.5 V to 6.0 V, I_{OUT} = 10 mA		0.008		%/V
	Load regulation	I_{OUT} = 0 A to 500 mA, V_{IN} = 3.3 V		0.15		%/A
LDO REGULATOR						
V_{LVOUT}	LDO output voltage range		1.240		4	V
V_{ADJ}	Feedback regulation voltage	I_{LVOUT} = 2mA, V_{LVOUT} = 1.240 V, T_A = -40°C to 85°C	1.222	1.240	1.258	V
		I_{LVOUT} = 2mA, V_{LVOUT} = 1.240 V, T_A = 25°C	1.225	1.240	1.255	
I_{ADJ}	Feedback input bias current	V_{ADJ} = 1.240 V			0.1	µA
I_{SC_LDO}	Short circuit current limit	V_{IN} = V_{LVIN} = 6 V, LVOUT = GND, ADJ = GND			750	mA
V_{DO}	Dropout voltage	I_{LVOUT} = 350 mA, V_{LVIN} = V_{LVOUT} – 0.1V		280	410	mV
		I_{LVOUT} = 500 mA, V_{LVIN} = V_{LVOUT} – 0.1V		430	620	
	Line regulation	V_{LVIN} = 2.7 V to 5.5 V, I_{LVOUT} = 100 mA		0.005		%/V
	Load regulation	I_{LVOUT} = 1 mA to 300 mA		0.6		%/A

(1) Maximum output voltage limited by the Overvoltage Protection and not the maximum power switch rating of the boost converter.

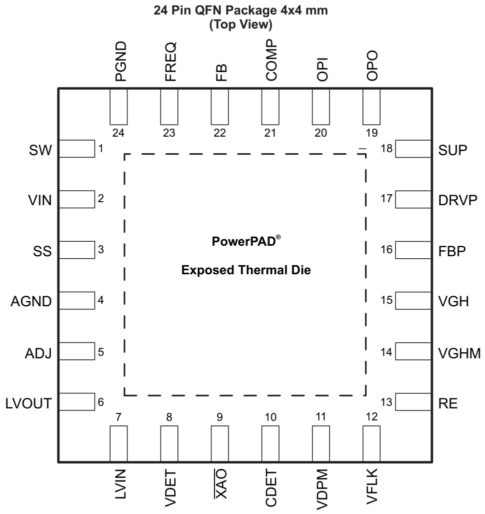
ELECTRICAL CHARACTERISTICS (continued)

$V_{IN} = V_{LVIN} = 3.3$ V, $V_S = V_{SUP} = 9$ V, $V_{LVOUT} = 2.5$ V, $V_{GH} = 20$ V, $T_A = –40°C$ to 85°C, typical values are at $T_A = 25°C$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VGH REGULATOR						
f_{SW}	Switching frequency		0.5 × f_{OSC}			MHz
V_{FBP}	Reference voltage of feedback	T_A = -40°C to 85°C	1.210	1.240	1.270	V
		T_A = 25°C	1.221	1.240	1.259	
I_{FBP}	Feedback input bias current	V_{FBP}= 1.240 V			0.1	µA
$R_{DS(ON)Q1}$	DRVP $R_{DS(ON)}$ (Q1 PMOS)	V_S = 9 V, I_{DRVP} = 40 mA		8	20	Ω
$R_{DS(ON)Q2}$	DRVP $R_{DS(ON)}$ (Q2 NMOS)	V_S = 9 V, I_{DRVP} = - 40 mA		2	6	Ω
GATE VOLTAGE SHAPING VGHM						
I_{DPM}	Capacitor charge current VDPM pin			20		µA
$R_{DS(ON)M1}$	VGH to VGHM $R_{DS(ON)}$ (M1 PMOS)	VFLK = low, I_{VGHM} = 20 mA, V_{GH} = 20 V		13	25	Ω
$R_{DS(ON)M2}$	VGHM to RE $R_{DS(ON)}$ (M2 PMOS)	VFLK = high, I_{VGHM} = 20 mA, V_{GHM} = 7.5 V		13	25	Ω
RESET FUNCTION						
V_{IN_DET}	Operating voltage for V_{IN}		1.6		6.0	V
V_{DET}	Threshold voltage	Falling, T_A = -40°C to 85°C	1.074	1.100	1.126	V
		Falling, T_A = 25°C	1.079	1.100	1.121	
V_{DET_HYS}	Threshold hysterisis			65		mV
I_{DET_B}	Iinput bias current	V_{DET} = 1.1 V			0.1	µA
I_{CDET}	Delay capacitor charge current	V_{CDET} ≤ 1.240 V		10		µA
$I_{\overline{XAO}(ON)}$	Sink current capability[2]	$V_{\overline{XAO}(ON)}$ = 0.5 V	1			mA
$V_{\overline{XAO}(ON)}$	Low voltage level	$I_{\overline{XAO}(ON)}$= 1 mA			0.5	V
$I_{LEAK\_\overline{XAO}}$	Leakage current	$V_{\overline{XAO}}$ = V_{IN} = 3.3V			2	µA
VCOM BUFFER						
V_{SUP}	V_S supply range[3]		7		16.5	V
V_{OFFSET}	Input offset voltage	$V_{CM} = V_{OPI} = V_{SUP}/2 = 4.5$ V	–15		15	mV
I_B	Input bias current	$V_{CM} = V_{OPI} = V_{SUP}/2 = 4.5$ V	-1		1	µA
V_{CM}	Common mode input voltage range	V_{OFFSET} = 10 mV, I_{OPO} = 10 mA	2		V_S-2	V
CMRR	Common mode rejection ratio	$V_{CM} = V_{OPI} = V_{SUP}/2 = 4.5$ V, 1 MHz		66		dB
V_{OL}	Output voltage swing low	I_{OPO} = 10 mA		0.10	0.20	V
V_{OH}	Output voltage swing high	I_{OPO} = 10 mA	V_S - 0.80	V_S - 0.65		V
I_{sc}	Short circuit current	Source ($V_{OPI} = V_{SUP}/2 = 4.5$ V, OPO = GND)	90	135		mA
		Sink ($V_{OPI} = V_{SUP}/2 = 4.5$ V, $V_{COM} = V_{SUP} = 9$ V)	100	160		
I_o	Output current	Source ($V_{OPI} = V_{SUP}/2 = 4.5$V, V_{OFFSET} = 15 mV)		120		mA
		Sink ($V_{OPI} = V_{SUP}/2 = 4.5$V, V_{OFFSET} = 15 mV)		130		
PSRR	Power supply rejection ratio			40		dB
SR	Slew rate	A_V = 1, V_{OPI} = 2 Vpp		40		V/µs
BW	–3db bandwidth	A_V = 1, V_{OPI} = 60 mVpp		60		MHz

(2) External pull-up resistor to be chosen so that the current flowing into $\overline{XAO}$ Pin ($V_{\overline{XAO}}$ = 0 V) when active is below $I_{\overline{XAO}\_MIN}$ = 1mA.
(3) Maximum output voltage limited by the Overvoltage Protection and not the maximum power switch rating of the boost converter.

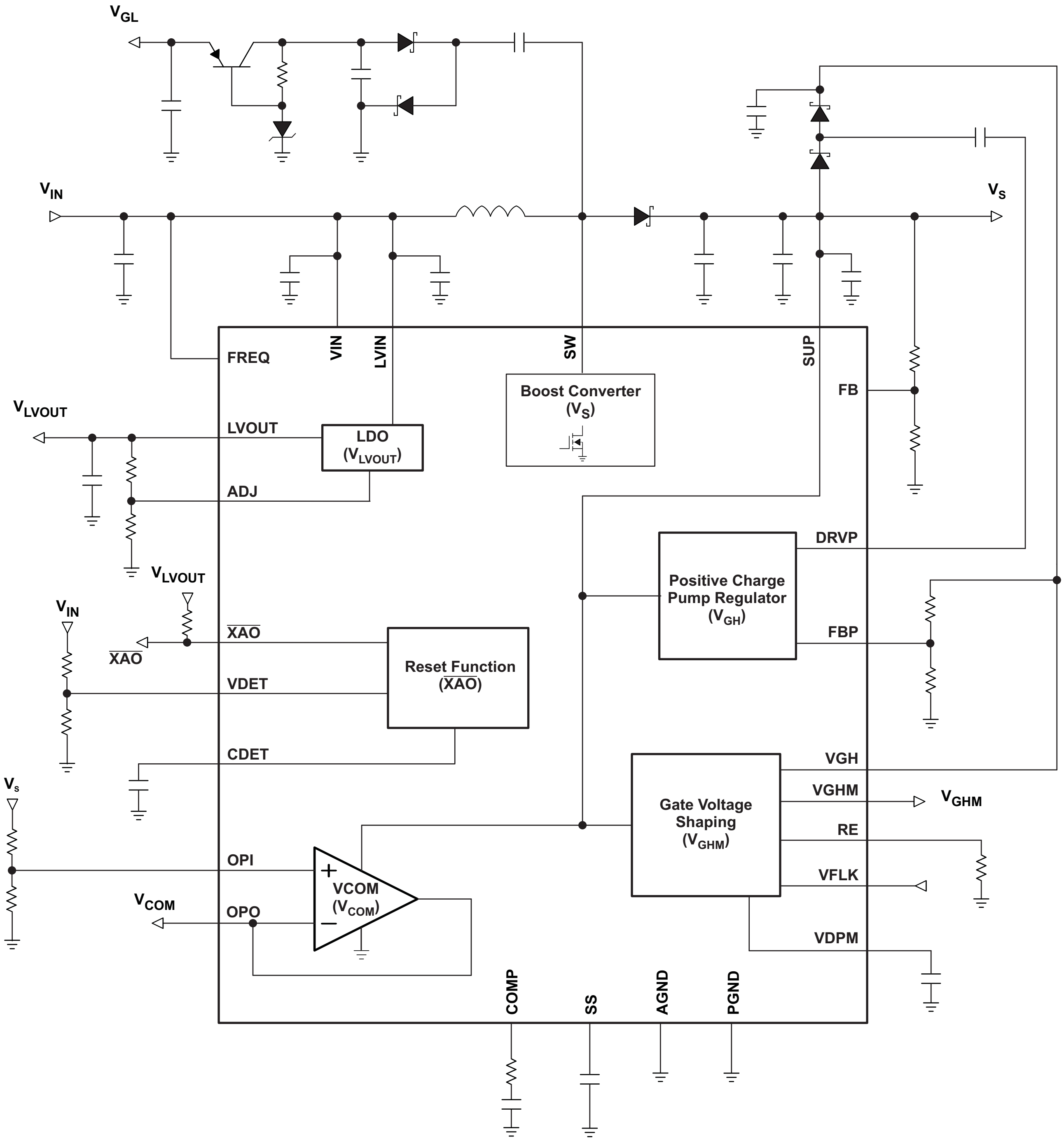
PIN ASSIGNMENT


24 Pin QFN Package 4x4 mm
(Top View)
PGND
FREQ
FB
COMP
OPI
OPO
24
23
22
21
20
19
SW
1
VIN
2
SS
3
AGND
4
ADJ
5
LVOUT
6
18
SUP
17
DRVP
16
FBP
15
VGH
14
VGHM
13
RE
PowerPAD®
Exposed Thermal Die
7
8
9
10
11
12
LVIN
VDET
$\overline{XAO}$
CDET
VDPM
VFLK

TERMINAL FUNCTIONS

PIN		I/O	DESCRIPTION
NAME	NO.		
SW	1		Switch pin of the boost converter.
VIN	2	I	Input supply pin.
SS	3	I/O	Boost soft-start control pin. Connect a capacitor to this pin if a soft-start is needed. Open = no soft-start.
AGND	4, exposed pad		Analog ground.
ADJ	5	I	LDO feedback pin.
LVOUT	6	O	LDO output pin.
LVIN	7	I	LDO input supply pin.
VDET	8	I	Reset function threshold pin. Connect a voltage divider to this pin to set the threshold voltage.
$\overline{XAO}$	9	O	Reset function output pin (open-drain). $\overline{XAO}$ signal is active low.
CDET	10	I/O	Sets the reset delay time. Pin for external capacitor. Floating if no delay is needed.
VDPM	11	I/O	Sets the delay to enable VGHM Output. Pin for external capacitor. Floating if no delay needed.
VFLK	12	I	Input pin for charge/discharge signal for V_{GHM}. VFLK = “high” discharges V_{GHM} through RE pin.
RE	13		Slope adjustment pin for gate voltage shaping. Connect a resistor to this pin to set the discharging slope of V_{GHM} when VFLK = “high”.
VGHM	14	O	Gate voltage shaping output pin
VGH	15	I	Input pin for the positive charge pump voltage.
FBP	16	I	Positive charge pump feedback pin.
DRVP	17	O	Voltage driver pin of the positive charge pump.
SUP	18	I	Input supply pin for the gate voltage shaping and operational amplifier blocks. Also overvoltage protection sense pin. SUP pin must be supplied by V_S voltage.
OPO	19	O	Output pin of the VCOM Buffer.
OPI	20	I	Input pin of the VCOM Buffer.
COMP	21	I/O	Boost converter compensation pin .
FB	22	I	Boost converter feedback pin.
FREQ	23	I	Boost converter frequency select pin. Oscillator is 650 kHz when FREQ is connected to GND and 1.2 MHz when FREQ is connected to VIN.
PGND	24		Power ground.

FUNCTIONAL BLOCK DIAGRAM


V_{GL}
V_{IN}
V_S
FREQ
VIN
LVIN
SW
SUP
FB
Boost Converter
(V_S)
V_{LVOUT}
LVOUT
LDO
(V_{LVOUT})
ADJ
DRVP
Positive Charge
Pump Regulator
(V_{GH})
FBP
V_{LVOUT}
V_{IN}
$\overline{XAO}$
$\overline{XAO}$
VDET
Reset Function
($\overline{XAO}$)
CDET
VGH
V_s
VGHM
V_{GHM}
Gate Voltage
Shaping
(V_{GHM})
RE
OPI
VFLK
V_{COM}
OPO
VCOM
(V_{COM})
VDPM
COMP
SS
AGND
PGND

TYPICAL CHARACTERISTICS

TABLE OF GRAPHS

		FIGURE
Efficieny vs Load Current	V_{IN} = 3.3 V, V_S = 9 V f = 650 kHz/1.2 MHz	Figure 1
Efficiency vs Load Current	V_{IN} = 3.3 V, V_S = 12 V f = 650 kHz/1.2 MHz	Figure 2
PWM Switching Discontinuous Conduction Mode	V_{IN} = 3.3 V, V_S = 9 V/ 4 mA f = 1.2 MHz	Figure 3
PWM Switching Continuous Conduction Mode	V_{IN} = 3.3 V, V_S = 9 V/ 300 mA f = 1.2 MHz	Figure 4
Boost Frequency vs Load Current	V_{IN} = 3.3 V, V_S = 9 V f = 650 kHz/1.2 MHz	Figure 5
Boost Frequency vs Supply Voltage	V_S = 9 V/150 mA, f = 650 kHz/1.2 MHz	Figure 6
Load Transient Response Boost Converter High Frequency	V_{IN} = 3.3 V, V_S = 9 V I_{OUT} = 50 mA ~ 200 mA, f = 1.2 MHz	Figure 7
Load Transient Response Boost Converter Low Frequency	V_{IN} = 3.3 V, V_S = 9 V I_{OUT} = 50 mA ~ 200 mA, f = 650 kHz	Figure 8
Soft-start Boost Converter	V_{IN} = 3.3 V, V_S = 9 V, I_{OUT} = 300 mA	Figure 9
Overvoltage Protection Boost Converter (OVP)	V_{IN} = 3.3 V, V_S = 9 V	Figure 10
Load Transient Response LDO	V_{LVIN} = 3.3 V, V_{LVOUT} = 2.5 V I_{LVOUT} = 100 mA - 300 mA	Figure 11
Gate Voltage Shaping	V_{GH} = 20 V	Figure 12
V_{GHM} Voltage vs Load Current	V_{IN} = 3.3 V, V_S = 9 V, V_{GHM} = 19.8 V	Figure 13
V_{GL} Voltage vs Load Current	V_{IN} = 3.3 V, V_S = 9 V, V_{GL} = -6.7 V	Figure 14
Power on Sequencing $\overline{XAO}$ Signal and VGHM Delay	V_{IN} = 3.3 V, V_S = 9 V, V_{GHM} = 20 V	Figure 15
Power off Sequencing $\overline{XAO}$ Signal and VGHM Delay	V_{IN} = 3.3 V, V_S = 9 V, V_{GHM} = 20 V	Figure 16
Power on Sequencing	V_{IN} = 3.3 V, V_S = 9 V, V_{LVOUT} = 2.5 V, V_{VCOM} = 4.5V, V_{GHM} = V_{GH} = 20 V, V_{GL} = -7V	Figure 17
Power off Sequencing	V_{IN} = 3.3 V, V_S = 9 V, V_{LVOUT} = 2.5 V, V_{VCOM} = 4.5V, V_{GHM} = V_{GH} = 20 V V_{GL} = -7V	Figure 18

For all the following graphics, the inductors used for the measurements are MSS7341 (L = 5 µF) for f = 1.2 MHz, and CDRH8D28 (L = 10 µF) for f = 650 kHz.

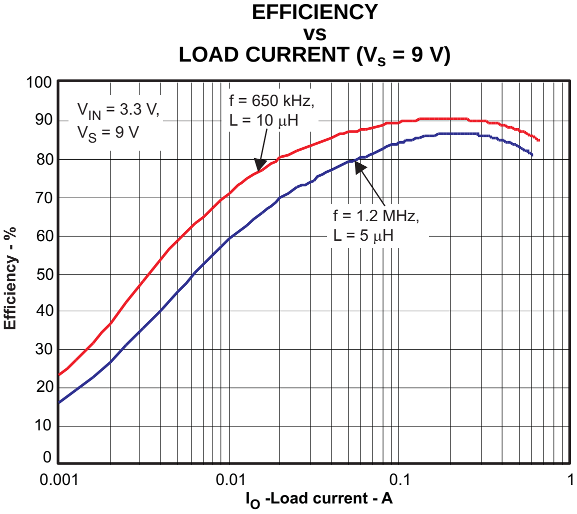


Figure 1.

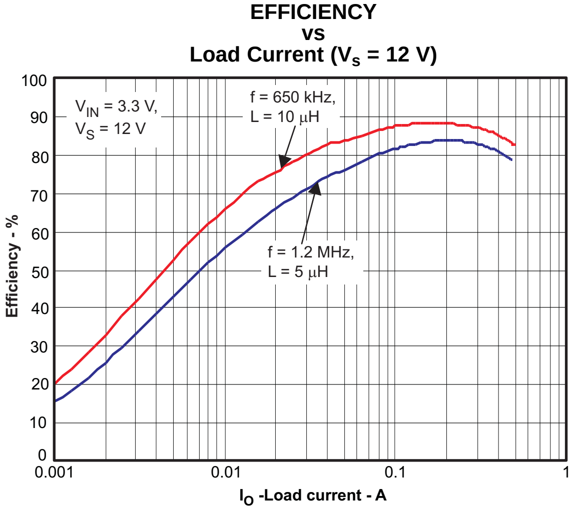


Figure 2.

PWM SWITCHING
DISCONTINUOUS CONDUCTION MODE

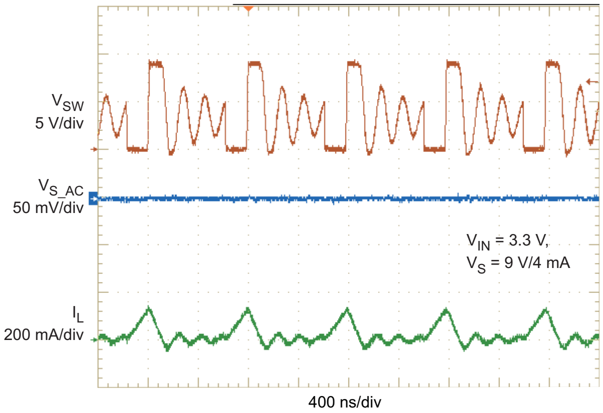


Figure 3.

PWM SWITCHING
CONTINUOUS CONDUCTION MODE

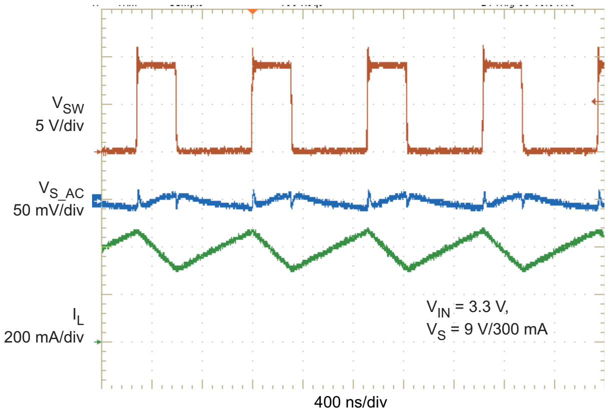


Figure 4.

BOOST FREQUENCY
vs
LOAD CURRENT

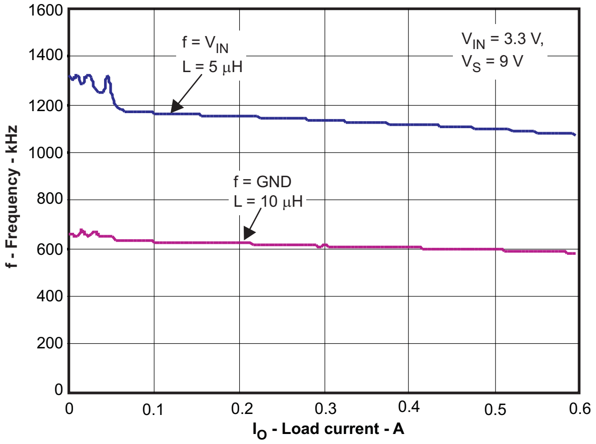


Figure 5.

BOOST FREQUENCY
vs
SUPPLY VOLTAGE

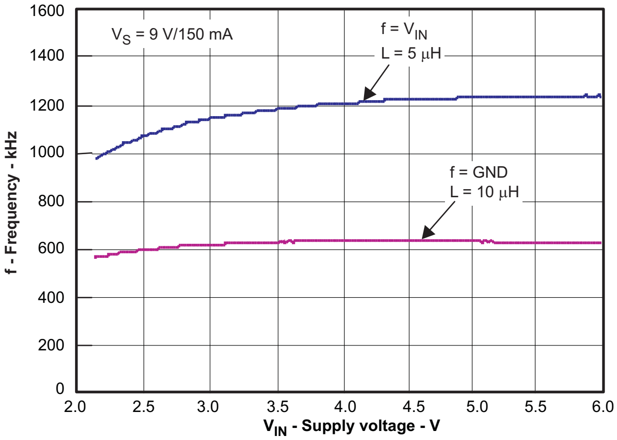


Figure 6.

LOAD TRANSIENT RESPONSE
BOOST CONVERTER HIGH FREQUENCY

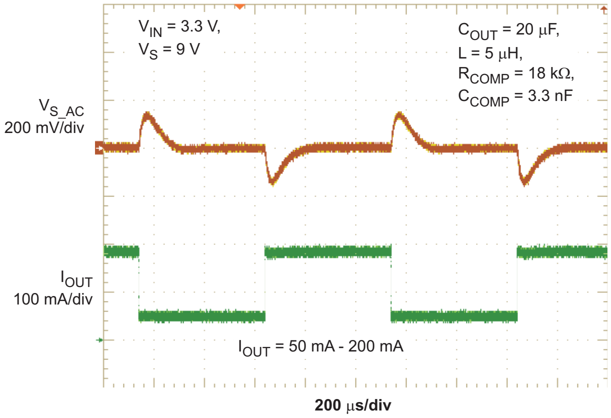


Figure 7.

LOAD TRANSIENT RESPONSE
BOOST CONVERTER LOW FREQUENCY

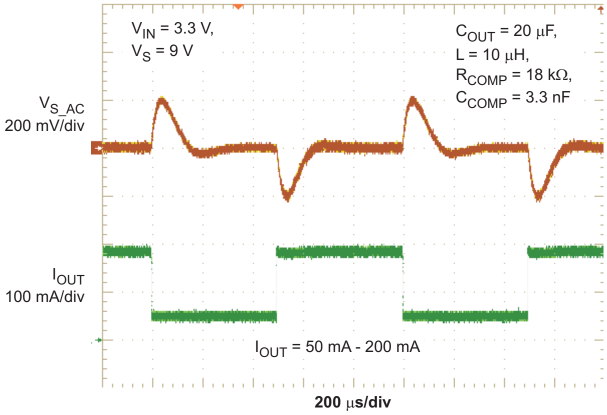


Figure 8.

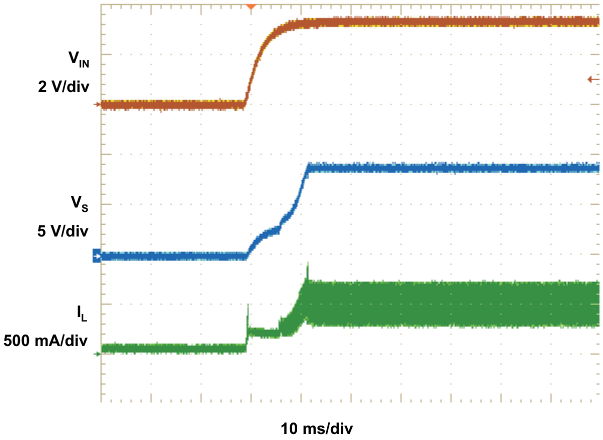

BOOST CONVERTER SOFT-START

Figure 9.

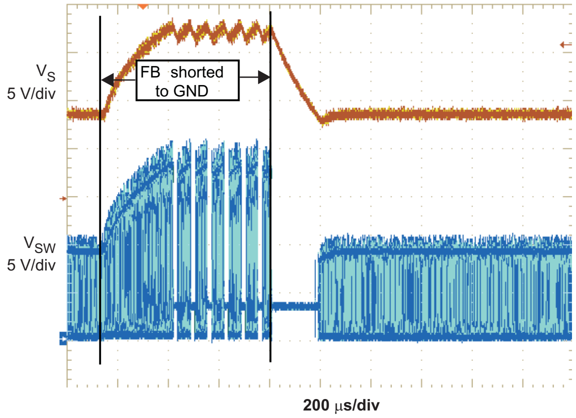

OVERVOLTAGE PROTECTION BOOST CONVERTER (OVP)

Figure 10.

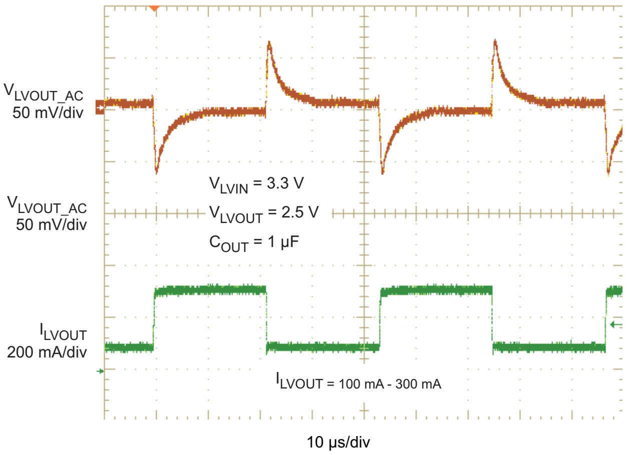

LOAD TRANSIENT RESPONSE LDO

Figure 11.

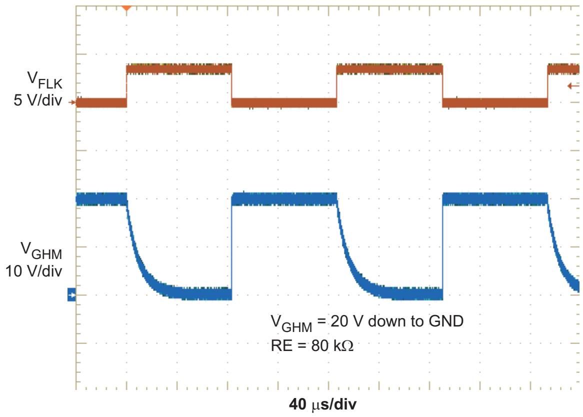

GATE VOLTAGE SHAPING

Figure 12.

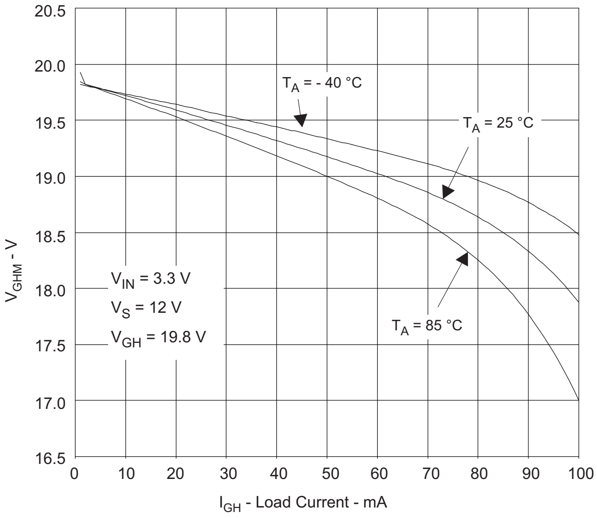

VGHM VOLTAGE vs LOAD CURRENT

Figure 13.

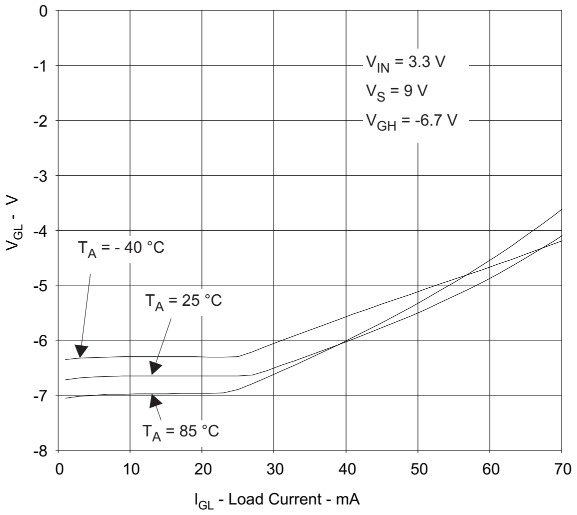

VGL VOLTAGE vs LOAD CURRENT

Figure 14.

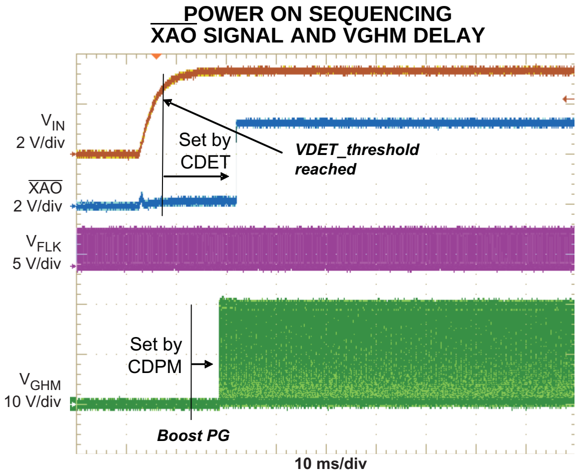


Figure 15.

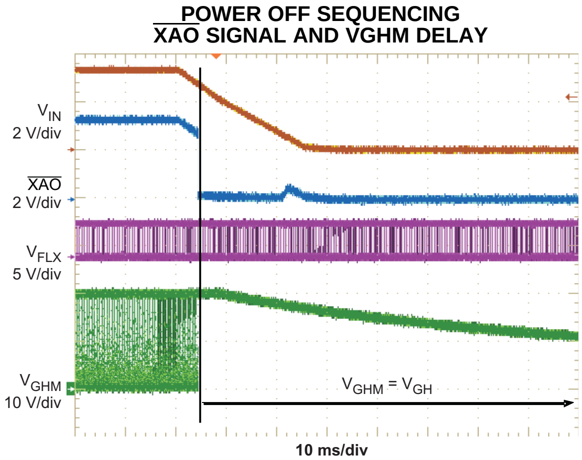


Figure 16.

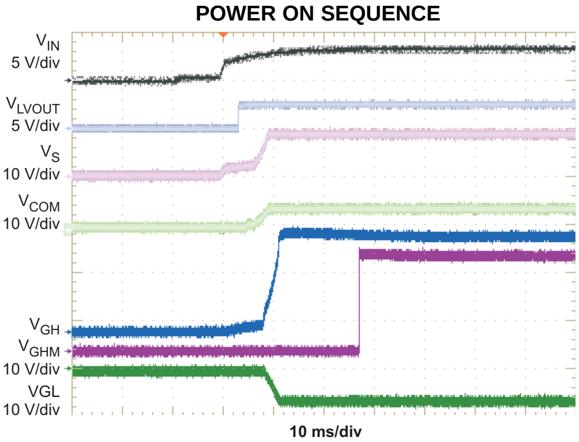


Figure 17.

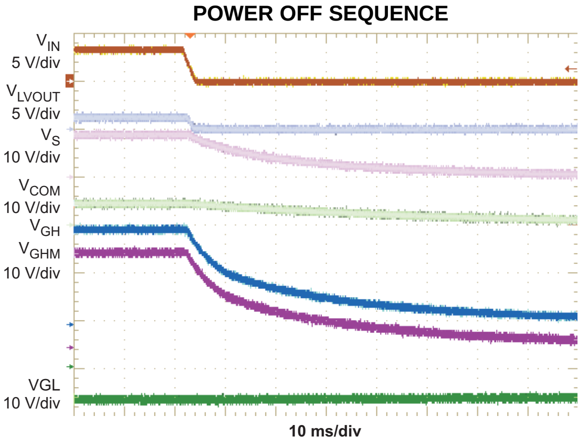


Figure 18.

APPLICATION INFORMATION

BOOST CONVERTER

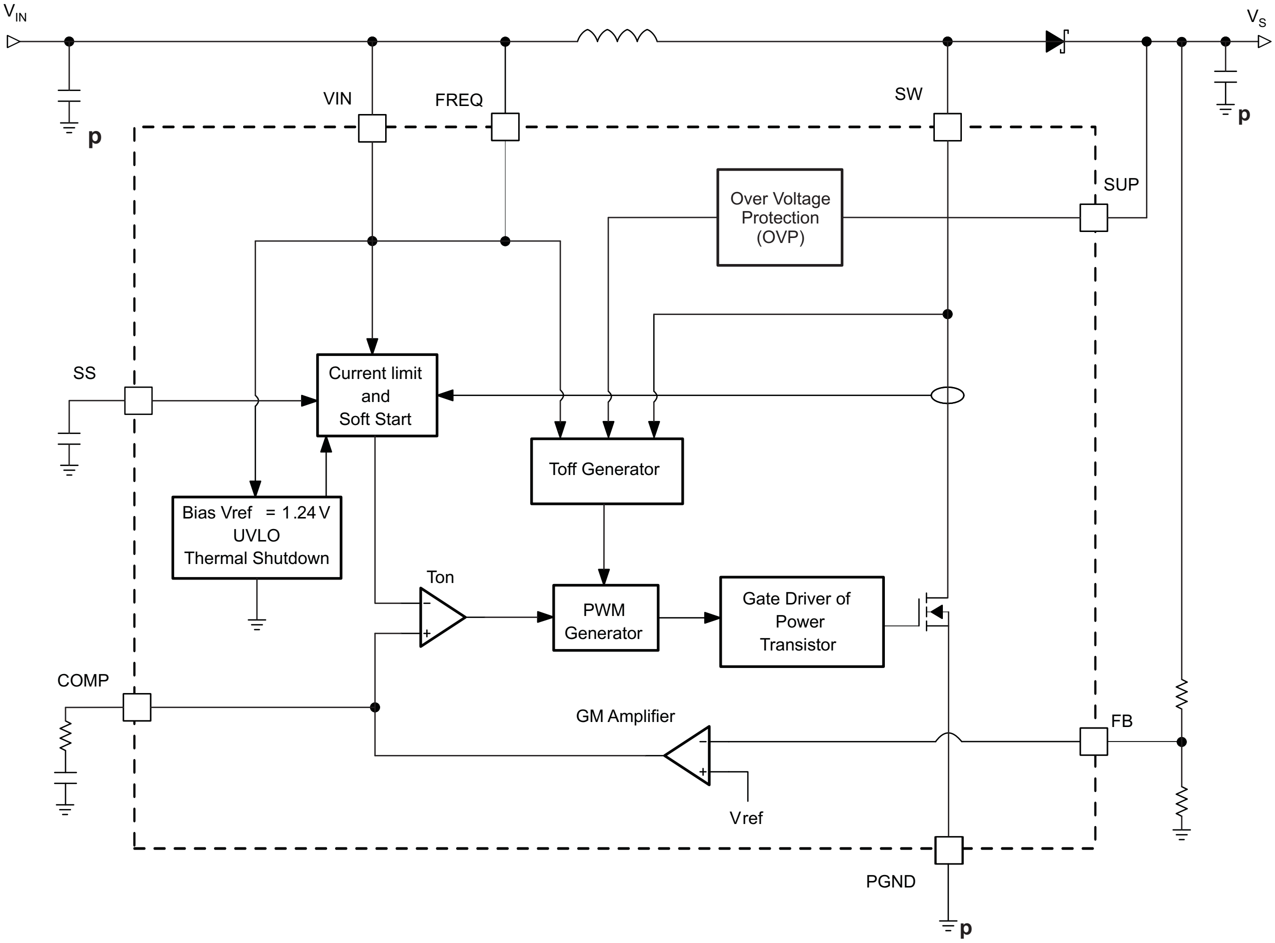

V_IN
V_S
VIN
FREQ
SW
SUP
Over Voltage Protection (OVP)
SS
Current limit and Soft Start
Toff Generator
Bias Vref = 1.24 V
UVLO
Thermal Shutdown
Ton
PWM Generator
Gate Driver of Power Transistor
COMP
GM Amplifier
FB
Vref
PGND
p

Figure 19. Boost converter block diagram

The boost converter is designed for output voltages up to 16.5 V with a switch peak current limit of 2.0 A minimum. The device, which operates in a current mode scheme with quasi-constant frequency, is externally compensated for maximum flexibility and stability. The switching frequency is selectable between 650 kHz and 1.2 MHz and the minimum input voltage is 2.5 V. To limit the inrush current at start-up a soft-start pin is available.

During the on-time, the current rises into the inductor. When the current reaches a threshold value set by the internal GM amplifier, the power transistor is turned off. The polarity of the inductor changes and forward biases the Schottky diode which lets the current flow towards the output of the boost converter. The off-time is fixed for a certain V_{IN} and V_S, and therefore maintains the same frequency when varying these parameters.

However, for different output loads, the frequency slightly changes due to the voltage drop across the $R_{DS(ON)}$ of the power transistor which will have an effect on the voltage across the inductor and thus on t_{ON} (t_{OFF} remains fixed).

The fixed off-time maintains a quasi-fixed frequency that provides better stability for the system over a wide range of input and output voltages than conventional boost converters. The TPS65146 topology has also the benefits of providing very good load and line regulations, and excellent line and load transient responses.

Boost Converter Design Procedure

The first step in the design procedure is to verify whether the maximum possible output current of the boost converter supports the specific application requirements. A simple approach is to estimate the converter efficiency, by taking the efficiency numbers from the provided efficiency curves or to use a worst case assumption for the expected efficiency, e.g. 85%.

1. Duty Cycle: $D = \frac{V_{IN} \times \eta}{V_S}$
2. Inductor ripple current: $\Delta I_L = \frac{V_{IN} \times D}{f \times L}$
3. Maximum output current: $I_{OUT\_max} = \left(I_{LIM\_min} - \frac{\Delta I_L}{2}\right) \times (1 - D)$
4. Peak switch Current: $I_{swpeak} = \frac{\Delta I_L}{2} + \frac{I_{out}}{1 - D}$

I_{swpeak} = converter switch current (must be < I_{LIM_min} = 2.0 A)
f_S = Converter switching frequency (typically 1.2 MHz or 650 kHz)
L = Selected inductor value (see the Inductor Selection section)
η = Estimated converter efficiency (please use the number from the efficiency plots or 85% as an estimation)
ΔI_L = Inductor peak-to-peak ripple current

The peak switch current is the steady state peak switch current the integrated switch, inductor and external Schottky diode has to be able to handle. The calculation must be done for the minimum input voltage where the peak switch current is highest.

Soft-Start (Boost Converter)

The boost converter has an adjustable soft-start to prevent high inrush current during start-up. To minimize the inrush current during start-up an external capacitor connected to the soft-start pin SS is used to slowly ramp up the internal current limit of the boost converter. When the V_{IN} exceeds the Undervoltage Lockout (UVLO) threshold, the soft-start capacitor C_{SS} is immediately charged up to 0.3 V. The capacitor is then charged at a constant current of 4 µA typically until the output of the boost converter V_S has reached its Power Good threshold (90% of V_S nominal value). During this time, the voltage on SS pin directly controls the peak inductor current, starting with 0 A at V_{SS} = 0.3 V up to the full current limit at $V_{SS} \approx$ 800 mV. The maximum load current is available after the soft-start is completed. The larger the capacitor, the slower the ramp of the current limit and the longer the soft-start time. A 100 nF capacitor is usually sufficient for most of the applications. When V_{IN} falls down below the UVLO level, the soft-start capacitor is discharged to ground.

Frequency Select Pin (FREQ)

The digital frequency select pin FREQ allows to set the switching frequency of the device to 650 kHz (FREQ = low) or 1.2 MHz (FREQ = high). Higher switching frequency improves load transient response but reduces slightly the efficiency. The other benefits of higher switching frequency are a lower output voltage ripple. Usually, it is recommended to use 1.2 MHz switching frequency unless light load efficiency is a major concern.

Inductor Selection

The main parameter for the inductor selection is the saturation current of the inductor which should be higher than the peak switch current as calculated above with additional margin to cover for heavy load transients. An alternative, more conservative, is to choose the inductor with a saturation current at least as high as the maximum switch current limit of 3.0 A. Another important parameter is the inductor DC resistance. Usually the lower the DC resistance the higher the efficiency. It is important to note that the inductor DC resistance is not the only parameter determining the efficiency. Especially for a boost converter where the inductor is the energy storage element, the type and core material of the inductor influences the efficiency as well. At high switching frequencies of 1.2 MHz inductor core losses, proximity effects and skin effects become more important. Usually an inductor with a larger form factor gives higher efficiency. The efficiency difference between different inductors can vary between 2% to 10%. For the TPS65146, inductor values between 3.3 µH and 6.8 µH are a good choice with a switching frequency of 1.2 MHz. At 650 kHz we recommend inductors between 7 µH and 13 µH. Isat ≥ I_{swpeak} imperatively. Possible inductors are shown in Table 1.

Table 1. Inductor Selection

L (µH)	COMPONENT SUPPLIER	COMPONENT CODE	SIZE (LxWxH mm)	DCR TYP (mΩ)	Isat (A)
1.2 MHz					
4.7	Sumida	CDRH3D14	4 × 4 × 1.5	120	1.1
4.7	Coilcraft	LPS4414-472ML	4.3 × 4.3 × 1.4	215	1.5
4.2	Sumida	CDRH5D28	5.7 × 5.7 × 3	23	2.2
5.0	Coilcraft	MSS7341	7.3 × 7.3 × 4.1	24	2.9
650 kHz					
10	Sumida	CDC5D23B	6 × 6 × 2.5	102	1.04
10	Sumida	CDR6D23MNNP	5 × 5 × 2.4	83	1.75
10	Würth Elektronik	744778910	7.3 × 7.3 × 3.2	51	2.2
10	Sumida	CDRH8D28	8.3 × 8.3 × 3	36	2.5

Rectifier Diode Selection

To achieve high efficiency a Schottky type should be used for the rectifier diode. The reverse voltage rating should be higher than the maximum output voltage of the converter. The averaged rectified forward current Iavg, the Schottky diode needs to be rated for, is equal to the output current I_{OUT}:

$$I_F = I_{OUT} \tag{1}$$

Usually a Schottky diode with 1 A to 1.5 A maximum average rectified forward current rating is sufficient for most of the applications. Also, the Schottky rectifier has to be able to dissipate the power. The dissipated power is the average rectified forward current I_F times the diode forward voltage V_F (or V_{Diode}).

$P_D = I_F \times V_F$

Typically the diode should be able to dissipate around 500mW depending on the load current and forward voltage.

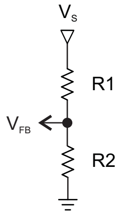
Table 2. Rectifier Diode Selection

CURRENT RATING I_F	V_R	V_F / I_F	COMPONENT SUPPLIER	COMPONENT CODE	PACKAGE TYPE
750 mA	20 V	0.425 V/750 mA	Fairchild Semiconductor	FYV0704S	SOT 23
1 A	20 V	0.39 V/1 A	NXP	PMEG2010AEH	SOD 123
1 A	20 V	0.5 V/1 A	Vishay	SS12	SMA
1 A	20 V	0.44 V/1 A	Vishay	MSS1P2L	µ-SMP (*Low Profile*)
1.5 A	25 V	0.5 V/1 A	Vishay	BYS10-25	SMA

Setting the Output Voltage

The output voltage is set by an external resistor divider. Typically, a minimum current of 50 µA flowing through the feedback divider is enough to cover the noise fluctuation. The resistors are then calculated with 70 µA as:

$$R2 = \frac{V_{FB}}{70\ \mu A} \approx 18\ k\Omega \qquad R1 = R2 \times \left(\frac{V_S}{V_{FB}} - 1\right) \tag{2}$$



with V_{FB} = 1.240 V

Compensation (COMP)

The regulation loop can be compensated by adjusting the external components connected to the COMP pin. The COMP pin is the output of the internal transconductance error amplifier. The compensation capacitor will adjust the low frequency gain and the resistor value will adjust the high frequency gain. Lower output voltages require a higher gain and therefore a lower compensation capacitor value. A good start, that will work for the majority of the applications is C_{COMP} = 3.3 nF and R_{COMP} = 18 kΩ for a 3.3 V input.

Input Capacitor Selection

For good input voltage filtering low ESR ceramic capacitors are recommended. TPS65146 has an analog input VIN. A 1-µF bypass is required as close as possible from VIN to GND.

One 10-µF ceramic input capacitor is sufficient for most of the applications. For better input voltage filtering this value can be increased. Refer to Table 3 and typical applications for input capacitor recommendations.

Output Capacitor Selection

For best output voltage filtering a low ESR output capacitor is recommended. Two 10-µF ceramic output capacitors work for most of the applications. Higher capacitor values can be used to improve the load transient response. Refer to Table 3 for the selection of the output capacitor.

Table 3. Rectifier Input and Output Capacitor Selection

CAPACITOR	VOLTAGE RATING	COMPONENT SUPPLIER	COMPONENT CODE	COMMENTS
10 µF/0805	10 V	Taiyo Yuden	LMK212 BJ 106KD	C_{IN}
1 µF/0603	10 V	Taiyo Yuden	EMK107 BJ 105KA	VIN bypass
10 µF/1206	25 V	Taiyo Yuden	TMK316 BJ 106ML	C_{OUT}

To calculate the output voltage ripple that following equations can be used:

$$\Delta V_C = \frac{V_S - V_{IN}}{V_S \times f} \times \frac{I_{OUT}}{C} \qquad \Delta V_{C\_ESR} = \Delta I_L \times R_{C\_ESR} \tag{3}$$

ΔV_{C_ESR} can be neglected in many cases since ceramic capacitors provide very low ESR.

Undervoltage Lockout (UVLO)

To avoid mis-operation of the device at low input voltages an undervoltage lockout is included that disables the device, if the input voltage falls below 2.0 V.

Thermal shutdown

A thermal shutdown is implemented to prevent damages because of excessive heat and power dissipation. Typically the thermal shutdown threshold for the junction temperature is 150°C. When the thermal shutdown is triggered the device stops switching until the junction temperature falls below typically 136 °C. Then the device starts switching again.

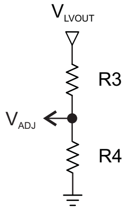
Overvoltage Protection

The boost converter has an integrated overvoltage protection to prevent the power switch from exceeding the absolute maximum switch voltage rating at pin SW in case the feedback (FB) pin is floating or shorted to GND. In such an event, the output voltage rises and is monitored with the overvoltage protection comparator over the SUP pin. As soon as the comparator trips at typically 18 V, the boost converter turns the N-Channel MOSFET switch off. The output voltage falls below the overvoltage threshold and the converter continues to operate. In order to detect overvoltage, the SUP pin needs to be connected to the output voltage of the boost converter V_S.

LOW DROPOUT LINEAR REGULATOR (LDO)

The TPS65146 includes a Low Dropout Regulator providing the logic voltage to the panel. The LDO is designed to operate typically with a 1-µF ceramic output capacitor. The LDO has an internal softstart feature to limit the inrush current. A minimum current of 50 µA flowing through the feedback divider is usually enough to cover the noise fluctuation. The resistors of the voltage divider are then calculated with 70 µA as:

$$R4 = \frac{V_{ADJ}}{70\ \mu A} \approx 18\ k\Omega \qquad R3 = R4 \times \left(\frac{V_{LVOUT}}{V_{ADJ}} - 1\right) \tag{4}$$

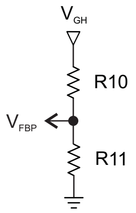


with V_{ADJ} = 1.240 V

REGULATED POSITIVE CHARGE PUMP

The positive charge pump sets the voltage applied on the VGH input pin, up to 32 V in tripler mode configuration. The charge pump block regulates the V_{GH} voltage by adjusting the drive current I_{DRVP}. Typically, a minimum current of 50 µA flowing through the feedback divider is usually enough to cover the noise fluctuation. The resistors of the divider used to set the V_{GH} voltage are calculated as:

$$R11 = \frac{V_{FBP}}{70\ \mu A} \approx 18\ k\Omega \qquad R10 = R11 \times \left(\frac{V_{GH}}{V_{FBP}} - 1\right) \tag{5}$$


V_GH
R10
V_FBP
R11

with V_{FBP} = 1.240 V

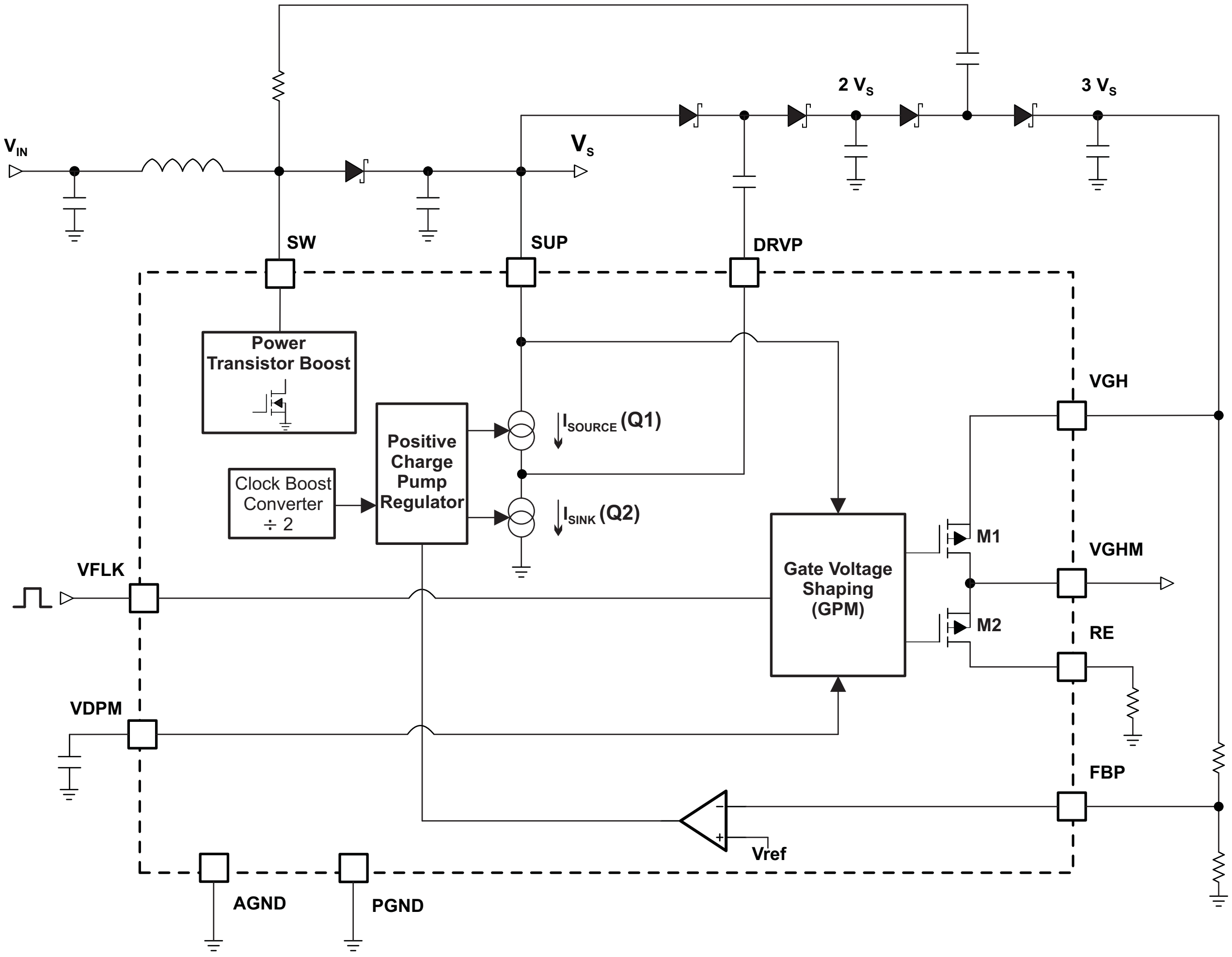

V_IN
V_S
2 V_S
3 V_S
SW
SUP
DRVP
Power Transistor Boost
Clock Boost Converter ÷ 2
Positive Charge Pump Regulator
I_SOURCE (Q1)
I_SINK (Q2)
VGH
VGHM
RE
FBP
M1
M2
Gate Voltage Shaping (GPM)
VFLK
VDPM
Vref
AGND
PGND

Figure 20. Positive Charge Pump regulator and Gate Voltage Shaping blocks

Doubler Mode: to use the positive Charge Pump in doubler mode configuration, the Schottky diode connected between the capacitor of DRVP pin and the 2.V_S point has to be connected to the 3.V_S point (seeFigure 20).

Tripler Mode: since VGH pin is rated to maximum 32 V, the maximum output voltage of the boost converter (V_S) possible is then limited to 11 V.

POSTIVE CHARGE PUMP CURRENT CAPABILITY

The possible output current that the positive charge pump is able to deliver in doubler mode depends mainly on the headroom ($2*V_S$ - V_{GH}) and the internal voltage drop $V_{drop\_internal}$. The graph below (Figure 21) helps defining the headroom range that the system needs:

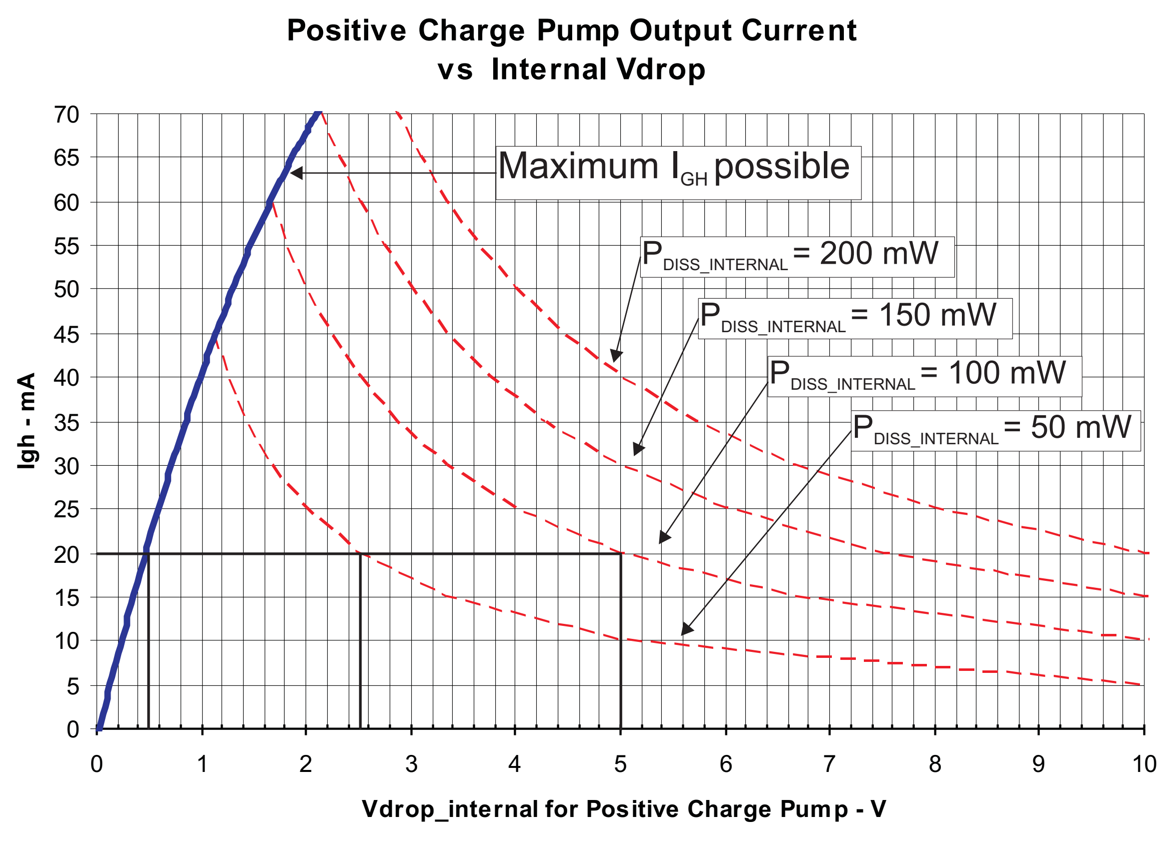


Figure 21.

Example:

For I_{GH} = 20 mA, we refer to the “maximum I_{GH} possible” curve to determine the minimum headroom needed.

$$V_{headroom\_20mA} = 2.V_{SUP} - V_{GH} \geq V_{drop\_int\_20mA} + 2.V_{Diode}* = 0.5 + 2V = 2.5V \qquad (6)$$

* in the case where V_{Diode} = 1 V

This means that the headroom in this example must be more than 2.5 V to be able to source 20 mA at the output of the positive charge pump.

However, generating a too large headroom can lead to excessive power dissipation. The dashed curves show the internal power dissipation generated by a certain internal voltage drop. In the above example, if $V_{headroom\_20mA}$ = 7 V (with V_{Diode} = 1 V), $V_{drop\_internal\_min}$ = 5 V and the internal power dissipation $P_{DISS\_INTERNAL}$ for the positive charge pump would reach 100 mW. The power dissipation of the charge pump block needs to be taken into account for the overall power dissipation rating.

NOTE:

refer to the power rating table not to exceed the overall maximum package power dissipation allowed.

EXTERNAL NEGATIVE CHARGE PUMP

The external negative charge pump works with two stages (charge pump and regulation). The charge pump provides a negative regulated output voltage. Figure 22 shows the operation details of the negative charge pump. With the first stage, the voltage on the collector of the bipolar transistor is equal to $-V_S+V_D$.

The next stage regulates the output voltage V_{GL}. A resistor and a Zener diode are used to clamp the voltage to the desired output value. The bipolar transistor is used to provide better load regulation as well as to reduce the quiescent current. The output voltage on V_{GL} will be equal to $-V_Z-V_{be}$.

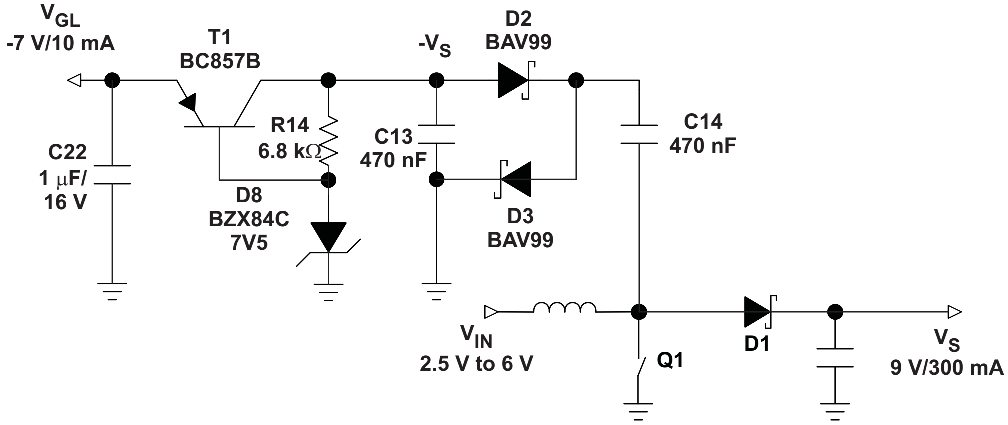


Figure 22. Partially Regulated External Negative

Capacitors (Charge Pumps)

For best output voltage filtering a low ESR output capacitor is recommended. Ceramic capacitors have a low ESR value but depending on the application tantalum capacitors can be used as well. For every capacitor, the reactance value has to be calculated as follows:

$$Xc = \frac{1}{2 \times \pi \times f \times C} \tag{7}$$

This value should be as low as possible in order to reduce the voltage drop due to the current flowing through it. The rated voltage of the capacitor has to be able to withstand the voltage across it. Capacitors rated at 50 V are enough for most of the applications. Typically a 470-nF capacitance is sufficient for the flying capacitors whereas bigger values like 1 µF or more can be used for the output capacitors to reduce the output voltage ripple.

CAPACITOR	COMPONENT SUPPLIER	COMPONENT CODE	COMMENTS
100 nF/0603	Taiyo Yuden	UMK107 BJ 104KA	Flying Cap
470 nF/0805	Taiyo Yuden	UMK212 BJ 474KG	Output Cap 1
1 µF/1210	Taiyo Yuden	UMK325 BJ 105KH	Output Cap 2

Diodes (Charge Pumps)

For high efficiency, one has to minimize the forward voltage drop of the diodes. Schottky diodes are recommended. The reverse voltage rating must withstand the maximum output voltage V_S of the boost converter. Usually a Schottky diode with 200 mA average forward rectified current is suitable for most of the applications.

CURRENT RATING I_{avg}	V_r	$V_{forward}$ / I_{avg}	COMPONENT SUPPLIER	COMPONENT CODE	PACKAGE TYPE
200 mA	30 V	0.5V / 30mA	International Rectifier	BAT54S	SOT 23

GATE VOLTAGE SHAPING FUNCTION

Sequencing

At start-up, the VGHM output is enabled once VDPM voltage is higher than V_{ref} = 1.240 V. The capacitor connected to VDPM pin sets a delay from the Power Good signal of the boost converter.

$$C_{VDPM} = \frac{I_{DPM} \times t_{DPM}}{V_{ref}} = \frac{20\ \mu A \times t_{DPM}}{1.240\ V} \quad (8)$$

At power off, VGHM is connected to VGH as soon as V_{IN} reaches the threshold voltage of the reset function.

Setting the Discharge Slope for Gate Voltage Shaping

VFLK = ‘high’ → VGHM discharges to 0V

VFLK = ‘low’ → VGHM = VGH

The slope at which V_{GHM} discharges is set by the external resistor connected to RE, the internal MOSFET $R_{DS(ON)}$ (typ. 13Ω for M2 – see block diagram below) and by the external gate line capacitance connected to VGHM pin.

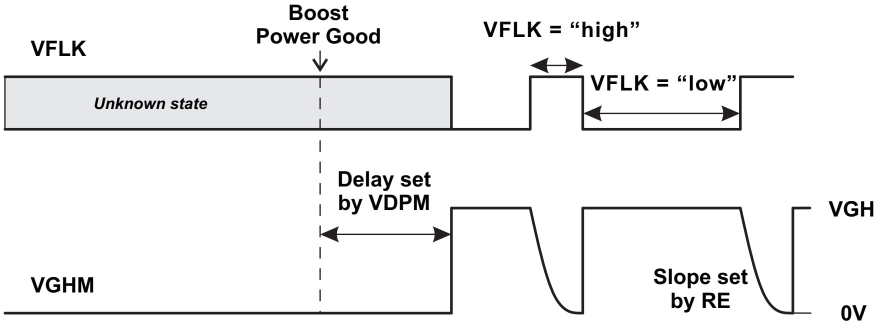


Figure 23. Gate Voltage Shaping Timing

If VFLK = ’high’ and RE is connected with a resistor to ground (see Figure 23), V_{GHM} will discharge from V_{GH} to 0V. Since 5*τ (τ = R*C) are needed to fully discharge C through R, we can define the time-constant of the gate voltage shaping block as follow:

$$\tau = (Re + R_{DS(ON)M2}) \times C_{VGHM}$$

Therefore, if the discharge of C_{VGHM} should finish during V_{FLK} = 'high':

$$t_{discharge} = 5 \times \tau = t_{V_{FLK} = \text{'high'}} \quad \Rightarrow \quad RE = \frac{t_{V_{FLK} = \text{'high'}}}{5 \times C_{VGHM}} - R_{DS(ON)M2} \quad (9)$$

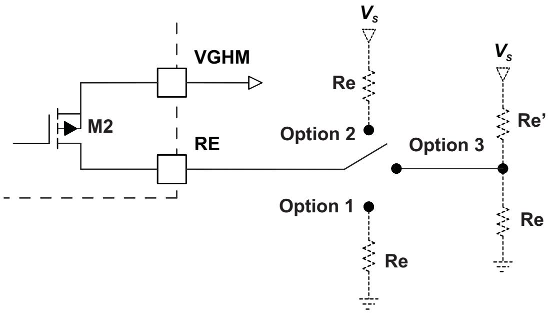


Figure 24. Discharge Path Options for VGHM

Options 2 and 3 from Figure 24 work like option 1 explained above. When M2 is turned on, V_{GHM} discharges with a slope set by Re from V_{GH} level down to V_S in option 2 configuration and in option 3 configuration down to the voltage set by the resistor divider. The discharging slope is set by Re resistor(s).

NOTE:

when options 2 or 3 are used, V_{GHM} is not held to 0V at startup but to the voltage set on RE pin by the resistors Re and Re’.

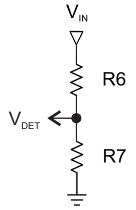
VCOM BUFFER

The VCOM Buffer power supply pin is the SUP pin connected to the boost converter V_S. To achieve good performance and minimize the output noise, a 1-µF ceramic bypass capacitor is required directly from the SUP pin to ground. The buffer is not designed to drive high capacitive loads; therefore it is recommended to connect a series resistor at the output to provide stable operation when driving high capacitive load. With a 3.3-Ω series resistor, a capacitive load of 10 nF can be driven, which is usually sufficient for typical LCD applications.

RESET FUNCTION

The device has an integrated reset function with an open drain output capable of sinking 1 mA. The reset function monitors the voltage applied to its sense input VDET. As soon as the voltage on VDET falls below the threshold voltage (V_{DET}) of typically 1.1 V, the reset function asserts its reset signal by pulling $\overline{\text{XAO}}$ low. Typically, a minimum current of 50µA flowing through the feedback divider is enough to cover the noise fluctuation. Therefore, to select R6, one has to set the input voltage limit (V_{IN_LIM}) at which the reset function will pull $\overline{\text{XAO}}$ to low state. *V_{IN_LIM} must be higher than the UVLO threshold*.

$$R7 = \frac{V_{DET}}{70\ \mu A} \approx 18\ k\Omega \qquad R6 = R7 \times \left(\frac{V_{IN\_LIM}}{1.1\ V} - 1\right) \tag{10}$$



with V_{DET} = 1.1 V

When the input voltage V_{IN} rises, once the voltage on VDET pin exceeds its threshold voltage plus hysterisis the $\overline{\text{XAO}}$ signal will go high after the delay time set by the capacitor connected to CDET.

$$C_{DET} = \frac{10\ \mu A \times t_{DET}}{1.240\ V} \tag{11}$$

The reset function is operational for $V_{IN} \geq 1.6$ V.

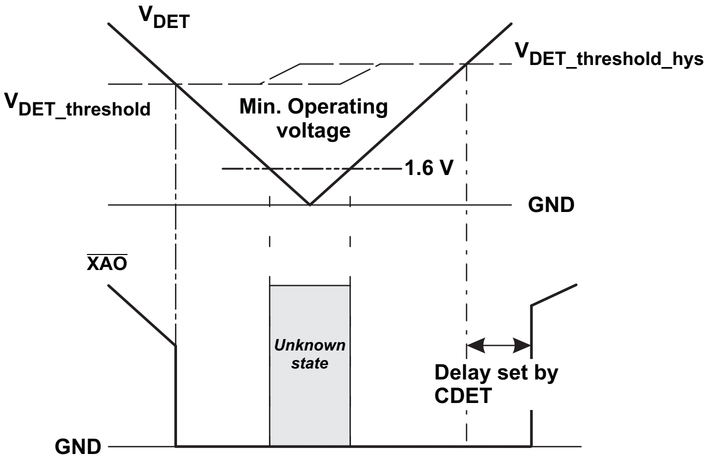


Figure 25. Voltage Detection and $\overline{\text{XAO}}$ Pin

The reset function is configured as a standard open-drain and requires a pull-up resistor. The resistor $R_{\overline{XAO}}$ (R5) which must be connected between the $\overline{\text{XAO}}$ pin and a positive voltage V_X greater than 2V - 'high' logic level - e.g. V_{LVOUT} , can be chosen as follows:

$$R_{\overline{XAO}\_min} > \frac{V_X}{1\ mA} \qquad \& \qquad R_{\overline{XAO}\_max} < \frac{V_X - 2\ V}{2\ \mu A} \tag{12}$$

Power on sequencing

Once the input voltage V_{IN} reaches the Under Voltage Lockout (UVLO), the device is internally enabled and the LDO starts rising. When V_{LVOUT} of the LDO is at its Power Good voltage, the boost converter, as well as the Vcom buffer are enabled. As soon as V_S of the boost converter reaches its Power Good (90% of its nominal value), the positive charge pump block is enabled. Then the capacitor connected to VDPM is charged, setting the gate voltage shaping block delay time, and finally enables the VGHM signal.

1. LDO
2. Boost converter & VCOM Buffer
3. VGH and VDPM (delay time to enable the gate voltage shaping function)
4. VGHM (after proper delay)

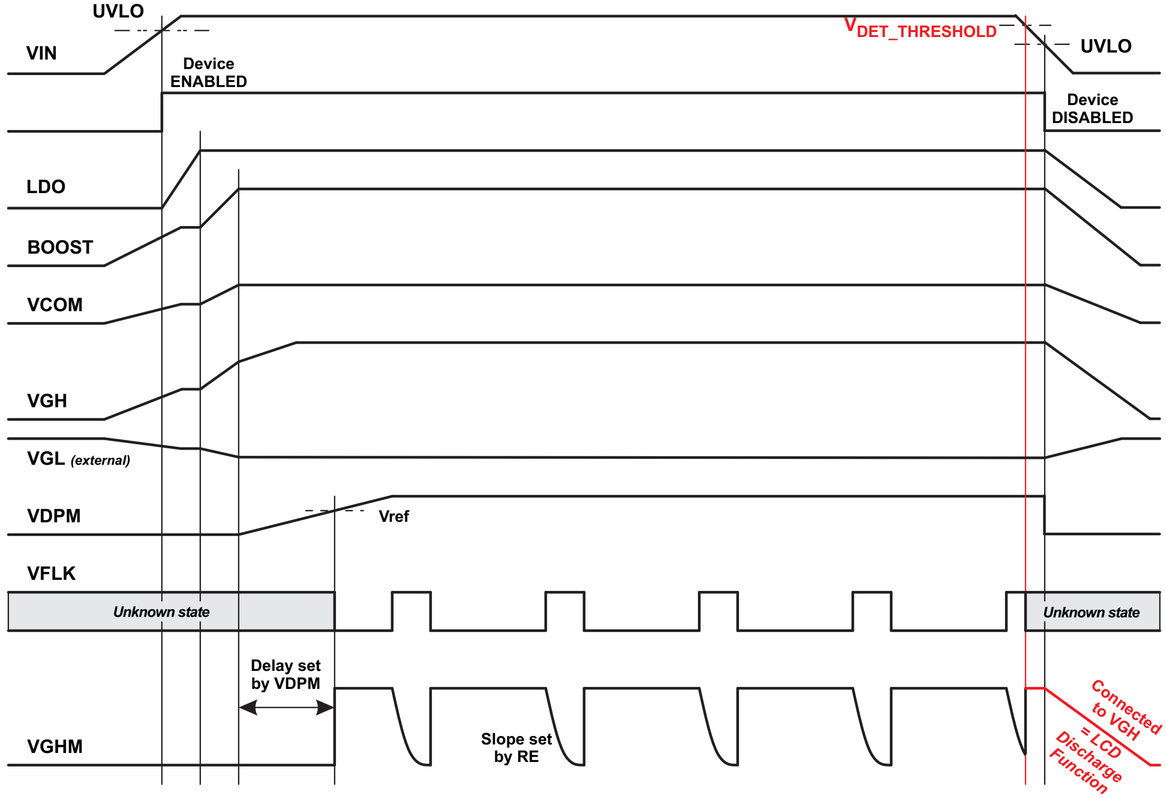

UVLO
VIN
Device
ENABLED
$V_{DET\_THRESHOLD}$
UVLO
Device
DISABLED
LDO
BOOST
VCOM
VGH
VGL (external)
VDPM
Vref
VFLK
Unknown state
Unknown state
Delay set
by VDPM
Slope set
by RE
VGHM
Connected
to VGH
= LCD
Discharge
Function

Figure 26. Sequencing TPS65146

Power off sequencing and LCD discharge function

When the input voltage V_{IN} falls below a predefined threshold (set by $V_{DET\_THRESHOLD}$ - see Figure 26), $\overline{\text{XAO}}$ is driven low and V_{GHM} is driven to V_{GH}. (Note that when V_{IN} falls below the UVLO threshold, all IC functions are disabled except $\overline{\text{XAO}}$ and V_{GHM}). Since VGHM is connected to VGH, it tracks the output of the positive charge pump as it decays. This feature, together with $\overline{\text{XAO}}$ can be used to discharge the panel by turning on all the pixel TFTs and discharging them into the gradually decaying V_{GHM} voltage. V_{GHM} is held low during power-up.

APPLICATION INFORMATION

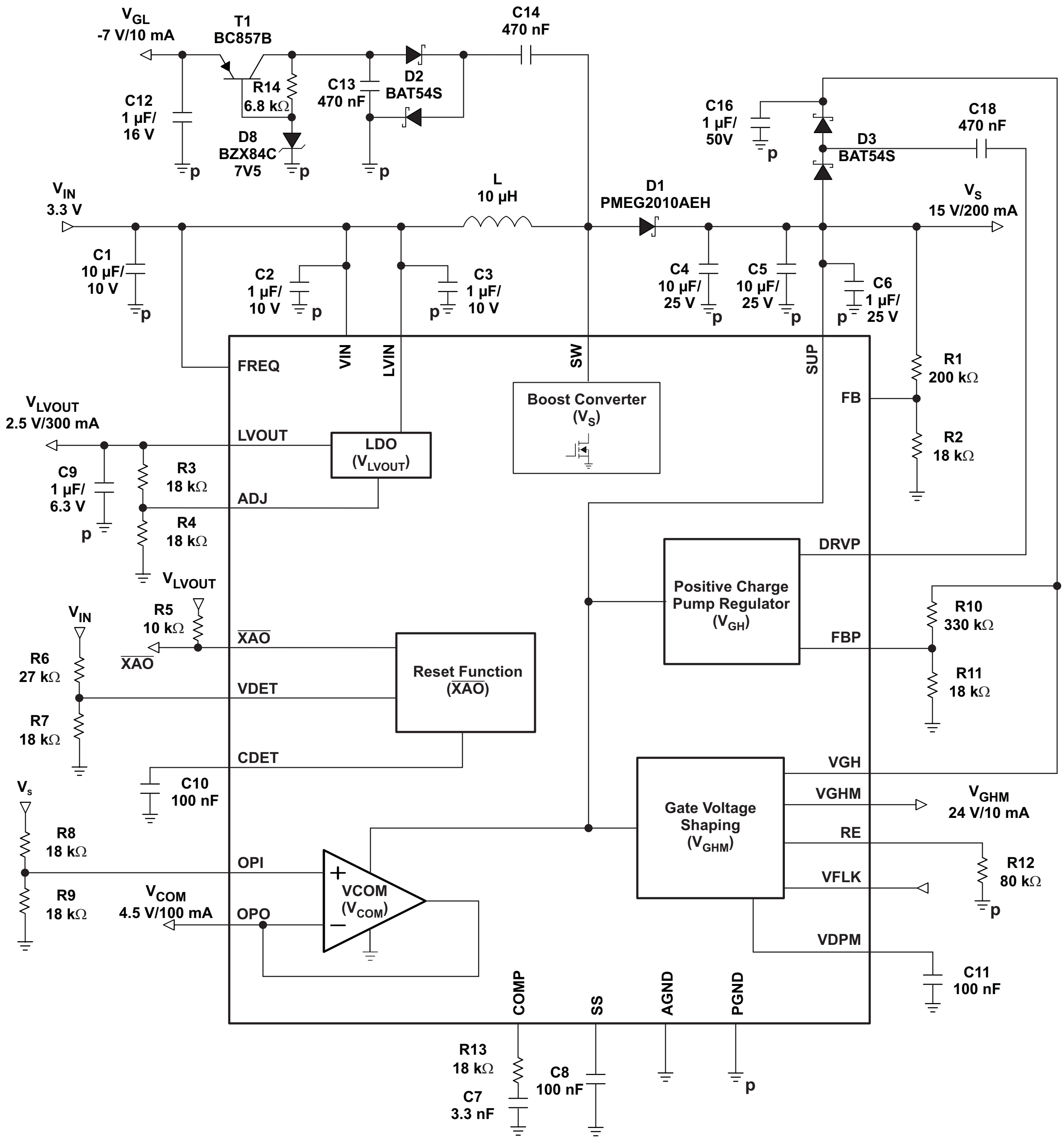

VGL -7 V/10 mA
T1 BC857B
C14 470 nF
C12 1 µF/ 16 V
R14 6.8 kΩ
C13 470 nF
D2 BAT54S
D8 BZX84C 7V5
C16 1 µF/ 50V
C18 470 nF
D3 BAT54S
VIN 3.3 V
L 10 µH
D1 PMEG2010AEH
VS 15 V/200 mA
C1 10 µF/ 10 V
C2 1 µF/ 10 V
C3 1 µF/ 10 V
C4 10 µF/ 25 V
C5 10 µF/ 25 V
C6 1 µF/ 25 V
FREQ
VIN
LVIN
SW
SUP
FB
R1 200 kΩ
R2 18 kΩ
Boost Converter (VS)
VLVOUT 2.5 V/300 mA
LVOUT
LDO (VLVOUT)
ADJ
C9 1 µF/ 6.3 V
R3 18 kΩ
R4 18 kΩ
DRVP
Positive Charge Pump Regulator (VGH)
FBP
R10 330 kΩ
R11 18 kΩ
VLVOUT
R5 10 kΩ
XAO
Reset Function (XAO)
VDET
R6 27 kΩ
R7 18 kΩ
CDET
C10 100 nF
VGH
VGHM
VGHM 24 V/10 mA
Gate Voltage Shaping (VGHM)
RE
R12 80 kΩ
VFLK
VDPM
C11 100 nF
Vs
R8 18 kΩ
R9 18 kΩ
OPI
OPO
VCOM (VCOM)
VCOM 4.5 V/100 mA
COMP
SS
AGND
PGND
R13 18 kΩ
C7 3.3 nF
C8 100 nF
p

Figure 27. TPS65146 Typical Application with Positive Charge Pump in Doubler Mode Configuration

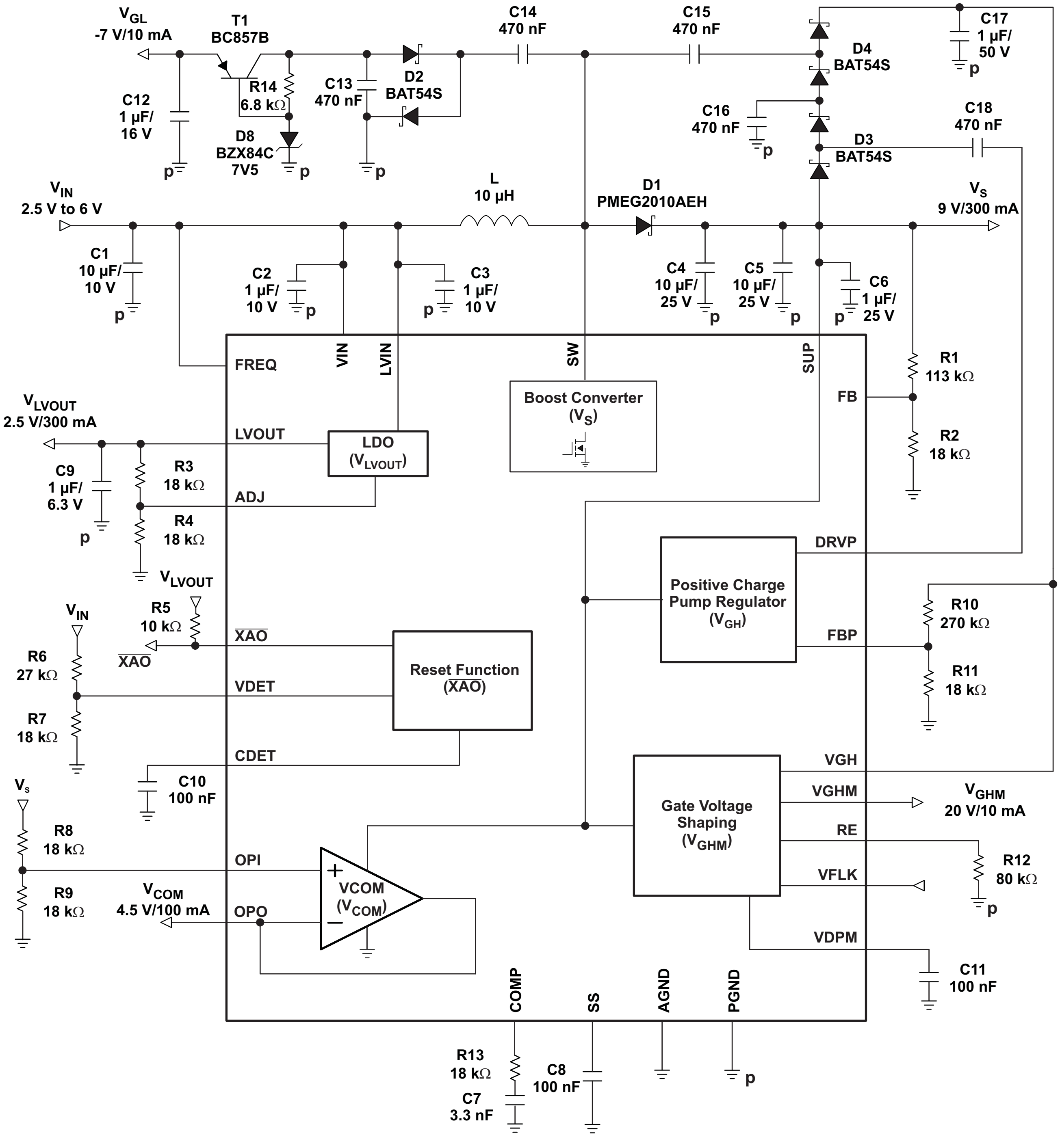

V_{GL}
-7 V/10 mA
T1
BC857B
R14
6.8 kΩ
C12
1 µF/
16 V
D8
BZX84C
7V5
C13
470 nF
D2
BAT54S
C14
470 nF
C15
470 nF
C17
1 µF/
50 V
D4
BAT54S
C16
470 nF
C18
470 nF
D3
BAT54S
V_{IN}
2.5 V to 6 V
L
10 µH
D1
PMEG2010AEH
V_S
9 V/300 mA
C1
10 µF/
10 V
C2
1 µF/
10 V
C3
1 µF/
10 V
C4
10 µF/
25 V
C5
10 µF/
25 V
C6
1 µF/
25 V
p
FREQ
VIN
LVIN
SW
SUP
FB
R1
113 kΩ
R2
18 kΩ
Boost Converter
(V_S)
V_{LVOUT}
2.5 V/300 mA
LVOUT
LDO
(V_{LVOUT})
ADJ
C9
1 µF/
6.3 V
R3
18 kΩ
R4
18 kΩ
V_{LVOUT}
DRVP
Positive Charge
Pump Regulator
(V_{GH})
FBP
R10
270 kΩ
R11
18 kΩ
V_{IN}
R5
10 kΩ
$\overline{XAO}$
R6
27 kΩ
R7
18 kΩ
VDET
Reset Function
($\overline{XAO}$)
CDET
C10
100 nF
VGH
VGHM
V_{GHM}
20 V/10 mA
Gate Voltage
Shaping
(V_{GHM})
RE
R12
80 kΩ
VFLK
VDPM
C11
100 nF
V_S
R8
18 kΩ
R9
18 kΩ
OPI
V_{COM}
4.5 V/100 mA
OPO
VCOM
(V_{COM})
COMP
SS
AGND
PGND
R13
18 kΩ
C7
3.3 nF
C8
100 nF

Figure 28. TPS65146 Typical Application with Positive Charge Pump in Tripler Mode Configuration

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS65146RGER	ACTIVE	VQFN	RGE	24	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CEZ	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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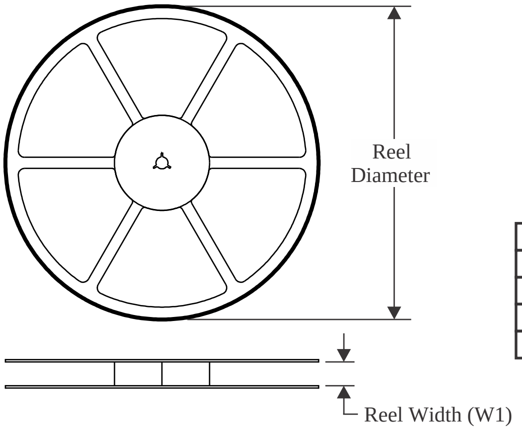
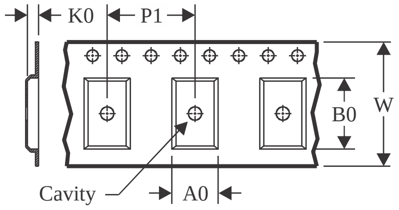
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

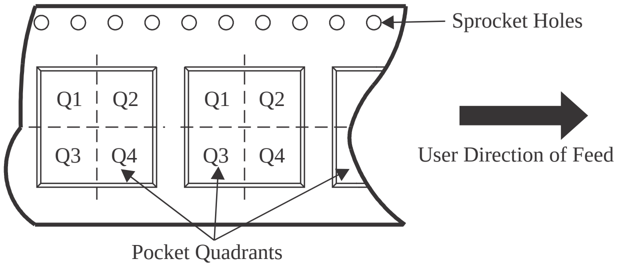

Reel
Diameter
Reel Width (W1)

TAPE DIMENSIONS


K0
P1
B0
W
Cavity
A0

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

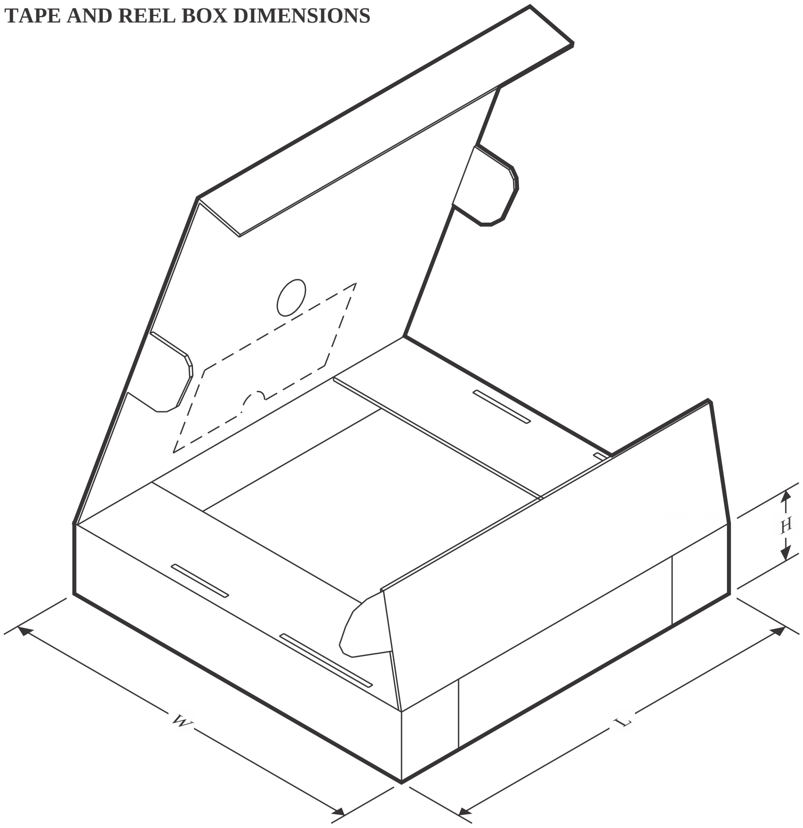
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


Sprocket Holes
Q1
Q2
Q3
Q4
Q1
Q2
Q3
Q4
User Direction of Feed
Pocket Quadrants

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65146RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

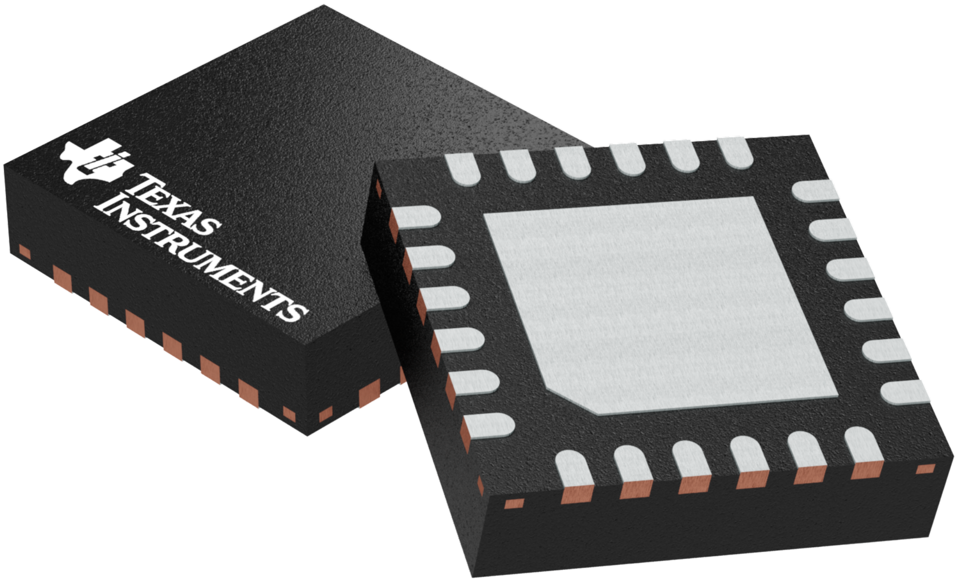
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65146RGER	VQFN	RGE	24	3000	356.0	356.0	35.0

GENERIC PACKAGE VIEW

RGE 24

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

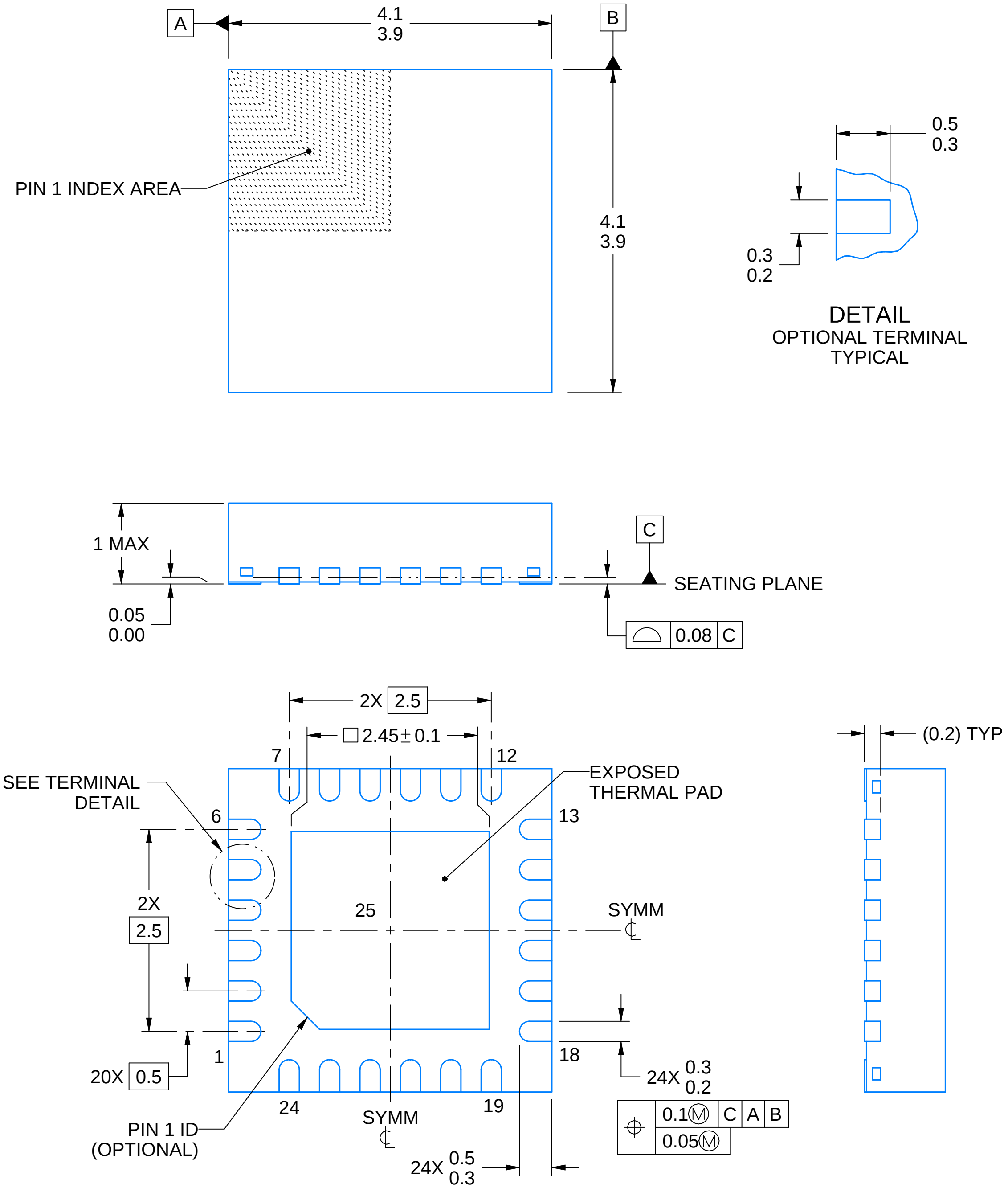


Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD


A
4.1
3.9
B
PIN 1 INDEX AREA
4.1
3.9
0.5
0.3
0.3
0.2
DETAIL
OPTIONAL TERMINAL
TYPICAL
1 MAX
C
SEATING PLANE
0.05
0.00
0.08 C
2X 2.5
□2.45±0.1
7
12
SEE TERMINAL
DETAIL
EXPOSED
THERMAL PAD
6
13
25
SYMM
2X
2.5
18
1
20X 0.5
24X 0.3
0.2
0.1Ⓜ C A B
0.05Ⓜ
24
19
SYMM
PIN 1 ID
(OPTIONAL)
24X 0.5
0.3
(0.2) TYP

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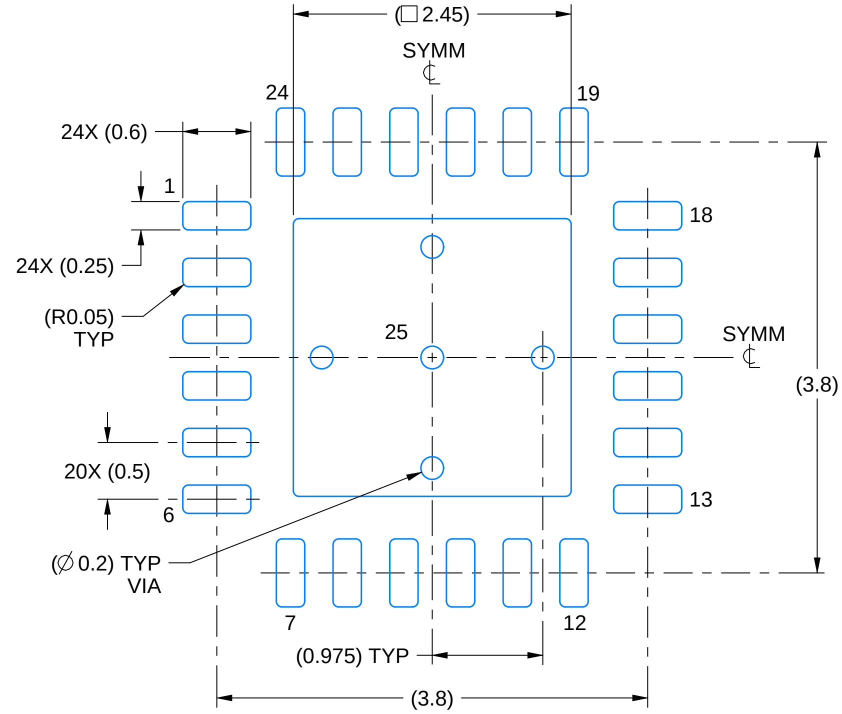
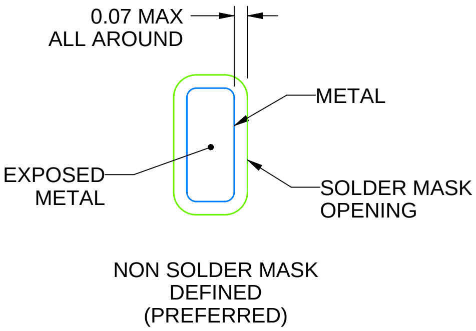
NOTES:

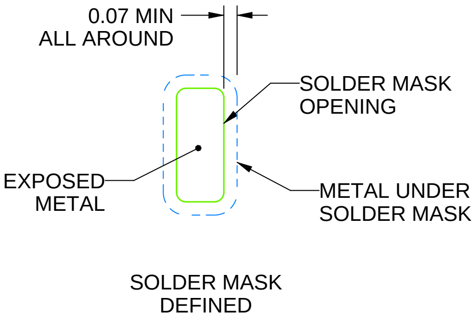
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.


(□2.45)
SYMM
℄
24
19
24X (0.6)
1
24X (0.25)
(R0.05)
TYP
25
SYMM
℄
18
(3.8)
20X (0.5)
6
13
(∅0.2) TYP
VIA
7
12
(0.975) TYP
(3.8)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X


0.07 MAX
ALL AROUND
METAL
EXPOSED
METAL
SOLDER MASK
OPENING

NON SOLDER MASK
DEFINED
(PREFERRED)


0.07 MIN
ALL AROUND
SOLDER MASK
OPENING
EXPOSED
METAL
METAL UNDER
SOLDER MASK

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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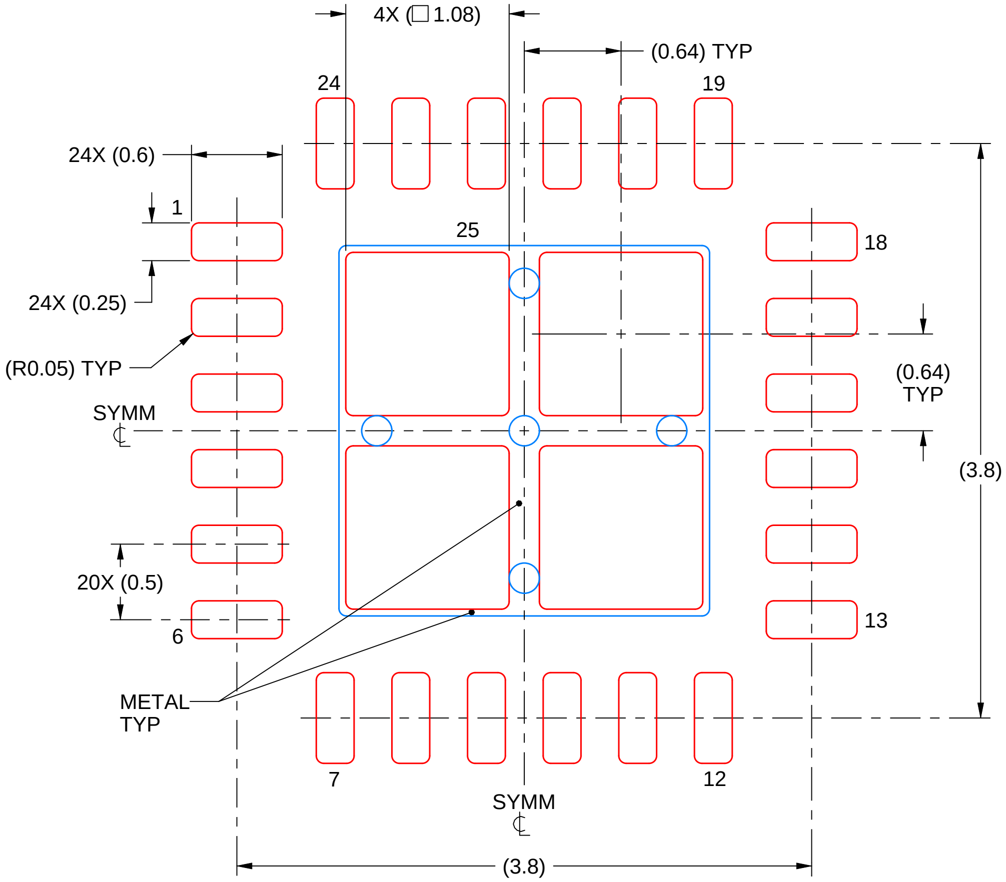
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



4X (□1.08)
(0.64) TYP
24
19
24X (0.6)
1
25
18
24X (0.25)
(R0.05) TYP
(0.64)
TYP
SYMM
℄
(3.8)
20X (0.5)
6
13
METAL
TYP
7
12
SYMM
℄
(3.8)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4219013/A 05/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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