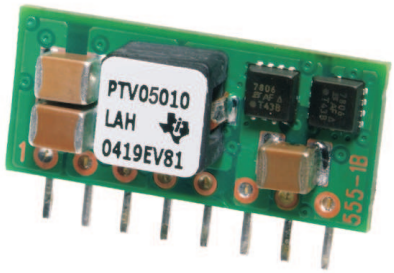
8-A, 5-V INPUT NONISOLATED WIDE-OUTPUT ADJUST SIP MODULE

FEATURES

- **Up to 8-A Output Current**
- **5-V Input Bus**
- **Wide-Output Voltage Adjust (0.8 V to 3.6 V)**
- **Efficiencies up to 95%**
- **On/Off Inhibit**
- **Prebias Start-Up**
- **Undervoltage Lockout**
- **Auto-Track™ Sequencing**
- **Output Overcurrent Protection (Nonlatching, Auto-Reset)**
- **Operating Temperature: –40°C to 85°C**
- **Safety Agency Approvals: UL/cUL 60950, EN60950 VDE**
- **POLA™ Compatible**

APPLICATIONS

- **Multivoltage Digital Systems**
- **High-Density Logic Circuits**
- **High-End Computers and Servers**
- **5-V Intermediate Bus Architectures**



DESCRIPTION

The PTV05010W is a ready-to-use nonisolated power module, and part of a new class of complete dc/dc switching regulators from Texas Instruments. These regulators combine high performance with double-sided, surface-mount construction, to give designers the flexibility to power the most complex multiprocessor digital systems using off-the-shelf catalog parts.

The PTV05010W series is produced in a 8-pin, single in-line pin (SIP) package. The SIP footprint minimizes board space, and offers an alternate package option for space conscious applications. Operating from a 5-V input bus, the series provides step-down conversion to a wide range of output voltages, at up to 8 A of output current. The output voltage can be set to any value over the range, 0.8 V to 3.6 V, using a single external resistor.

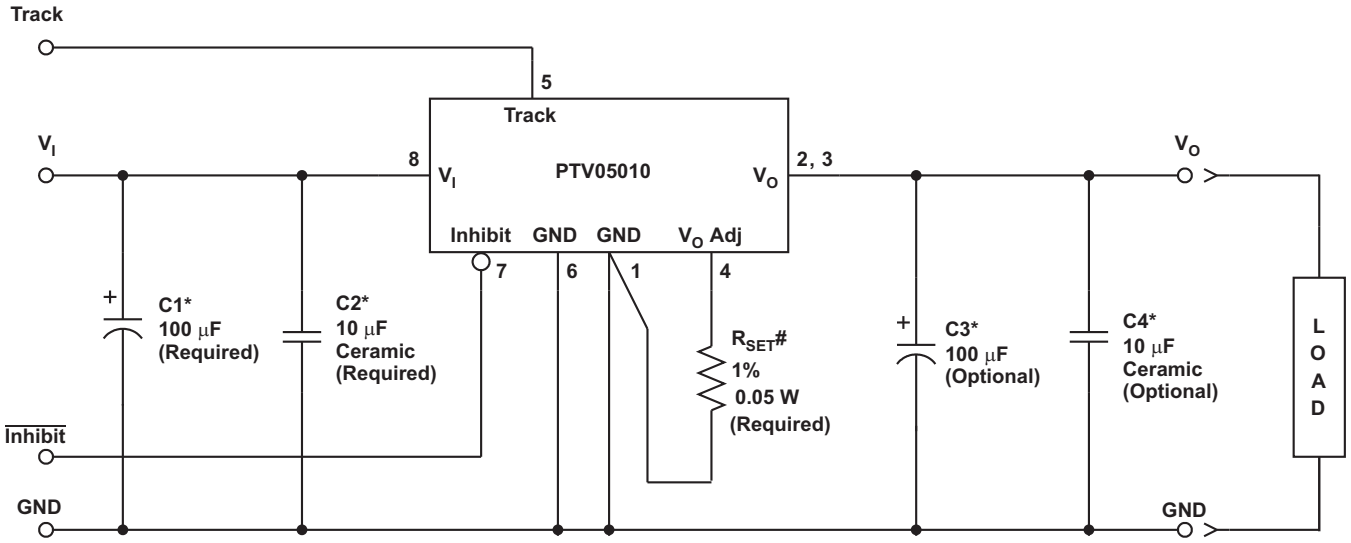
This series includes Auto-Track™. Auto-Track™ simplifies the task of supply-voltage sequencing in a power system by enabling the output voltage of multiple modules to accurately track each other, or any external voltage, during power up and power down.

Other operating features include an on/off inhibit, and the ability to start up into an existing output voltage or prebias. A nonlatching overcurrent trip protects against load faults.

Target applications include complex multivoltage, multiprocessor systems that incorporate the industry's high-speed microprocessors, bus drivers, and the TMS320™ DSP family.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

STANDARD APPLICATION



* See the Application Information for capacitor recommendations

R_{SET} is required to adjust the output voltage higher than its lowest value. See the *Application Information* section for values.

ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum at the end of this data sheet, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

			UNIT
$V_{(Track)}$	Track input voltage		–0.3 V to V_I +0.3 V
T_A	Operating temperature range	Over V_I range	–40°C to 85°C
	Lead temperature	5 seconds	260°C (2)
T_{stg}	Storage temperature		–55°C to 125°C
$V_{(INH)}$	Inhibit input voltage		–0.3 V to 7 V

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) This product is not compatible with surface-mount reflow solder processes.

PACKAGE SPECIFICATIONS

PTV05010W (Suffix AH)		
Weight		2.5 grams
Flammability	Meets UL 94 V-O	
Mechanical shock	Per Mil-STD-883D, Method 2002.3, 1 ms, 1/2 sine, mounted	500 G (1)
Mechanical vibration	Mil-STD-883D, Method 2007.2, 20 Hz - 2000 Hz	10 G (1)

(1) Qualification limit.

ELECTRICAL CHARACTERISTICS

operating at 25°C free-air temperature, V_I = 5 V, V_O = 3.3 V, C1 = 100 µF, C2 = 10 µF, C3 = 0 µF, C4 = 0 µF, and I_O = I_O max (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_O	Output current	Natural convection airflow		0		8 (1)	A
V_I	Input voltage range	Over I_O load range		4.5		5.5	V
V_O	Set-point voltage tolerance					2% (2)	
	Temperature variation	–40°C < T_A < 85°C			0.5%		
	Line regulation	Over V_I range			5		mV
	Load regulation	Over I_O range			5		mV
	Total output variation	Includes set-point, line, load, –40°C ≤ T_A ≤ 85°C				3 (2)	%V_o
	Adjust range	Over V_I range		0.8		3.6	V
η	Efficiency	I_O = I_O max	R_{SET} = 698 Ω, V_O = 3.3 V		95%		
			R_{SET} = 2.21 kΩ, V_O = 2.5 V		93%		
			R_{SET} = 5.49 kΩ, V_O = 1.8 V		90%		
			R_{SET} = 8.87 kΩ, V_O = 1.5 V		89%		
			R_{SET} = 17.4 kΩ, V_O = 1.2 V		87%		
			R_{SET} = 36.5 kΩ, V_O = 1 V		85%		
	Output voltage ripple (pk-pk)	20-MHz bandwidth			15		mV_{PP}
I_O (trip)	Overcurrent threshold	Reset, followed by auto-recovery			12		A
	Transient response	1-A/µs load step, 50 to 100% I_O max, C3 = 100 µF					
			Recovery time		70		µs
			V_o over/undershoot		100		mV
	Track control (pin 9)	I_{IL} Input low current	Pin to GND			–0.13	mA
		Control slew-rate limit	C3 ≤ C3 (max)			1	V/ms
UVLO	Undervoltage lockout	V_I increasing			4.3	4.5	V
		V_I decreasing		3.1	3.7		
	Inhibit control (pin 12)	V_{IH} Input high voltage	Referenced to GND	V_I – 0.5		Open (3)	V
		V_{IL} Input low voltage		–0.2		0.6	
		I_{IL} Input low current	Pin to GND		0.24		mA
I_I (stby)	Input standby current	Inhibit (pin 7) to GND, Track (pin 5) open			5		mA
f_S	Switching frequency	Over V_I and I_O ranges		550	600	650	kHz
	External input capacitance		Nonceramic (C1)	100 (4)			µF
			Ceramic (C2)	10 (4)			
	External output capacitance (C3)	Capacitance value	Nonceramic	0	100 (5)	3300 (6)	µF
			Ceramic	0		300	
		Equivalent series resistance (nonceramic)		4 (7)			mΩ
MTBF	Reliability	Per Telcordia SR-332, 50% stress, T_A = 40°C, ground benign			5		10^6 Hr

(1) See thermal derating curves for safe operating area (SOA), or consult factory for appropriate derating.
(2) The set-point voltage tolerance is affected by the tolerance and stability of R_{SET}. The stated limit is unconditionally met if R_{SET} has a tolerance of 1%, with 100 ppm/°C or better temperature stability.
(3) This control pin is internally pulled up to the input voltage, V_I. If this input is left open circuit, the module will operate when input power is applied. A small low-leakage (< 100 nA) MOSFET is recommended for control. For further information, see the related application note.
(4) A 10-µF high-frequency ceramic capacitor and 100-µF electrolytic input capacitor are required for proper operation. The electrolytic capacitor must be rated for 300 mArms minimum ripple current. See the Application Information for further guidance on capacitor selection.
(5) An external output capacitor is not required for basic operation. Adding 100 µF of distributed capacitance at the load improves the transient response.
(6) This is the calculated maximum. The minimum ESR limitation often results in a lower value. When controlling the Track pin using a voltage supervisor, C_O(max) is reduced to 2200 µF. See the Application Information for further guidance.
(7) This is the typical ESR for all the electrolytic (nonceramic) output capacitance. Use 7 mΩ as the minimum when using maximum-ESR values to calculate.

TYPICAL CHARACTERISTICS (5-V INPUT)(8)(9)

EFFICIENCY vs OUTPUT CURRENT

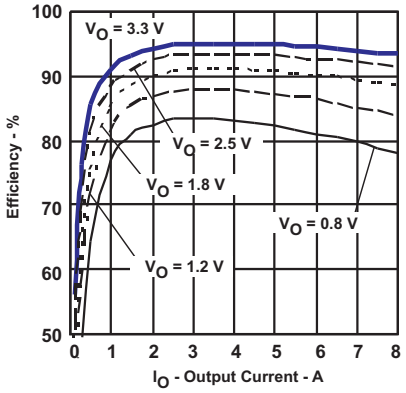


Figure 1.

OUTPUT VOLTAGE RIPPLE vs OUTPUT CURRENT

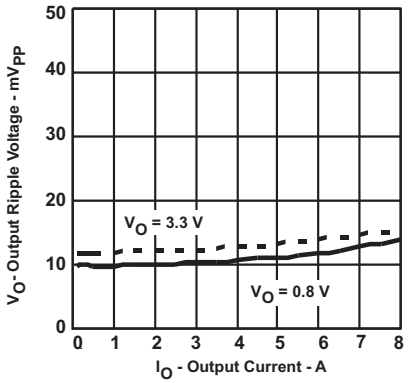


Figure 2.

POWER DISSIPATION vs OUTPUT CURRENT

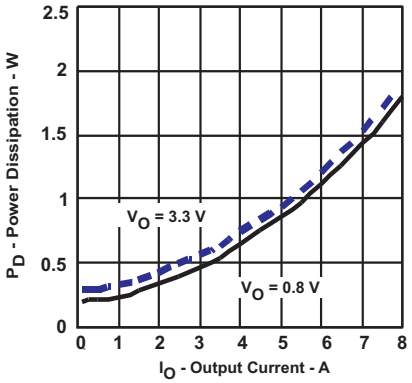


Figure 3.

TEMPERATURE DERATING vs OUTPUT CURRENT

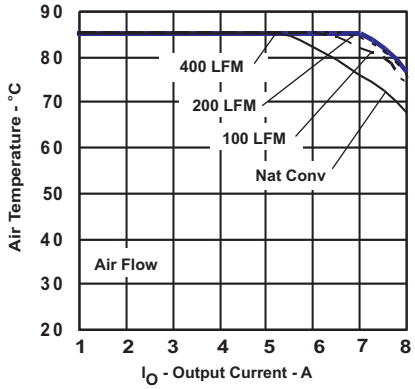


Figure 4.

(8) The electrical characteristic data has been developed from actual products tested at 25C. This data is considered typical for the converter. Applies to Figure 1, Figure 2, and Figure 3.

(9) The temperature derating curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. The airflow direction is parallel to the long axis of the module. Derating limits apply to modules soldered directly to a 100 mm x 100 mm, double-sided PCB with 2 oz. copper. Applies to Figure 4.

DEVICE INFORMATION

TERMINAL FUNCTIONS

TERMINAL		DESCRIPTION
NAME	NO.	
V_I	8	The positive input voltage power node to the module, which is referenced to common GND.
V_O	2, 3	The regulated positive power output with respect to the GND node.
GND	1, 6	This is the common ground connection for the V_I and V_O power connections. It is also the 0-Vdc reference for the control inputs. Both pins must be connected to common ground.
Inhibit	7	The Inhibit pin is an open-collector/drain, active-low input that is referenced to GND. Applying a low-level ground signal to this input disables the module's output and turns off the output voltage. When the Inhibit control is active, the input current drawn by the regulator is significantly reduced. If the inhibit feature is not used, the control pin should be left open-circuit. The module then produces an output voltage whenever a valid input source is applied.
V_o Adjust	4	A 1% or 0.5% resistor must be connected directly between this pin and GND (pin 1 is recommended) to set the output voltage of the module higher than its lowest value. The temperature stability of the resistor should be 100 ppm/°C (or better). The set-point range is 0.8 V to 3.6 V. The resistor value can be calculated using a formula. If this input is left open-circuit, the output voltage defaults to its lowest value. For further information, consult the related application note. *The specification table gives the standard resistor values for a number of common output voltages.*
Track	5	This is an analog control input that enables the output voltage to follow an external voltage. This pin becomes active typically 20 ms after the input voltage has been applied, and allows direct control of the output voltage from 0 V up to the nominal set-point voltage. Within this range, the output follows the voltage at the Track pin on a volt-for-volt basis. When the control voltage is raised above this range, the module regulates at its set-point voltage. The feature allows the output voltage to rise simultaneously with other modules powered from the same input bus. If unused, this input should be connected to V_I. *NOTE: Due to the undervoltage lockout feature, the output of the module cannot follow its own input voltage during power up. Consult the related Application Information for further guidance.*

Front View of Module

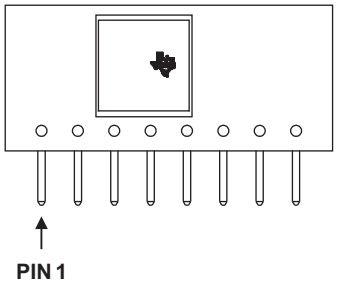


Figure 5. Pin Terminal Locations

APPLICATION INFORMATION

Capacitor Recommendations for the PTV05010W Power Module

Input Capacitors

The required input capacitors are a 10-µF ceramic and a minimum of 100-µF electrolytic type. The 100-µF capacitance must be rated for 300 mArms ripple current capability. See Table 1.

The above ripple current requirements are *conditional* that the 10-µF ceramic capacitor is present. The 10-µF X5R/X7R ceramic capacitor is necessary to reduce both the magnitude of ripple current through the electroytic capacitor and the amount of ripple current reflected back to the input source. Ceramic capacitors should be located within 0.5 inch. (1,3 cm) of the module's input pins. Additional ceramic capacitors can be added to reduce the RMS ripple current requirement for the electrolytic capacitor.

Ripple current (rms) rating, less than 150-mΩ equivalent series resistance (ESR), and temperature are the major considerations when selecting input capacitors. Unlike polymer-tantalum capacitors, regular tantalum capacitors have a recommended minimum voltage rating of 2 × (max. dc voltage + ac ripple). This is standard practice to ensure reliability. Only a few tantalum capacitors were found to have sufficient voltage rating to meet this requirement. At temperatures below 0°C, the ESR of aluminum electrolytic capacitors increases. For these applications, Os-Con, polymer-tantalum, and polymer-aluminum types should be considered.

Output Capacitor (Optional)

For applications with load transients (sudden changes in load current), regulator response benefits from external output capacitance. The recommended output capacitance of 100 µF allows the module to meet its transient response specification. For most applications, a high-quality computer-grade aluminum electrolytic capacitor is adequate. These capacitors provide decoupling over the frequency range, 2 kHz to 150 kHz, and are suitable when ambient temperatures are above 0°C. For operation below 0°C, tantalum-, ceramic-, or Os-Con-type capacitors are recommended. When using one or more nonceramic capacitors, the calculated equivalent ESR should be no lower than 4 mΩ (7 mΩ using the manufacturer's maximum ESR for a single capacitor). A list of preferred low-ESR-type capacitors are identified in Table 1.

Ceramic Capacitors

Above 150 kHz, the performance of aluminum electrolytic capacitors is less effective. Multilayer ceramic capacitors have low ESR and a resonant frequency higher than the bandwidth of the regulator. They can be used to reduce the reflected ripple current at the input as well as improve the transient response of the output. When used on the output, their combined ESR is not critical as long as the total value of ceramic capacitance does not exceed approximately 300 µF. Also, to prevent the formation of local resonances, do not place more than five identical ceramic capacitors in parallel with values of 10 µF or greater.

Tantalum Capacitors

Tantalum-type capacitors can only be used on the output bus, and are recommended for applications where the ambient operating temperature can be less than 0°C. The AVX TPS, Sprague 593D/594/595 and Kemet T495/T510 capacitor series are suggested over many other tantalum types due to their higher rated surge, power dissipation, and ripple current capability. As a caution, many general-purpose tantalum capacitors have considerably higher ESR, reduced power dissipation, and lower ripple current capability. These capacitors are also less reliable as they have reduced power dissipation and surge current ratings. Tantalum capacitors that have no stated ESR or surge current rating are not recommended for power applications.

When specifying Os-con and polymer tantalum capacitors for the output, the minimum ESR limit is encountered before the maximum capacitance value is reached.

Capacitor Table

Table 1 identifies the characteristics of capacitors from a number of vendors with acceptable ESR and ripple current (rms) ratings. The recommended number of capacitors required at both the input and output buses is identified for each capacitor type.

Note: *This is not an extensive capacitor list. Capacitors from other vendors are available with comparable specifications. Those listed are for guidance. The RMS ripple current rating and ESR (at 100 kHz) are critical parameters necessary to ensure both optimum regulator performance and long capacitor life.*

Table 1. Input/Output Capacitors(1)

Capacitor Vendor, Type/Series (Style)	Capacitor Characteristics					Quantity		Vendor Part Number
	Working Voltage (V)	Value (µF)	Max ESR at 100 kHz (Ω)	Max Ripple Current at 85°C (Irms) (mA)	Physical Size (mm)	Input Bus	Optional Output Bus	
Panasonic, Aluminum	10	330	0.117	555	8 × 11.5	1	1	EEUFC1A331
FC(Radial)	16	220	0.117	117	8 × 11,5	1	1	EEUFC1C221
FK (SMD)	6.3	470	0.16	600	8 × 10.2	1	1	EEVFK0J471P
United Chemi-Con								
PSA,Poly-Alum (Radial)	6.3	220	0.02	3160	6.3 × 9.8	1	≤ 3	PSA6.3VB220MF11
LXZ, Alum (Radial)	10	470	0.12	555	8 × 125	1	1	LXZ10VB471M8X12LL
MVZ, Alum (SMD)	16	680	0.09	670	10 × 10	1	1	MVZ16VC681MJ10TP
PXA, Poly-Alum (SMD)	10	120	0.027	2800	8 × 6,7	1	≤3	PXA10VC121MH70TP
Nichicon, Aluminum	16	270	0.09	575	10 × 12,5	1	1	UPM1C271MHH6
HD (Radial)	10	470	0.072	760	8 × 11,5	1	1	UHD1A471MPR
Sanyo								
TP, Poscap	10	220	0.025	2400	7.3 × 4.3	1	≤ 2	10TPE220M
SEQP, Os-Con (Radial)	10	120	0.035	>2500	8 × 7	1	≤ 5	10SEQP120M
SVP, Os-Con (SMD)	6.3	100	0.04	1810	6.3 × 6,0	1	≤ 4	6SVP100M
AVX, Tantalum, Ser III	10	100	0.075	>1090	7.3 × 5.7 × 4.1	N/R	≤ 4	TPSC107M010R0075
TPS (SMD)	10	150	0.05	>1559	7.3 × 5.7 × 4.1	N/R	≤ 4	TPSD157M010R0050
Kemet (SMD)								
T520, Poly-Tant	10	100	0.055	1500	7.3 × 4.3 × 4	1	≤ 4	T520D107M010ASE055
T530, Poly-Tant/Organic	10	330	0.01	>3800	7.3 × 4.3 × 4	1	≤ 1	T530X337M010ASE010
Vishay-Sprague 94SVP	10	120	0.04	2120	8 ×7	1	≤ 3	94SVP127X0010E7
595D, Tantalum (SMD)	10	220	0.14	1040	7.5 × 4.3 × 4.1	1	≤ 4	595D227X0010D2T
94SA, Os-Con (Radial)	10	100	0.03	2670	10 × 10.5	1	≤ 3	94SA107X0010EBP
Kemet, Ceramic X5R	16	10	0.002	—	3225	≥1 (2)	≤ 5	C1210C106M4PAC
(SMD)	6.3	22	0.002		3225	≥1 (2)	≤ 5	C1210C226K9PAC
	6.3	47	0.002		3225	≥1(2)	≤ 5	C1210C476K9PAC
Murata, Ceramic X5R	6.3	100	0.002	—	3225	≥1(2)	≤ 3	GRM32ER60J107M
(SMD)	6.3	47				≥1(2)	≤ 5	GRM32ER60J476M
	16	22				≥1 (2)	≤ 5	GRM32ER61C226K
	16	10				≥1 (2)	≤ 5	GRM32DR61C106K
TDK, Ceramic X5R	6.3	100	0.002	—	3225	≥1(2)	≤ 3	C3225X5R0J107MT
(SMD)	6.3	47				≥1 (2)	≤ 5	C3225X5R0J476MT
	16	22				≥1 (2)	≤ 5	C3225X5R1C226MT
	16	10				≥1 (2)	≤ 5	C3225X5R1C106MT

(1) **Capacitor Supplier Verification**
Please verify availability of capacitors identified in this table. Capacitor suppliers may recommend alternative part numbers because of limited availability or obsolete products. In some instances, the capacitor product life cycle may be in decline and have short-term consideration for obsolescence.
RoHS, Lead-free and Material Details
Please consult capacitor suppliers regarding material composition, RoHS status, lead-free status, and manufacturing process requirements. Component designators or part number deviations can occur when material composition or soldering requirements are updated.

(2) Ceramic capacitors are required to complement electrolytic types at the input and to reduce high-frequency ripple current.

Designing for Fast Load Transients

The transient response of the dc/dc converter has been characterized using a load transient with a di/dt of 1 A/µs. The typical voltage deviation for this load transient is given in the data sheet specification table using the optional value of output capacitance. As the di/dt of a transient is increased, the response of a converter regulation circuit ultimately depends on its output capacitor decoupling network. This is an inherent limitation with any dc/dc converter once the speed of the transient exceeds its bandwidth capability. If the target application specifies a higher di/dt or lower voltage deviation, the requirement can only be met with additional output capacitor decoupling. In these cases, special attention must be paid to the type, value, and ESR of the capacitors selected.

If the transient performance requirements exceed that specified in the data sheet, or the total amount of load capacitance is above 3000 µF, the selection of output capacitors becomes more important.

Adjusting the Output Voltage

The *V_O Adjust* control (pin 4) sets the output voltage of the PTV05010W product to a value over the range, 0.8 V to 3.6 V. The adjustment method requires the addition of a single external resistor, R_{SET}, that must be connected directly between the V_O Adjust and the regulator's output GND (pin 1 is recommended). Without an adjust resistor, the output voltage is set to its lowest value. Table 2 gives the preferred value of the external resistor for a number of standard voltages, along with the actual output voltage that this resistance value provides. Figure 6 shows the placement of the required resistor.

Table 2. Nearest Standard Values of R_{SET} for Common Output Voltages

V_O (Required)	R_{SET} (Standard Value)	V_O (Actual)
3.3 V	698 Ω	3.309 V
2.5 V	2.21 kΩ	2.502 V
2 V	4.12 kΩ	2.010 V
1.8 V	5.49 kΩ	1.803 V
1.5 V	8.87 kΩ	1.504 V
1.2 V	17.4 kΩ	1.202 V
1 V	36.5 kΩ	1.005 V
0.8 V	Open	0.800 V

For other output voltages, the value of the required resistor can either be calculated or simply selected from the range of values given in Table 3. Equation 1 may be used for calculating the adjust resistor value.

$$R_{SET} = 10\ k\Omega \times \frac{0.8\ V}{V_O - 0.8\ V} - 2.49\ k\Omega \quad (1)$$

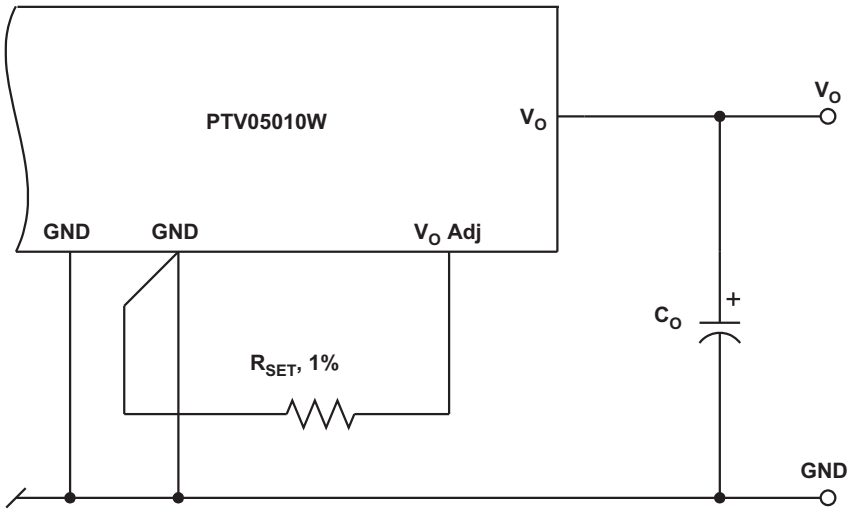


Figure 6. V_O Adjust Resistor Placement

Table 3. Calculated Values of R_{SET} for Other Output Voltages

V_O	R_{SET}	V_O	R_{SET}	V_O	R_{SET}
0.800	Open	1.450	9.82 kΩ	2.550	2.08 kΩ
0.825	318 kΩ	1.500	8.94 kΩ	2.600	1.95 kΩ
0.850	158 kΩ	1.550	8.18 kΩ	2.650	1.83 kΩ
0.875	104 kΩ	1.600	7.51 kΩ	2.700	1.72 kΩ
0.900	77.5 kΩ	1.650	6.92 kΩ	2.750	1.61 kΩ
0.925	61.5 kΩ	1.700	6.40 kΩ	2.800	1.51 kΩ
0.950	50.8 kΩ	1.750	5.93 kΩ	2.850	1.41 kΩ
0.975	43.2 kΩ	1.800	5.51 kΩ	2.900	1.32 kΩ
1.000	37.5 kΩ	1.850	5.13 kΩ	2.950	1.23 kΩ
1.025	33.1 kΩ	1.900	4.78 kΩ	3.000	1.15 kΩ
1.050	29.5 kΩ	1.950	4.47 kΩ	3.050	1.07 kΩ
1.075	26.6 kΩ	2.000	4.18 kΩ	3.100	998 Ω
1.100	24.2 kΩ	2.050	3.91 kΩ	3.150	914 Ω
1.125	22.1 kΩ	2.100	3.66 kΩ	3.200	843 Ω
1.150	20.4 kΩ	2.150	3.44 kΩ	3.250	775 Ω
1.175	18.8 kΩ	2.200	3.22 kΩ	3.300	710 Ω
1.200	17.5 kΩ	2.250	3.03 kΩ	3.350	647 Ω
1.225	16.3 kΩ	2.300	2.84 kΩ	3.400	587 Ω
1.250	15.3 kΩ	2.350	2.67 kΩ	3.450	529 Ω
1.300	13.5 kΩ	2.400	2.51 kΩ	3.500	473 Ω
1.350	12.1 kΩ	2.450	2.36 kΩ	3.550	419 Ω
1.400	10.8 kΩ	2.500	2.22 kΩ	3.600	367 Ω

Features of the PTH/PTV Family of Non-Isolated, Wide-Output Adjust Power Modules

POLA™ Compatibility

The PTH/PTV family of non-isolated, wide-output adjustable power modules from Texas Instruments are optimized for applications that require a flexible, high-performance module that is small in size. Each of these products are POLA™ compatible. POLA-compatible products are produced by a number of manufacturers, and offer customers advanced, non-isolated modules with the same footprint and form factor. POLA parts are also ensured to be interoperable, thereby providing customers with true second-source availability.

Soft-Start Power Up

The Auto-Track feature allows the power up of multiple PTH/PTV modules to be directly controlled from the Track pin. However, in a stand-alone configuration, or when the Auto-Track feature is not being used, the *Track* pin should be directly connected to the input voltage, V_I (see Figure 7).

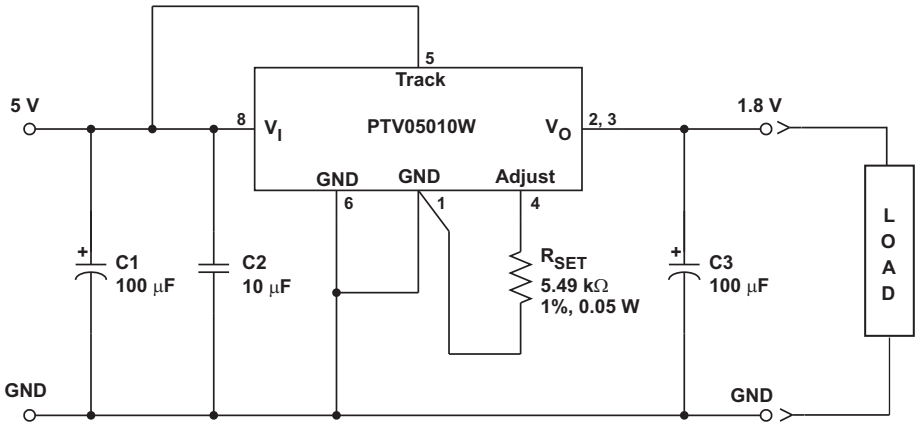


Figure 7. Power-Up Application Circuit

When the *Track* pin is connected to the input voltage, the Auto-Track function is permanently disengaged. This allows the module to power up entirely under the control of its internal soft-start circuitry. When power up is under soft-start control, the output voltage rises to the set-point at a quicker and more linear rate.

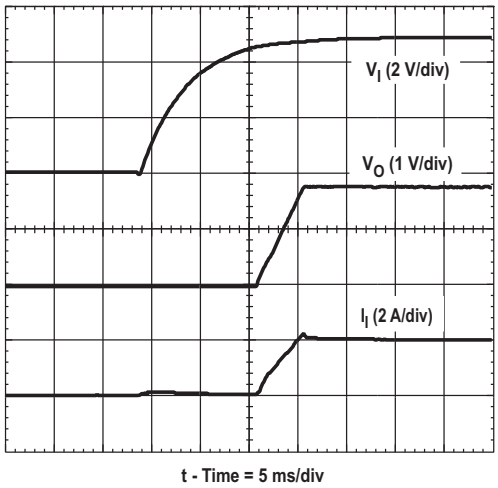


Figure 8. Power-Up Waveform

From the moment a valid input voltage is applied, the soft-start control introduces a short time delay (typically 8ms to 15ms) before allowing the output voltage to rise. The output then progressively rises to the module set-point voltage. Figure 8 shows the soft-start power-up characteristic of the PTV05010W, operating from a 5-V input bus and configured for a 1.8-V output. The waveforms were measured with a 5-A resistive load and the Auto-Track feature disabled. The initial rise in input current when the input voltage first starts to rise is the charge current drawn by the input capacitors. Power up is complete within 25 ms.

Overcurrent Protection (OCP)

For protection against load faults, the modules incorporate output overcurrent protection. Applying a load that exceeds the overcurrent threshold causes the regulated output to shut down. Following shutdown, a module periodically attempts to recover by initiating a soft-start power up. This is described as a *hiccup* mode of operation, whereby the module continues in the cycle of successive shutdown and power up until the load fault is removed. During this period, the average current flowing into the fault is significantly reduced. Once the fault is removed, the module automatically recovers and returns to normal operation.

Output On/Off Inhibit

For applications requiring output voltage on/off control, the modules incorporate an output Inhibit control pin. The inhibit feature can be used wherever there is a requirement for the output voltage from the regulator to be turned off.

The power modules function normally when the *Inhibit* input is left open-circuit, providing a regulated output whenever a valid source voltage is connected to V_I with respect to GND.

Figure 9 shows the typical application of the inhibit function. Note the discrete transistor (Q1). The *Inhibit* input has its own internal pullup (see footnotes to electrical characteristics table). The input is not compatible with TTL logic devices. An open-collector (or open-drain) discrete transistor is recommended for control.

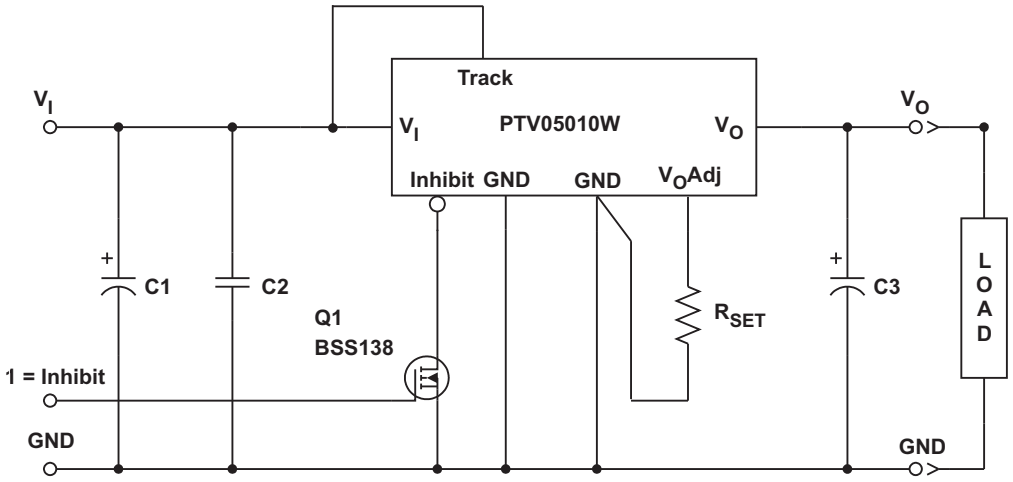


Figure 9. On/Off Inhibit Application Circuit

Turning Q1 on applies a low voltage to the Inhibit control and disables the output of the module. If Q1 is then turned off, the module executes a soft-start power-up sequence. A regulated output voltage is produced within 25ms. Figure 10 shows the typical rise in both the output voltage and input current, following the turnoff of Q1. The turnoff of Q1 corresponds to the rise in the waveform, Q1 V_{DS}. The waveforms were measured with a 5-A constant current load.

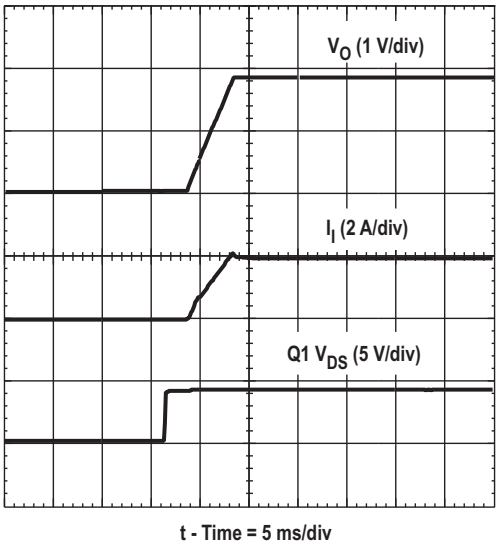


Figure 10. Inhibit Waveform

Auto-Track™ Function

The Auto-Track function is unique to the PTH/PTV family, and is available with all POLA products. Auto-Track was designed to simplify the amount of circuitry required to make the output voltage from each module power up and power down in sequence. The sequencing of two or more supply voltages during power up is a common requirement for complex mixed-signal applications that use dual-voltage VLSI ICs such as the TMS320™ DSP family, microprocessors, and ASICs.

How Auto-Track™ Works

Auto-Track works by forcing the module output voltage to follow a voltage presented at the *Track* control pin (1). This control range is limited to between 0 V and the module set-point voltage. Once the track-pin voltage is raised above the set-point voltage, the module output remains at its set-point (2). As an example, if the *Track* pin of a 2.5-V regulator is at 1 V, the regulated output is 1 V. If the voltage at the *Track* pin rises to 3 V, the regulated output does not go higher than 2.5 V.

Under Auto-Track control, the regulated output from the module follows the voltage at its *Track* pin on a volt-for-volt basis. By connecting the *Track* pin of a number of these modules together, the output voltages follow a common signal during power up and power down. The control signal can be an externally generated master ramp waveform, or the output voltage from another power supply circuit (3). For convenience, the *Track* input incorporates an internal RC-charge circuit. This operates off the module input voltage to produce a suitable rising waveform at power up.

Typical Auto-Track™ Application

The basic implementation of Auto-Track allows for simultaneous voltage sequencing of a number of Auto-Track compliant modules. Connecting the *Track* inputs of two or more modules forces their track input to follow the same collective RC-ramp waveform, and allows their power-up sequence to be coordinated from a common track control signal. This can be an open-collector (or open drain) device, such as a power-up reset voltage supervisor IC. See U3 in Figure 11.

To coordinate a power-up sequence, the Track control must first be pulled to ground potential. This should be done at or before input power is applied to the modules. The ground signal should be maintained for at least 20 ms after input power has been applied. This brief period gives the modules time to complete their internal soft-start initialization (4), enabling them to produce an output voltage. A low-cost supply voltage supervisor IC, that includes a built-in time delay, is an ideal component for automatically controlling the track inputs at power up.

Figure 11 shows how the TPS3808G50 supply voltage supervisor IC (U3) can be used to coordinate the sequenced power-up of two 5-V input Auto-Track modules. The output of the TPS3808G50 supervisor becomes active above an input voltage of 0.8 V, enabling it to assert a ground signal to the common track control well before the input voltage has reached the module's undervoltage lockout threshold. The ground signal is maintained until approximately 27 ms after the input voltage has risen above U3's voltage threshold, which is 4.65 V. The 27-ms time period is controlled by the capacitor C3. The value of 4700 pF provides sufficient time delay for the modules to complete their internal soft-start initialization. The output voltage of each module remains at zero until the track control voltage is allowed to rise. When U3 removes the ground signal, the track control voltage automatically rises. This causes the output voltage of each module to rise simultaneously with the other modules, until each reaches its respective set-point voltage.

Figure 12 shows the output voltage waveforms from the circuit of Figure 11 after input voltage is applied to the circuit. The waveforms, V_O1 and V_O2 represent the output voltages from the two power modules, U1 (3.3 V) and U2 (1.8 V), respectively. V_{TRK}, V_O1, and V_O2 are shown rising together to produce the desired simultaneous power-up characteristic.

The same circuit also provides a power-down sequence. When the input voltage falls below U3's voltage threshold, the ground signal is reapplied to the common track control. This pulls the track inputs to zero volts, forcing the output of each module to follow, as shown in Figure 13. In order for a simultaneous power-down to occur, the track inputs must be pulled low before the input voltage has fallen below the modules' undervoltage lockout. This is an important constraint. Once the modules recognize that a valid input voltage is no longer present, their outputs can no longer follow the voltage applied at their track input. During a power-down sequence, the fall in the output voltage from the modules is limited by the maximum output capacitance and the Auto-Track slew rate. If the *Track* pin is pulled low at a slew rate greater than 1 V/ms, the discharge of the output capacitors will induce large currents which could exceed the peak current rating of the module. This will result in a reduction in the maximum allowable output capacitance as listed in the Electrical Characteristics table. When controlling the *Track* pin of the PTV05010W using a voltage supervisor IC, the slew rate is increased, therefore $C_O$max is reduced to 2200µF.

Notes on Use of Auto-Track™

1. The Auto-Track function tracks almost any voltage ramp during power up, and is compatible with ramp speeds of up to 1 V/ms.
2. The *Track* pin voltage must be allowed to rise above the module set-point voltage before the module regulates at its adjusted set-point voltage.
3. The absolute maximum voltage that may be applied to the *Track* pin is the input voltage V_I.
4. The module cannot follow a voltage at its track control input until it has completed its soft-start initialization. This takes about 20 ms from the time that a valid voltage has been applied to its input. During this period, it is recommended that the *Track* pin be held at ground potential.
5. The Auto-Track function is disabled by connecting the *Track* pin to the input voltage (V_I). When Auto-Track is disabled, the output voltage rises at a quicker and more linear rate after input power has been applied.

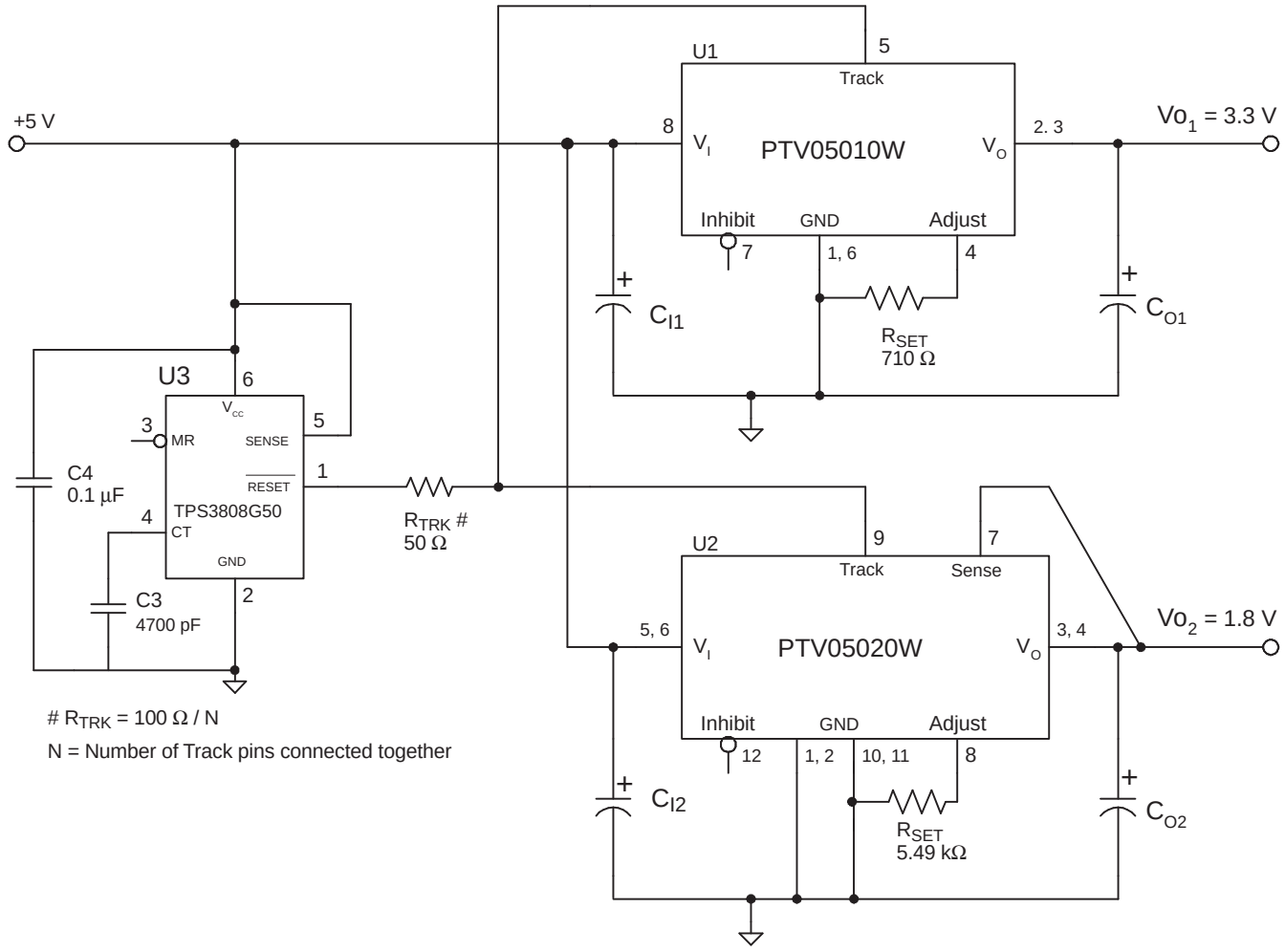
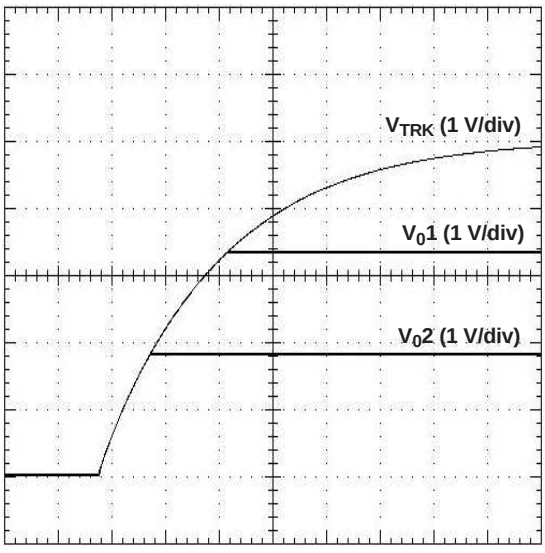
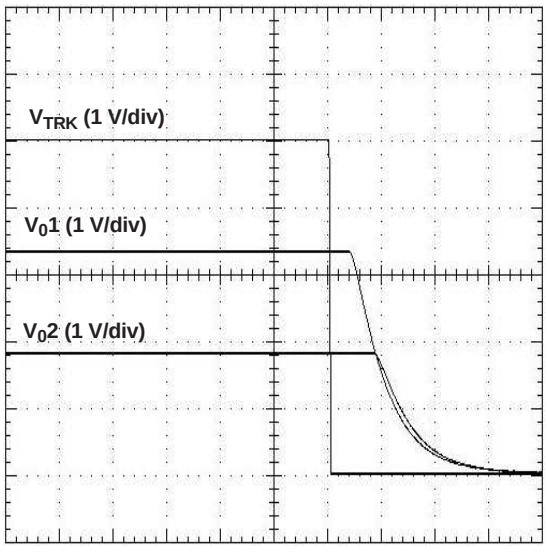


Figure 11. Sequenced Power Up and Power Down Using Auto-Track



t – Time – 20 ms/div

Figure 12. Simultaneous Power Up With Auto-Track Control



t – Time – 200 µs/div

Figure 13. Simultaneous Power Down With Auto-Track Control

Prebias Start-Up Capability

A prebias start-up condition occurs as a result of an external voltage being present at the output of a power module prior to its output becoming active. This often occurs in complex digital systems when current from another power source is backfed through a dual-supply logic component, such as an FPGA or ASIC. Another path might be via clamp diodes, sometimes used as part of a dual-supply power-up sequencing arrangement. A prebias can cause problems with power modules that incorporate synchronous rectifiers. This is because under most operating conditions, such modules can sink as well as source output current. The PTH/PTV modules incorporate synchronous rectifiers but do not sink current during start-up, or whenever the *Inhibit* pin is held low. Start-up includes an initial delay (approximately 8–15 ms), followed by the rise of the output voltage under the control of the module internal soft-start mechanism; see Figure 14.

Conditions for Prebias Holdoff

In order for the module to allow an output prebias voltage to exist (and not sink current), certain conditions must be maintained. The module holds off a prebias voltage when the *Inhibit* pin is held low, and whenever the output is allowed to rise under soft-start control. Power up under soft-start control occurs on the removal of the ground signal to the Inhibit pin (with input voltage applied), or when input power is applied with Auto-Track disabled(1). The input voltage must also be greater than the applied prebias source(2). The soft-start period is complete when the output begins rising above the prebias voltage. The module then functions as normal, and sinks current if a voltage higher than its set-point value is applied to its output.

Note: *If a prebias condition is not present, the soft-start period is complete when the output voltage has risen to either the set-point voltage, or the voltage applied at the module Track control pin, whichever is lowest, to its output.*

Demonstration Circuit

Figure 15 shows the start-up waveforms for the demonstration circuit shown in Figure 16. The initial rise in V_O2 is the prebias voltage, which is passed from the VCCIO to the VCORE voltage rail through the ASIC. Note that the output current from the module (I_O2) is negligible until its output voltage rises above the applied prebias.

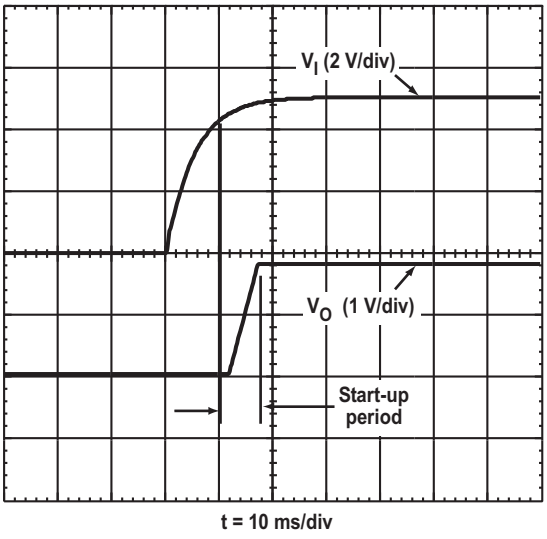


Figure 14. PTV05010W Start-Up

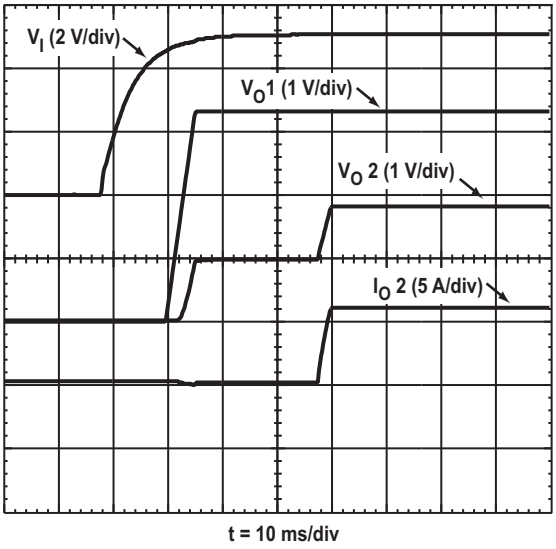


Figure 15. Prebias Start-Up Waveforms

NOTES:

1. The prebias start-up feature is not compatible with Auto-Track. If the rise in the output is limited by the voltage applied to the *Track* control pin, the output sinks current during the period that the track control voltage is below that of the back-feeding source. For this reason, Auto-Track should be disabled when not being used. This is accomplished by connecting the *Track* pin to the input voltage, V_I. This raises the *Track* pin well above the set-point voltage prior to start-up, thereby defeating the Auto-Track feature.
2. To further ensure that the regulator output does not sink current when power is first applied (even with a ground signal applied to the *Inhibit* control input), the input voltage *must* always be greater than the applied

prebias source. This condition must exist *throughout* the power-up sequence of the power system.

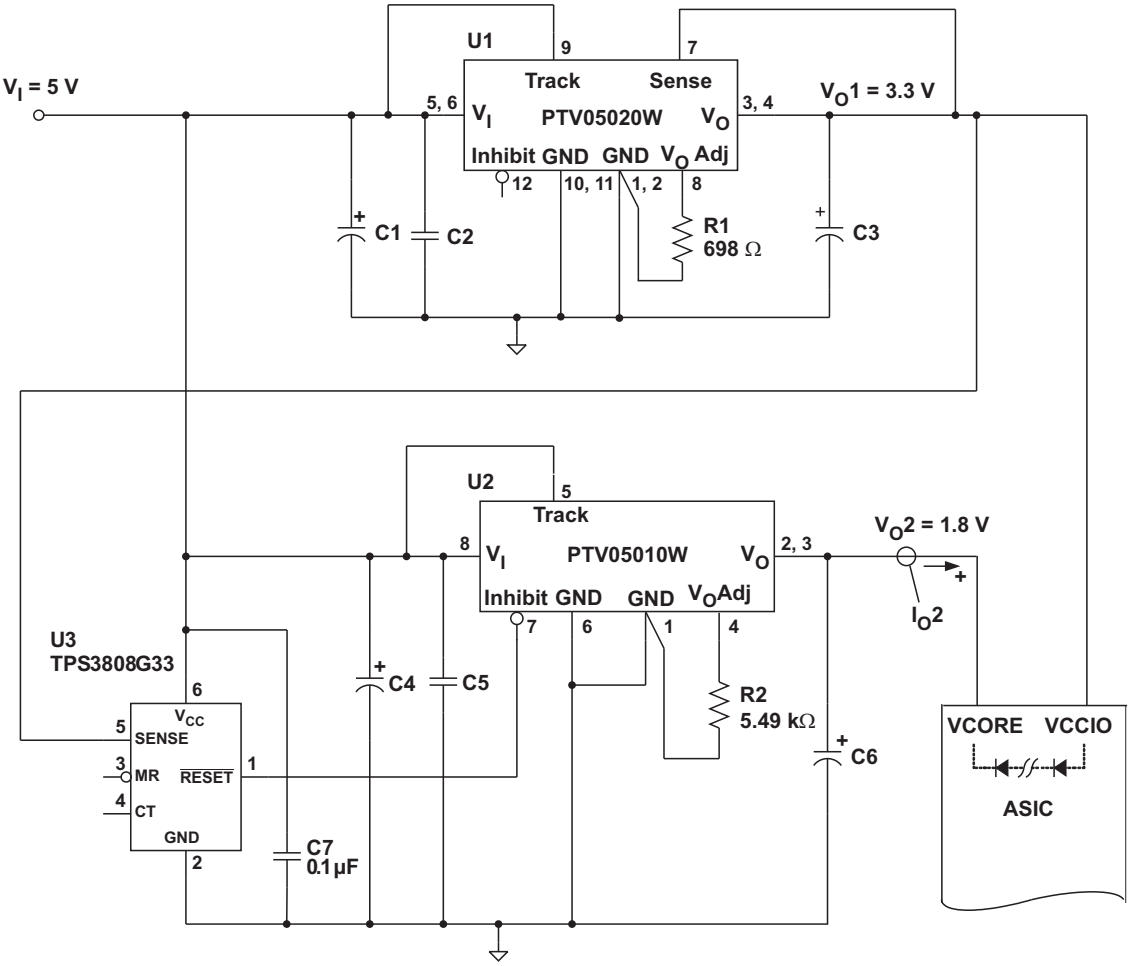


Figure 16. Application Circuit Demonstrating Prebias Start-Up

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTV05010WAH	ACTIVE	SIP MODULE	EVA	8	70	RoHS Exempt & non-Green	SN	N / A for Pkg Type	-40 to 85		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

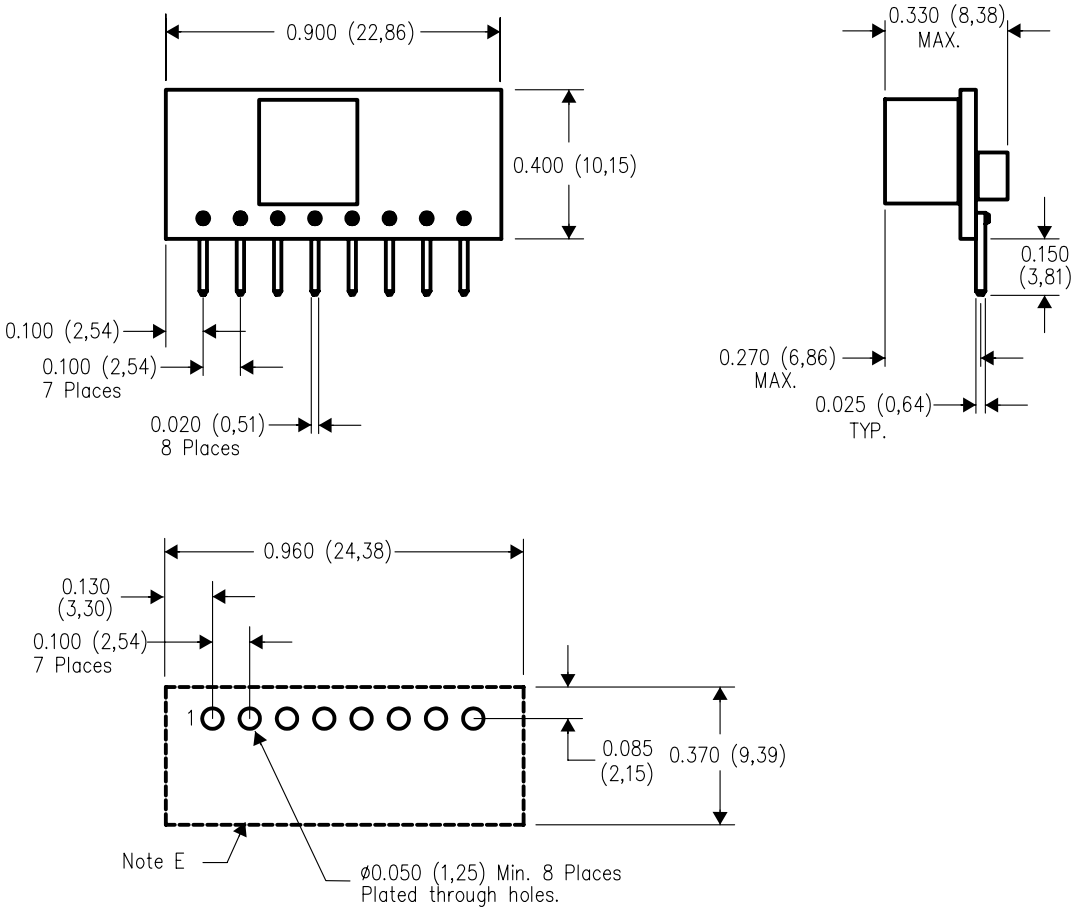
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

EVA (R–PDSS–T8) DOUBLE SIDED MODULE



PC LAYOUT

4205909/A 03/04

NOTES:
A. All linear dimensions are in inches (mm).
B. This drawing is subject to change without notice.
C. 2 place decimals are ±0.030 (±0,76mm).
D. 3 place decimals are ±0.010 (±0,25mm).
E. Recommended keep out area for user components.
F. Pins are 0.020" (0,51) x 0.025" (0,64).
G. All pins: Material – Copper Alloy
Finish – Tin (100%) over Nickel plate

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