SN74AC573 Octal D-type Transparent Latches with 3-State Outputs

1 Features

- Operation of 2V to 6V V_{CC}
- Inputs accept voltages to 6V
- Maximum t_{pd} of 9ns at 5V
- 3-State outputs drive bus lines directly

2 Applications

- Buffer registers
- Bidirectional bus drivers
- Working registers

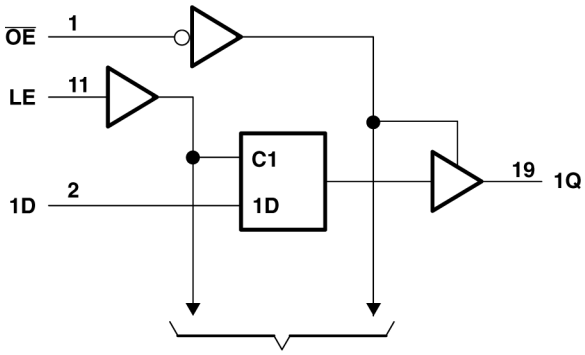
3 Description

These 8-bit latches feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. The devices are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)	BODY SIZE(3)
SN74AC573	RKS (VQFN, 20)	4.5 mm × 2.5 mm	4.5mm × 2.5mm
	DB (SSOP, 20)	7.2 mm × 7.8 mm	7.2mm x 5.30mm
	DGV (TVSOP, 20)	5 mm × 6.4 mm	5mm × 4.4mm
	DW (SOIC, 20)	12.8 mm × 10.3 mm	12.80mm x 7.50mm
	NS (SOP, 20)	12.6 mm × 7.8 mm	12.6mm x 5.3mm
	N (PDIP, 20)	24.33 mm × 9.4 mm	24.33mm x 6.35mm
	PW (TSSOP, 20)	6.5 mm × 6.4 mm	6.50mm x 4.40mm

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) The body size (length × width) is a nominal value and does not include pins.



Logic Diagram (Positive Logic)

Table of Contents

4 Pin Configuration and Functions

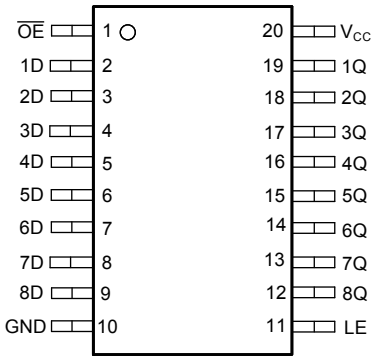


Figure 4-1. DB, DGV, DW, NS, N, or PW Packages, 20-Pin SSOP, TVSOP, SOIC, SOP, PDIP, or TSSOP (Top View)

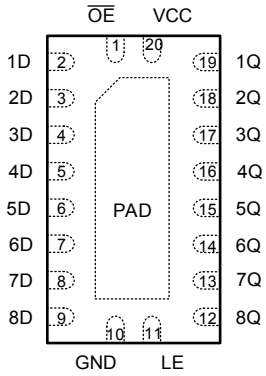


Figure 4-2. RKS Package, 20-Pin VQFN (Top View)

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
$\overline{OE}$	1	I	Output enable
1D	2	I	1D input
2D	3	I	2D input
3D	4	I	3D input
4D	5	I	4D input
5D	6	I	5D input
6D	7	I	6D input
7D	8	I	7D input
8D	9	I	8D input
GND	10	—	Ground
LE	11	I	Latch enable input
8Q	12	O	8Q output
7Q	13	O	7Q output
6Q	14	O	6Q output
5Q	15	O	5Q output
4Q	16	O	4Q output
3Q	17	O	3Q output
2Q	18	O	2Q output
1Q	19	O	1Q output
V_{CC}	20	—	Power pin
Thermal Pad[2]		—	The thermal pad can be connect to GND or left floating. Do not connect to any other signal or supply.

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.
(2) For RKS package only.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		−0.5	+ 7	V
V_I [2]	Input voltage range		−0.5	V_{CC} + 0.5	V
V_O [2]	Output voltage range		−0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	(V_I < 0 or V_I > V_{CC})		±20	mA
I_{OK}	Output clamp current	(V_O < 0 or V_O > V_{CC})		±20	mA
I_O	Continuous output current	(V_O = 0 to V_{CC})		±50	mA
	Continuous current through, V_{CC} or GND			±200	mA
T_{stg}	Storage temperature range		−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2	6	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1		V
		V_{CC} = 4.5 V	3.15		
		V_{CC} = 5.5 V	3.85		
V_{IL}	Low-level input voltage	V_{CC} = 3 V		0.9	V
		V_{CC} = 4.5 V		1.35	
		V_{CC} = 5.5 V		1.65	
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V		−12	mA
		V_{CC} = 4.5 V		−24	
		V_{CC} = 5.5 V		−24	
I_{OL}	Low-level output current	V_{CC} = 3 V		12	mA
		V_{CC} = 4.5 V		24	
		V_{CC} = 5.5 V		24	
Δt/Δv	Input transition rise or fall rate			8	ns/V
T_A	Operating free-air temperature		−40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND for proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

5.3 Thermal Information

THERMAL METRIC		SN74AC573						UNIT
		DW (SOIC)	DB (SSOP)	N (PDIP)	NS (SO)	PW (TSSOP)	RKS (VQFN)	
		20 PINS	20 PINS	20 PINS	20 PINS	20 PINS	20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance(1)	101.2	70	69	60	126.2	68	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN74AC573		UNIT
				MIN	TYP	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 µA		3 V	2.9			2.9		V
			4.5 V	4.4			4.4		
			5.5 V	5.4			5.4		
	I_{OH} = −12 mA		3 V	2.58			2.48		
	I_{OH} = −24 mA		4.5 V	3.94			3.8		
			5.5 V	4.94			4.8		
	I_{OH} = −75 mA(1)		5.5 V				3.85		
V_{OL}	I_{OL} = 50 µA		3 V			0.1		0.1	V
			4.5 V			0.1		0.1	
			5.5 V			0.1		0.1	
	I_{OL} = 12 mA		3 V			0.36		0.44	
	I_{OL} = 24 mA		4.5 V			0.36		0.44	
			5.5 V			0.36		0.44	
	I_{OL} = 75 mA		5.5 V					1.65	
I_I	V_I = V_{CC} or GND		5.5 V			±0.1		±1	µA
I_{OZ}	V_O = V_{CC} or GND		5.5 V			±0.25		±2.5	µA
I_{CC}	V_I = V_{CC} or GND,	I_O = 0	5.5 V			4		40	µA
C_i	V_I = V_{CC} or GND		5 V		5				pF

(1) Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

5.5 Timing Requirements, V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

		T_A = 25°C		SN74AC573		UNIT
		MIN	MAX	MIN	MAX	
t_w	Pulse duration, LE high	6		7		ns
t_{su}	Setup time, data before LE↓	3.5		4		ns
t_h	Hold time, data after LE↓	2		2		ns

5.6 Timing Requirements, V_{CC} = 5 V ± 0.5 V

over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

		T_A = 25°C		SN74AC573		UNIT
		MIN	MAX	MIN	MAX	
t_w	Pulse duration, LE high	4		5		ns
t_{su}	Setup time, data before LE↓	3		3.5		ns
t_h	Hold time, data after LE↓	2		2		ns

5.7 Switching Characteristics, V_{CC} = 3 V ± 0.3 V

over recommended operating free-air temperature range, V_{CC} = 3 V ± 0.3 V (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C		SN74AC573		UNIT
			MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	2.5	13	2	15	ns
t_{PHL}			2.5	12	2	14	
t_{PLH}	LE	Q	2.5	13	2	15	ns
t_{PHL}			2.5	12	2	14	
t_{PZH}	$\overline{OE}$	Q	2.5	11	2	12	ns
t_{PZL}			2.5	11	2	12.5	
t_{PHZ}	$\overline{OE}$	Q	2.5	12.5	2	13.5	ns
t_{PLZ}			2.5	9.5	2	10.5	

5.8 Switching Characteristics, V_{CC} = 5 V ± 0.5 V

over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

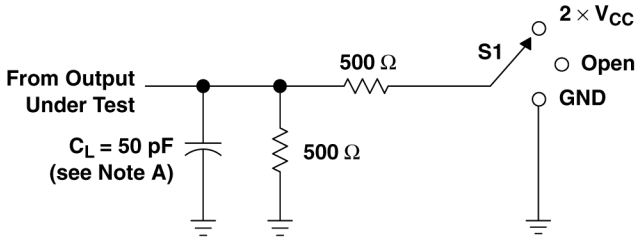
PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C		SN74AC573		UNIT
			MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	2.5	10	2	11.5	ns
t_{PHL}			2.5	9.5	2	11	
t_{PLH}	LE	Q	2.5	9.5	2	11	ns
t_{PHL}			2.5	8.5	2	10	
t_{PZH}	$\overline{OE}$	Q	2.5	9	2	10	ns
t_{PZL}			2.5	8.5	2	9.5	
t_{PHZ}	$\overline{OE}$	Q	2.5	11	2	12	ns
t_{PLZ}			2.5	8	2	9	

5.9 Operating Characteristics

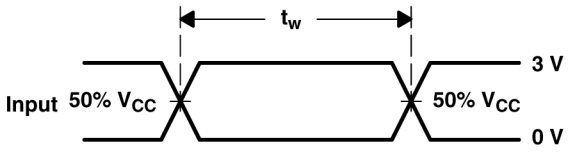
V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 1 MHz	25	pF

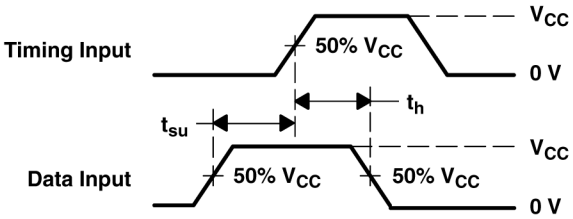
6 Parameter Measurement Information



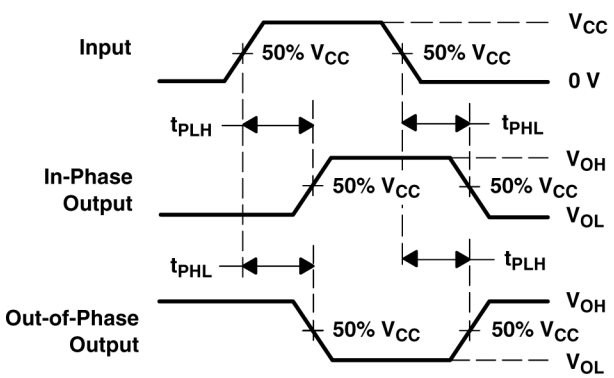
LOAD CIRCUIT



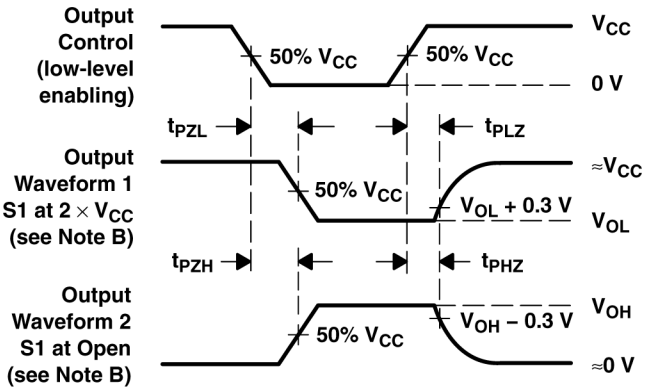
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 6-1. Load Circuit and Voltage Waveforms

Table 6-1.

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	Open

7 Detailed Description

7.1 Overview

The eight latches are D-type transparent latches. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the logic levels set up at the D Inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines in a bus-organized system without need for interface or pullup components.

$\overline{OE}$ does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

7.2 Functional Block Diagram

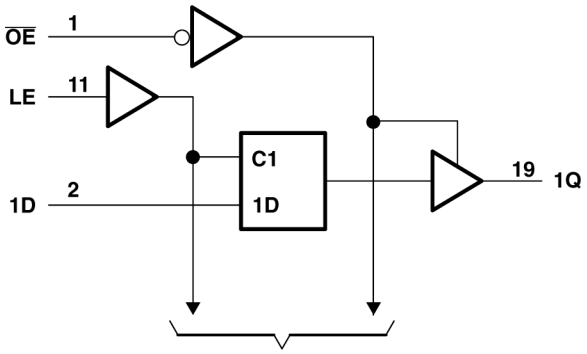


Figure 7-1. Logic Diagram (Positive Logic)

7.3 Device Functional Modes

Table 7-1. Function Table (Each Latch)

INPUTS(1)			OUTPUT(2) Q
OE	LE	D	
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

(1) H = High voltage level, L = Low voltage level, X = High or low voltage level

(2) H = Driving high, L = Driving low, Q_0 = Driving previous high or low state, Z = High impedance

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Section 5.2* table. The total current through Ground or V_{CC} must not exceed ±70 mA as per *Section 5.1* table.

Each V_{CC} pin must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends 0.1-µF capacitor; if there are multiple V_{CC} pins, then TI recommends 0.01-µF or 0.022-µF capacitor for each power pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. A 0.1-µF and 1-µF capacitor are commonly used in parallel. The bypass capacitor must be installed as close to the power pin as possible for best results.

8.2 Layout

8.2.1 Layout Guidelines

When using multiple-bit logic devices, inputs must never float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input and the gate are used, or only 3 of the 4 buffer gates are used. Such input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Layout Diagram specifies the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, they are tied to GND or V_{CC}, whichever makes more sense or is more convenient. It is acceptable to float outputs, unless the part is a transceiver. If the transceiver has an output enable pin, it disables the output section of the part when asserted. This does not disable the input section of the I/Os, so they cannot float when disabled.

8.2.2 Layout Example

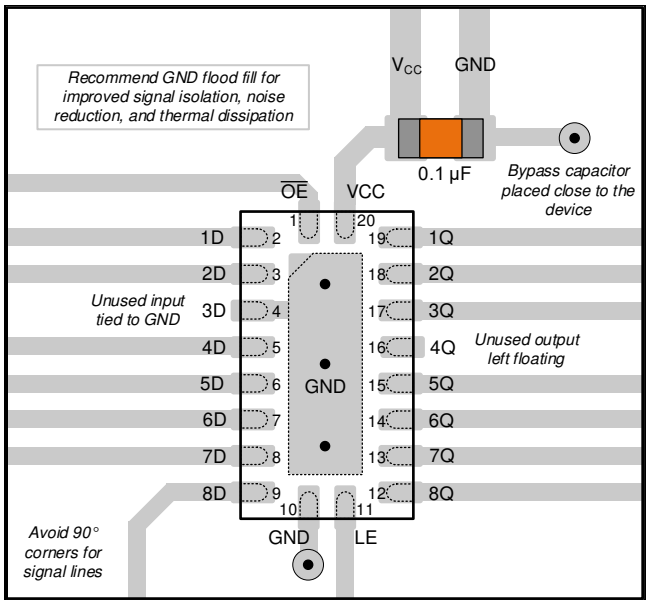


Figure 8-1. Layout example of the SN74AC573

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision G (November 2023) to Revision H (February 2024)	Page
• Added body size to *Package Information* table	1
• Updated RθJA values: DW = 58 to 101.2, PW = 83 to 126.2, all values in °C/W	5
• Added *Application and Implementation* section	9

Changes from Revision F (June 2023) to Revision G (November 2023)	Page
• Updated the *Package Information* table to include package lead size	1
• Added the *RKS* package information	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AC573DBR	ACTIVE	SSOP	DB	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC573	Samples
SN74AC573DBRG4	ACTIVE	SSOP	DB	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC573	Samples
SN74AC573DW	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI	-40 to 85	AC573	
SN74AC573DWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AC573	Samples
SN74AC573DWRG4	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC573	Samples
SN74AC573N	ACTIVE	PDIP	N	20	20	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74AC573N	Samples
SN74AC573NSR	ACTIVE	SO	NS	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC573	Samples
SN74AC573PW	OBSOLETE	TSSOP	PW	20		TBD	Call TI	Call TI	-40 to 85	AC573	
SN74AC573PWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AC573	Samples
SN74AC573PWRE4	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC573	Samples
SN74AC573RKSR	ACTIVE	VQFN	RKS	20	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AC573	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF SN74AC573 :

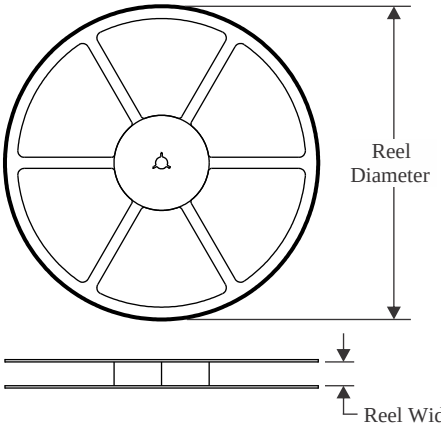
- Automotive : SN74AC573-Q1

NOTE: Qualified Version Definitions:

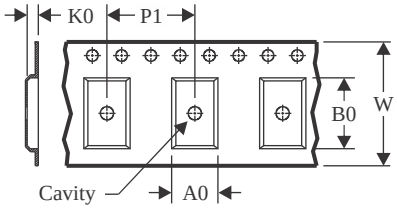
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

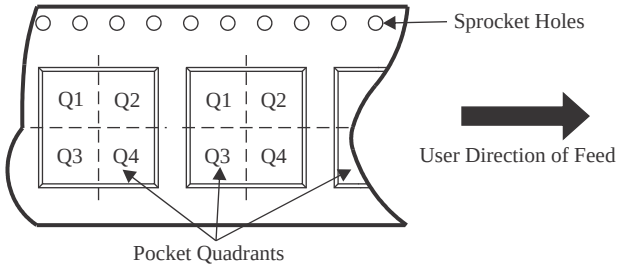


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

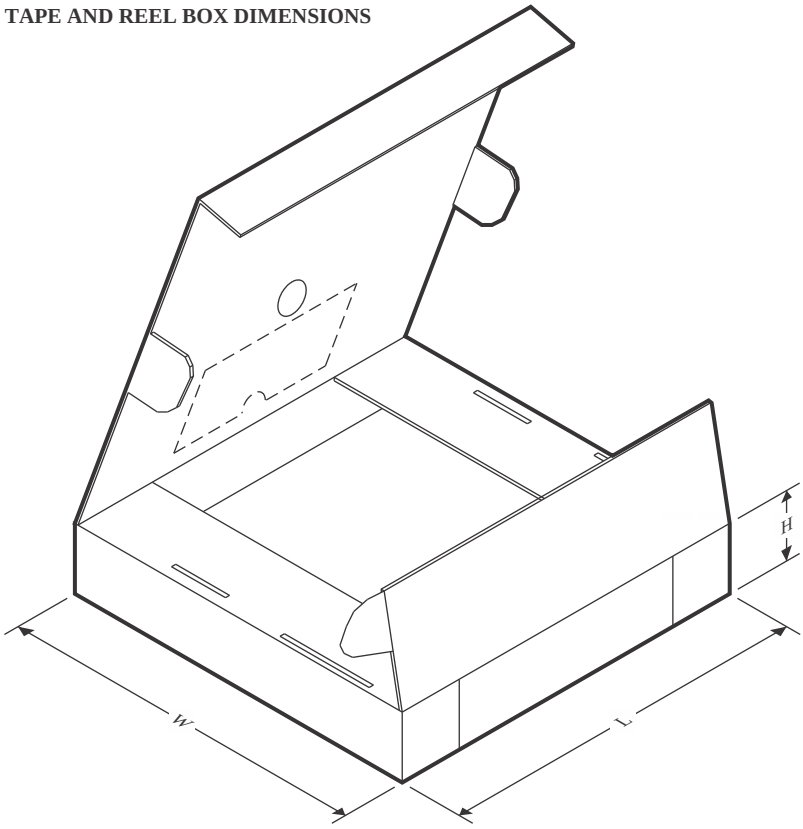
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AC573DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74AC573DWR	SOIC	DW	20	2000	330.0	24.4	10.9	13.3	2.7	12.0	24.0	Q1
SN74AC573DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74AC573NSR	SO	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74AC573PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
SN74AC573PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74AC573RKSR	VQFN	RKS	20	3000	180.0	12.4	2.8	4.8	1.2	4.0	12.0	Q1

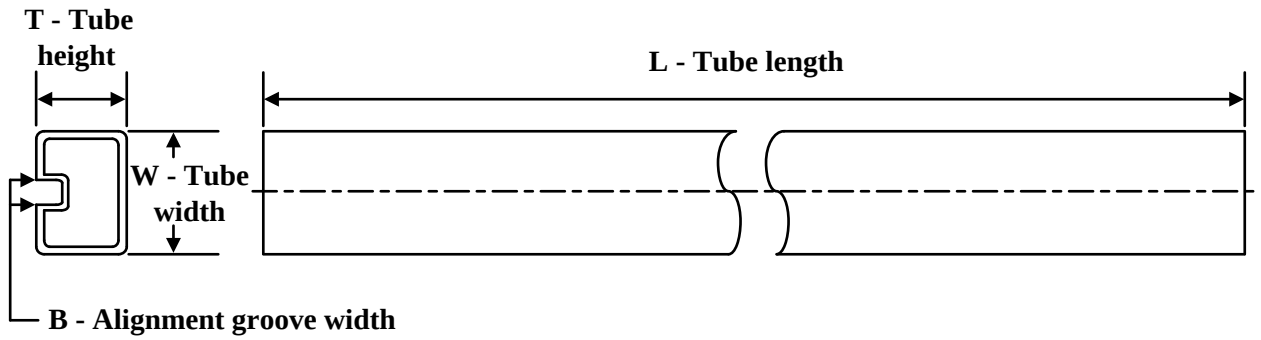
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AC573DBR	SSOP	DB	20	2000	356.0	356.0	35.0
SN74AC573DWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74AC573DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74AC573NSR	SO	NS	20	2000	367.0	367.0	45.0
SN74AC573PWR	TSSOP	PW	20	2000	356.0	356.0	35.0
SN74AC573PWR	TSSOP	PW	20	2000	353.0	353.0	32.0
SN74AC573RKSR	VQFN	RKS	20	3000	210.0	185.0	35.0

TUBE



*All dimensions are nominal

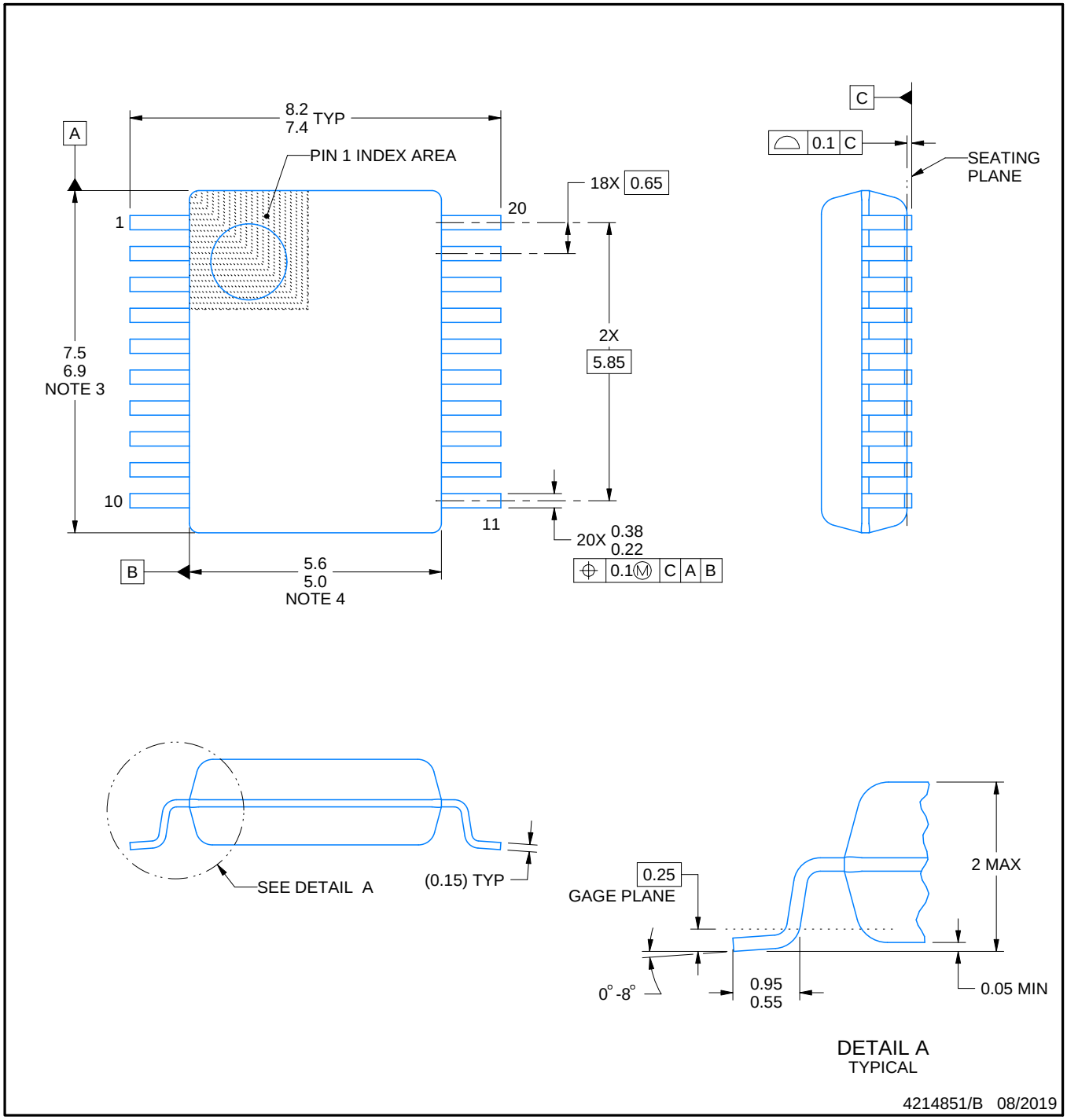
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74AC573N	N	PDIP	20	20	506	13.97	11230	4.32

PACKAGE OUTLINE

DB0020A

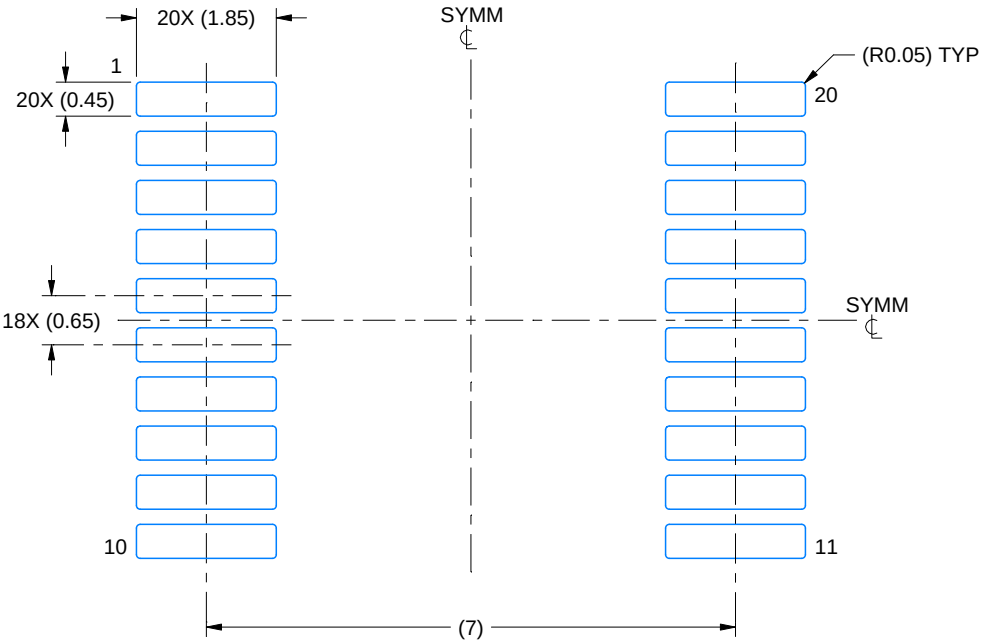
SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

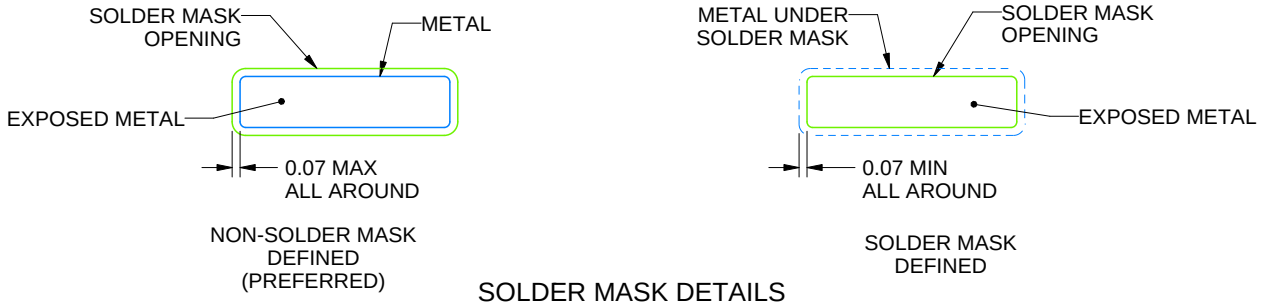


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4214851/B 08/2019

NOTES: (continued)

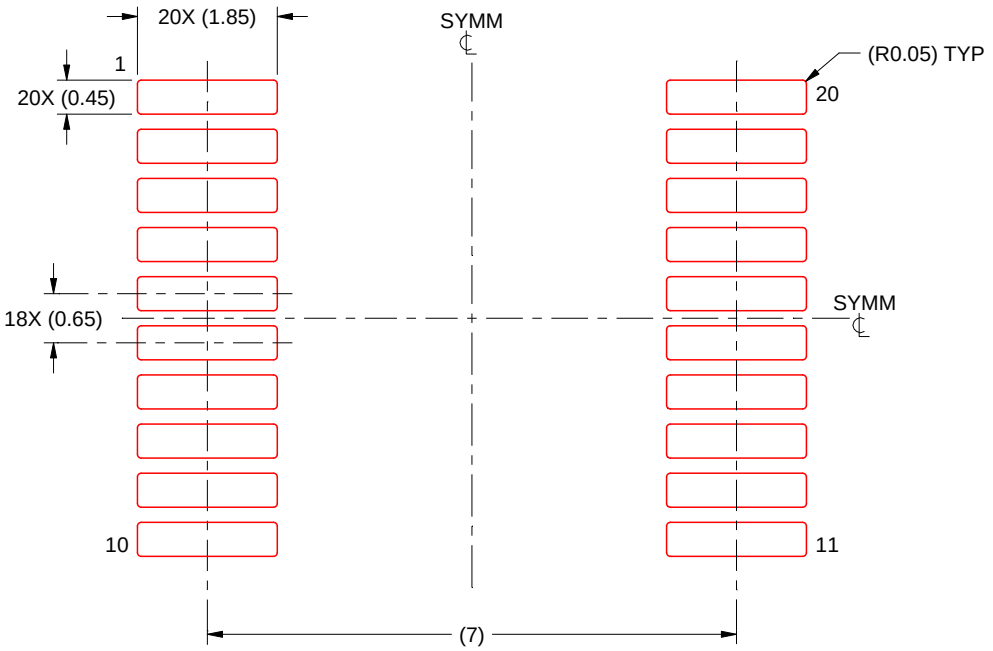
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

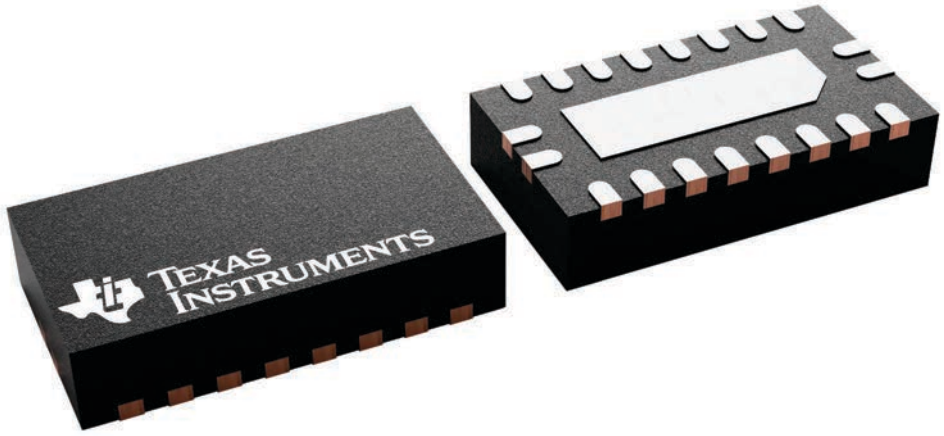
RKS 20

VQFN - 1 mm max height

2.5 x 4.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

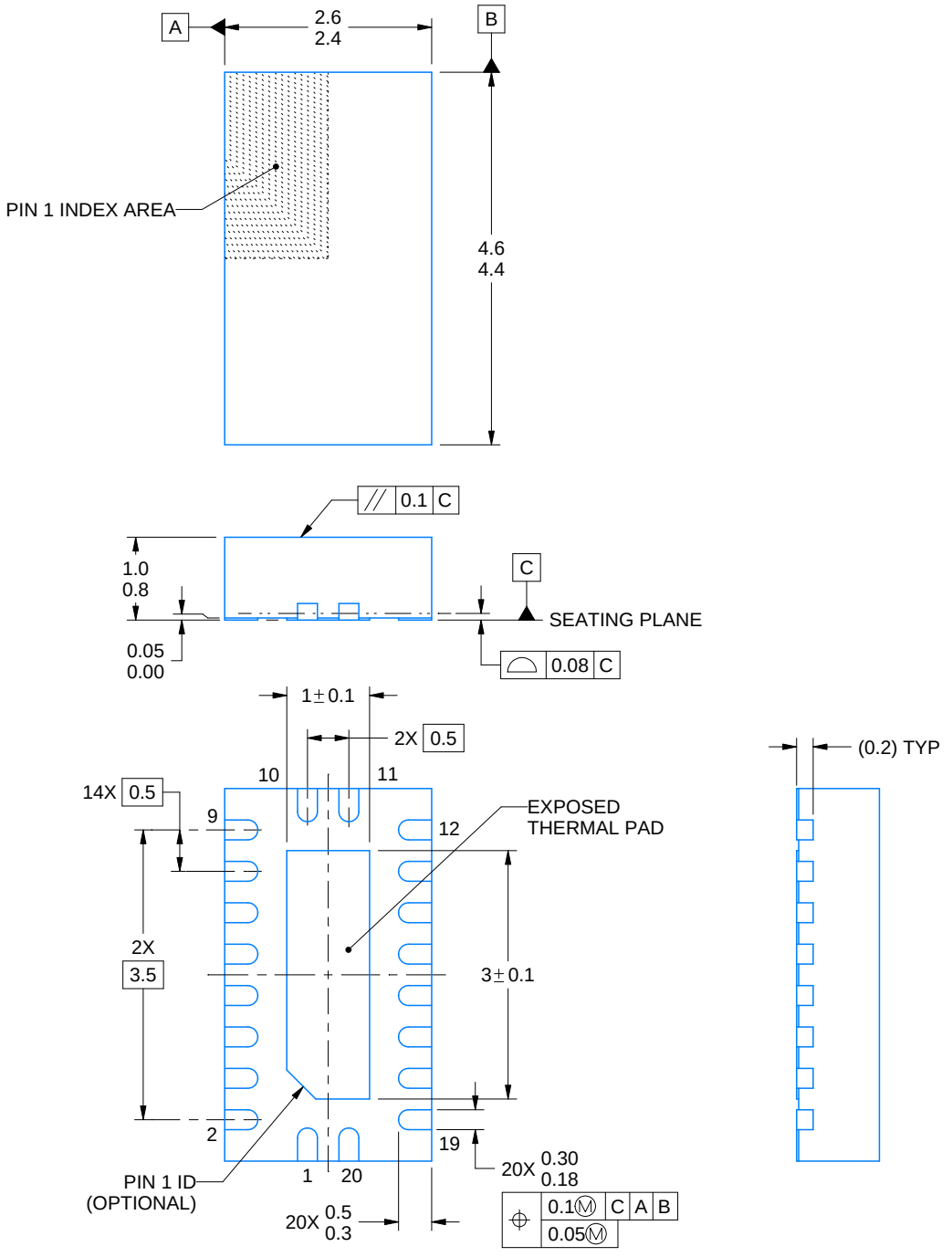


PACKAGE OUTLINE

RKS0020A

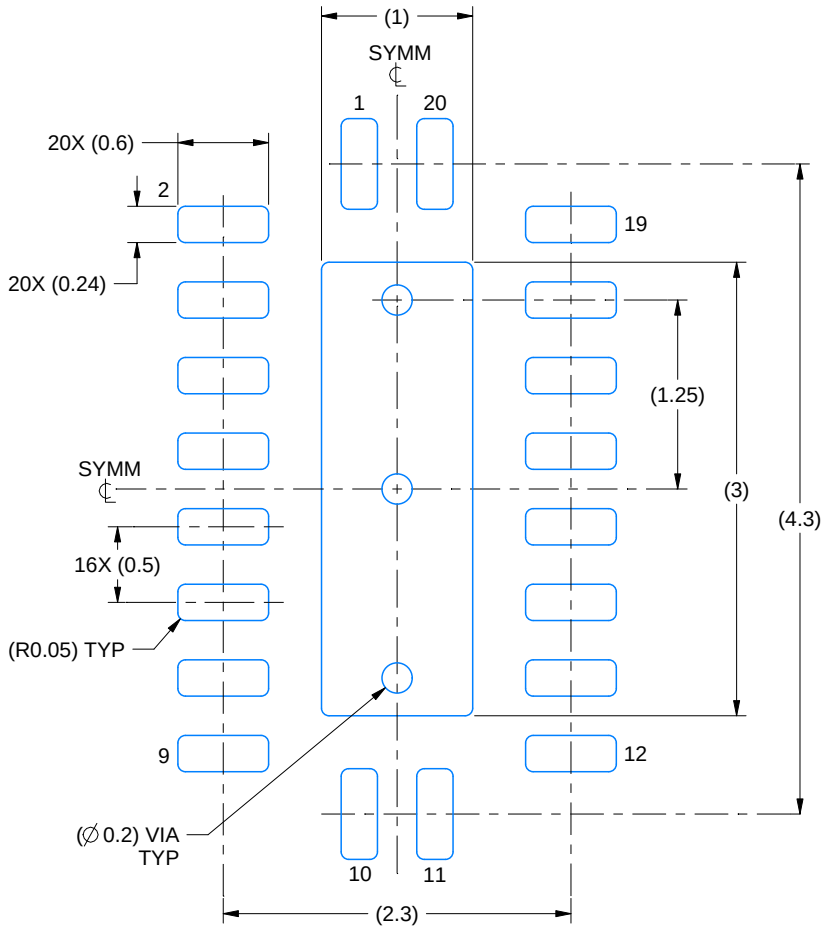
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

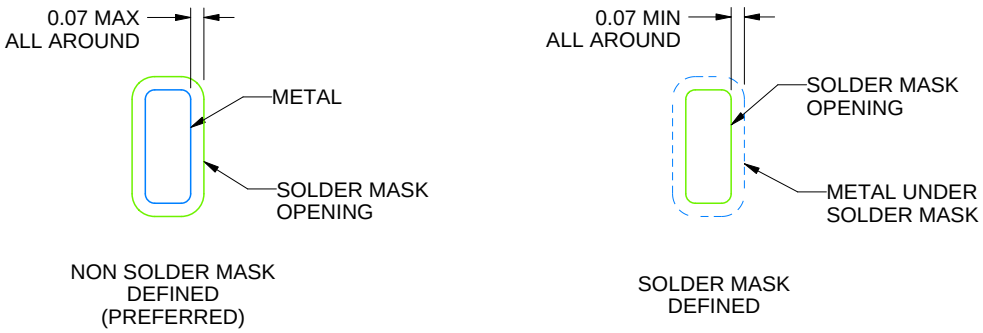


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

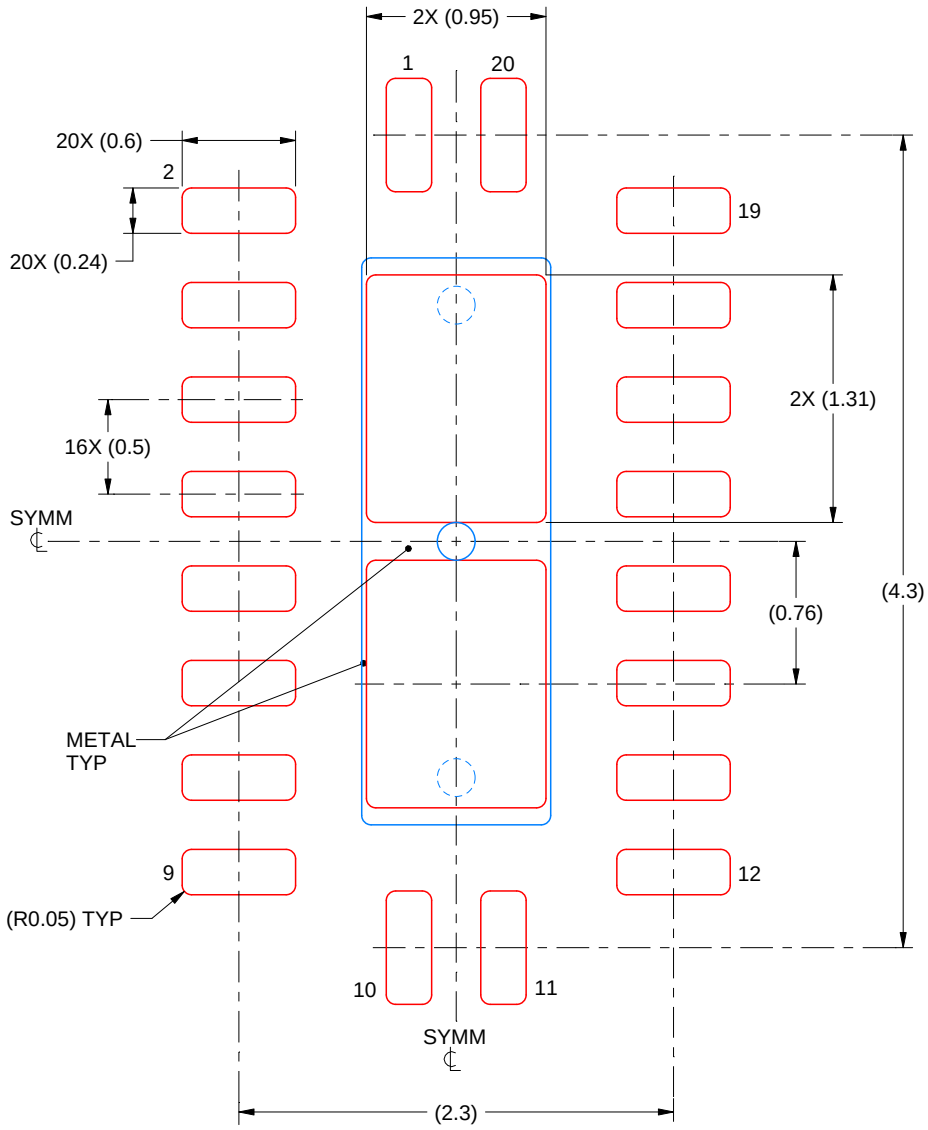


SOLDER MASK DETAILS

4222490/B 02/2021

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
83% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4222490/B 02/2021

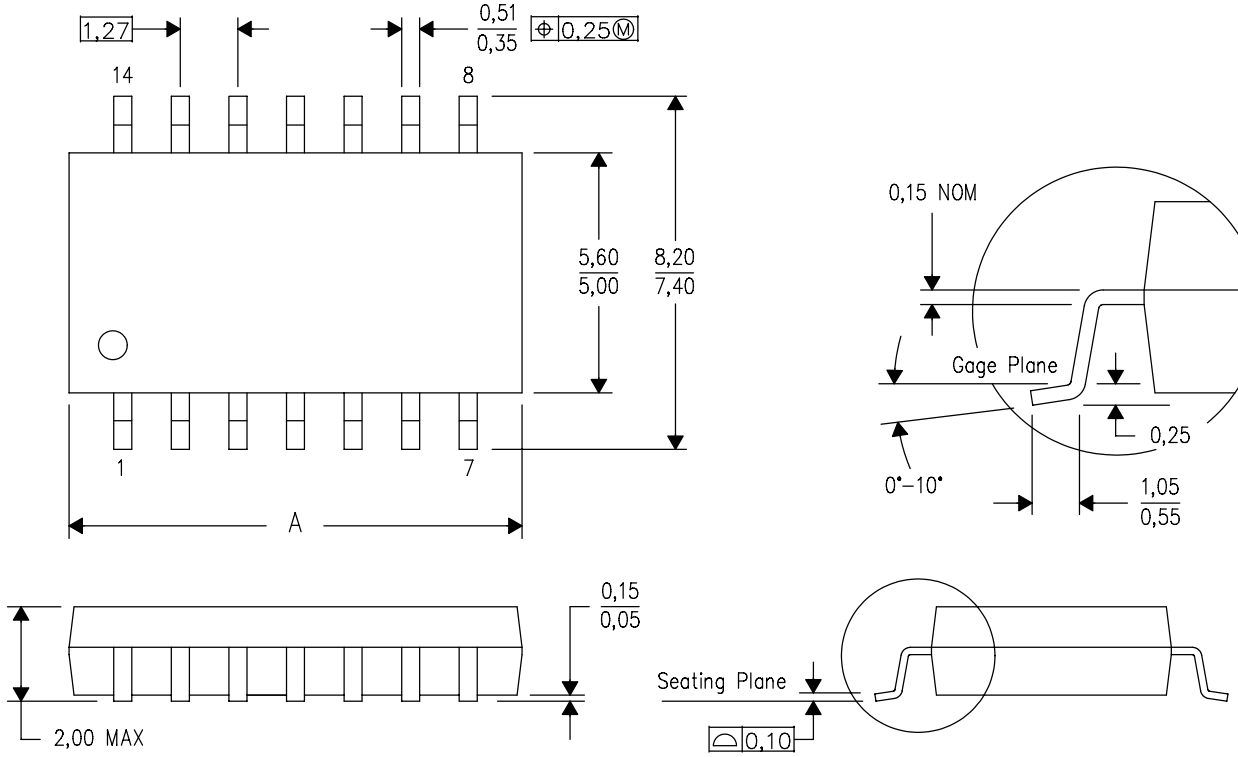
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

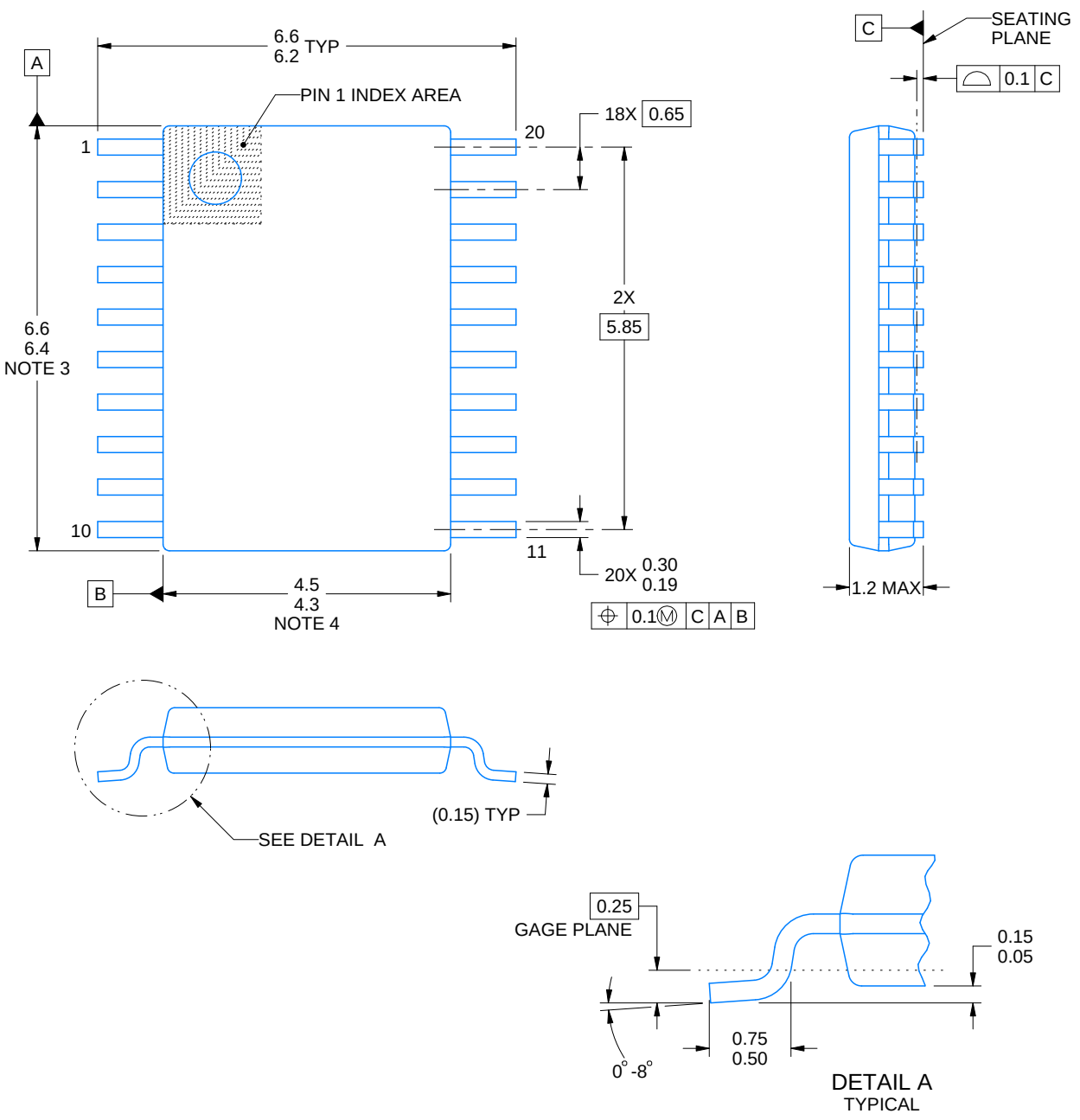
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PACKAGE OUTLINE

PW0020A

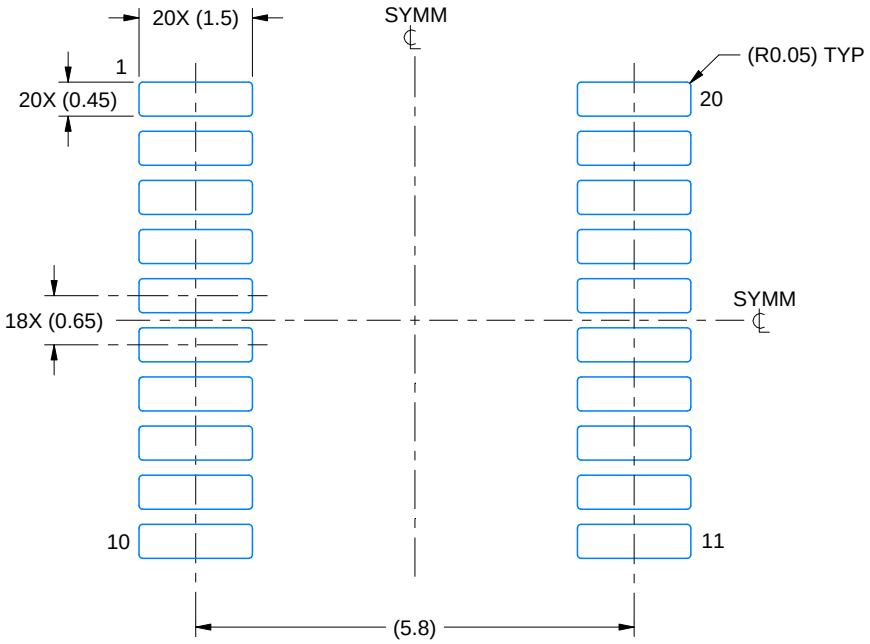
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



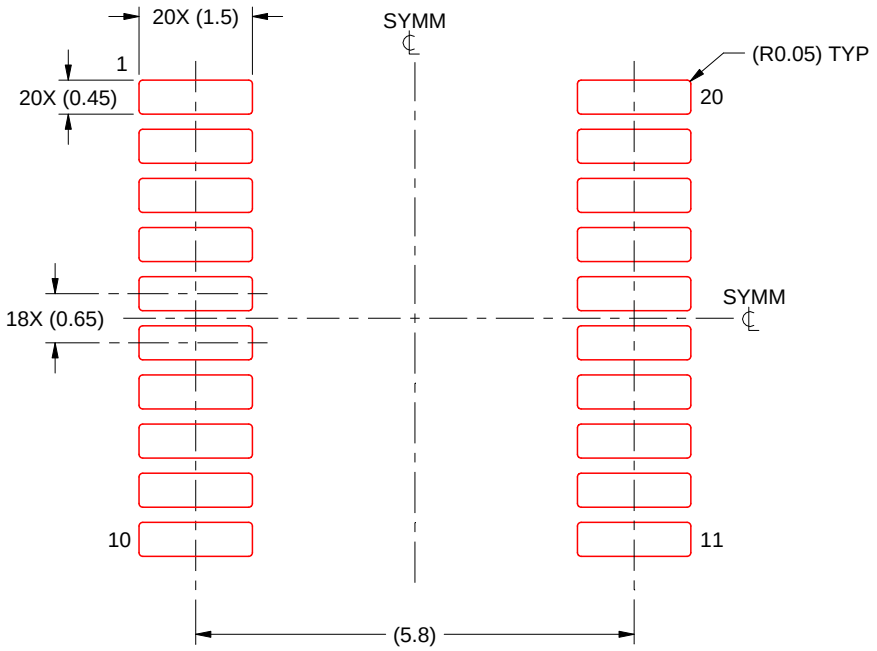
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

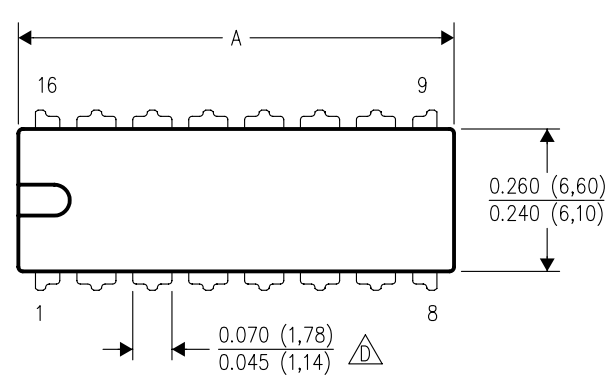
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

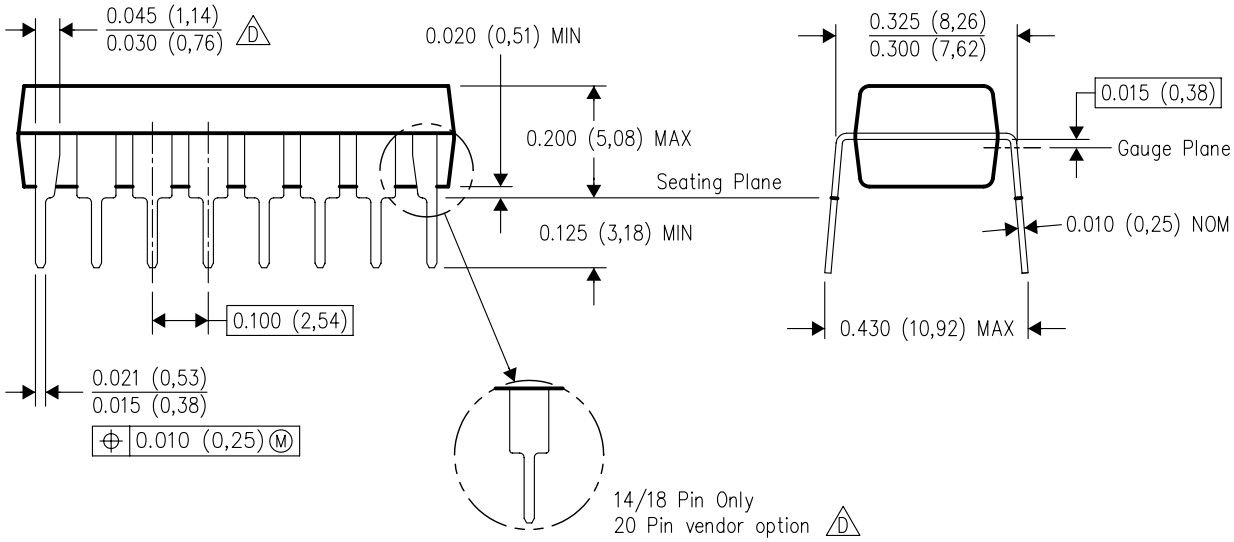
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

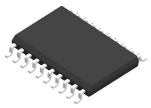


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

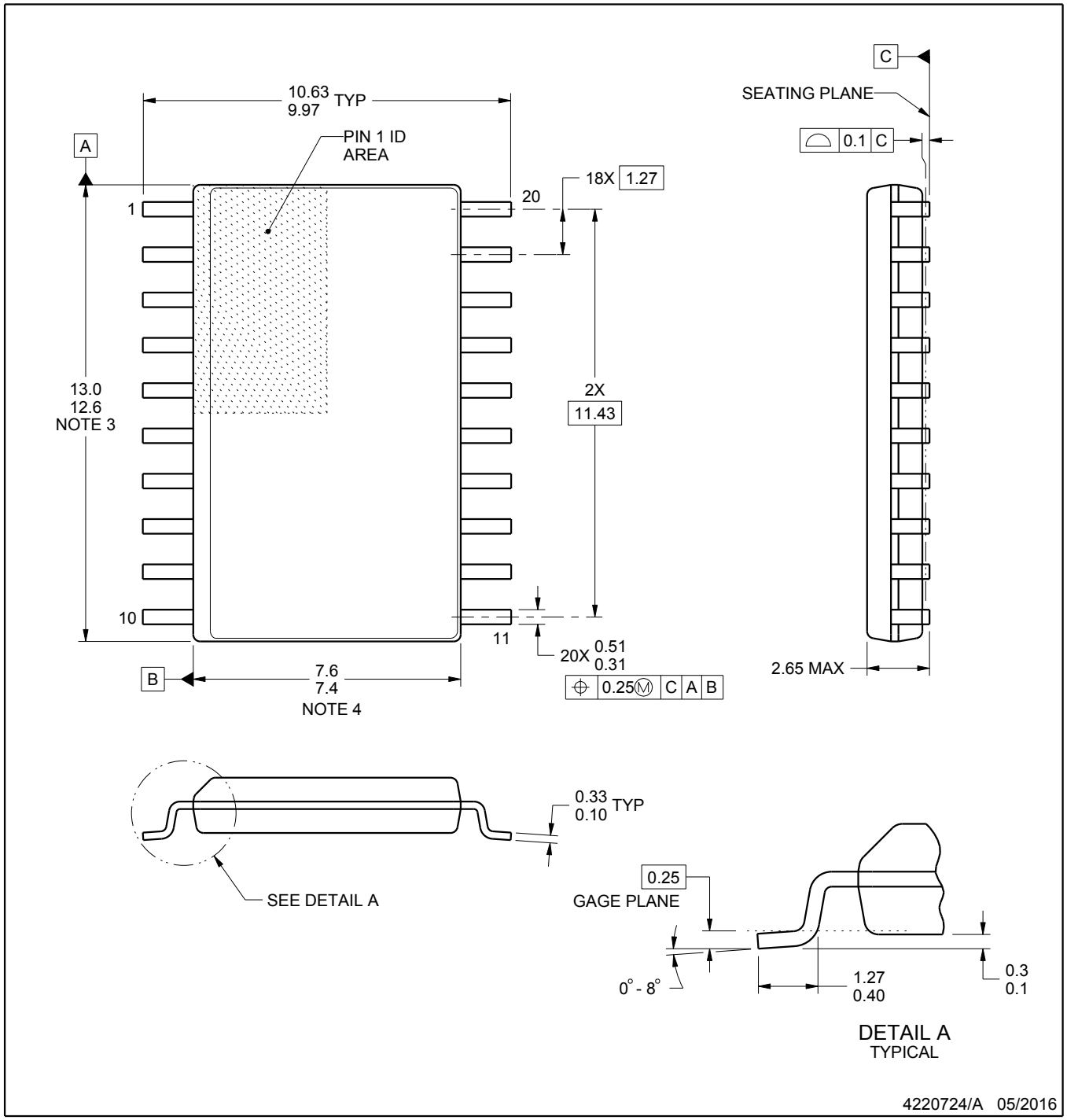


PACKAGE OUTLINE

DW0020A

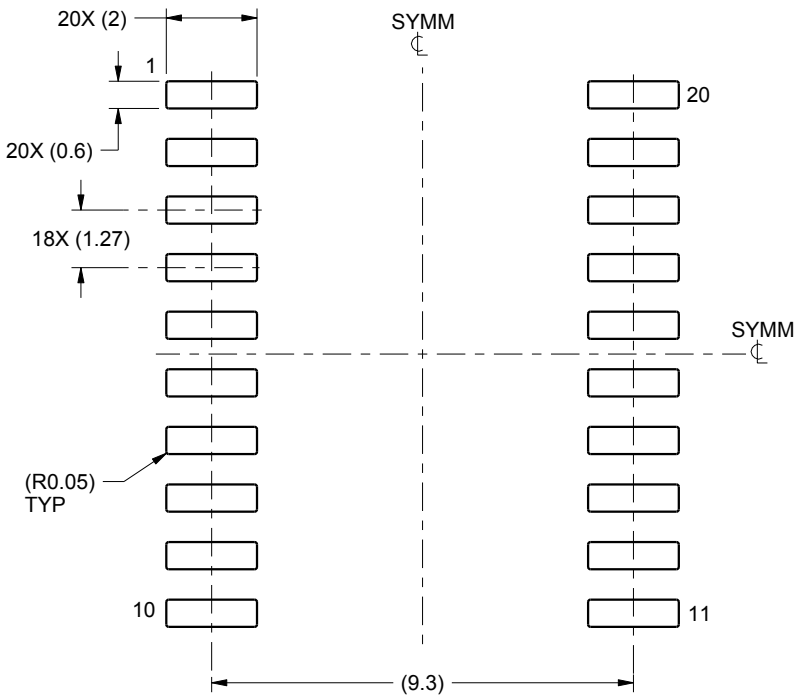
SOIC - 2.65 mm max height

SOIC

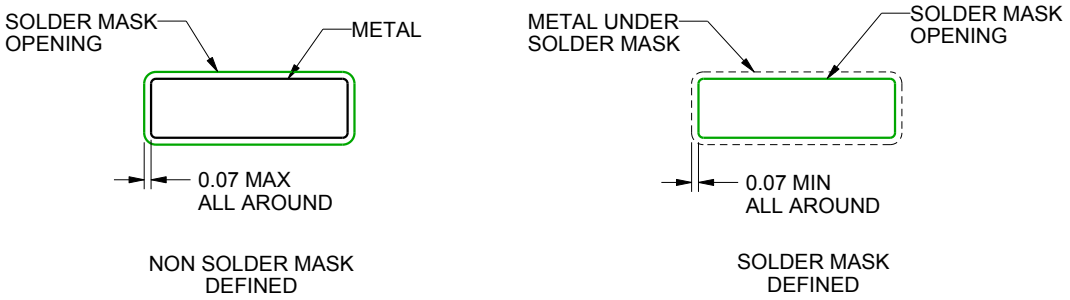


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X

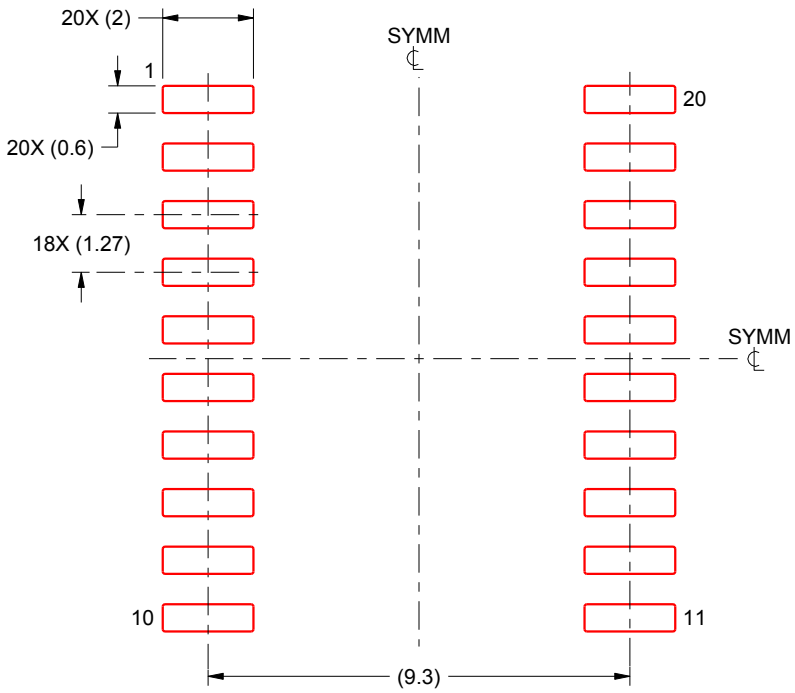


SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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