Functional Safety Information

LM5156, LM5156-Q1, LM51561, LM51561-Q1, LM5156H, LM5156H-Q1, LM51561H, LM51561H-Q1, and LM34966-Q1 Functional Safety FIT Rate and FMD

Table of Contents

1 Overview

This document contains information for LM5156, LM5156-Q1, LM51561, LM51561-Q1 (WSON), LM5156H, LM5156H-Q1, LM51561H, LM51561H-Q1, and LM34966-Q1 (HTSSOP) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device

Figure 1-1 and Figure 1-2 show the device functional block diagrams for reference.

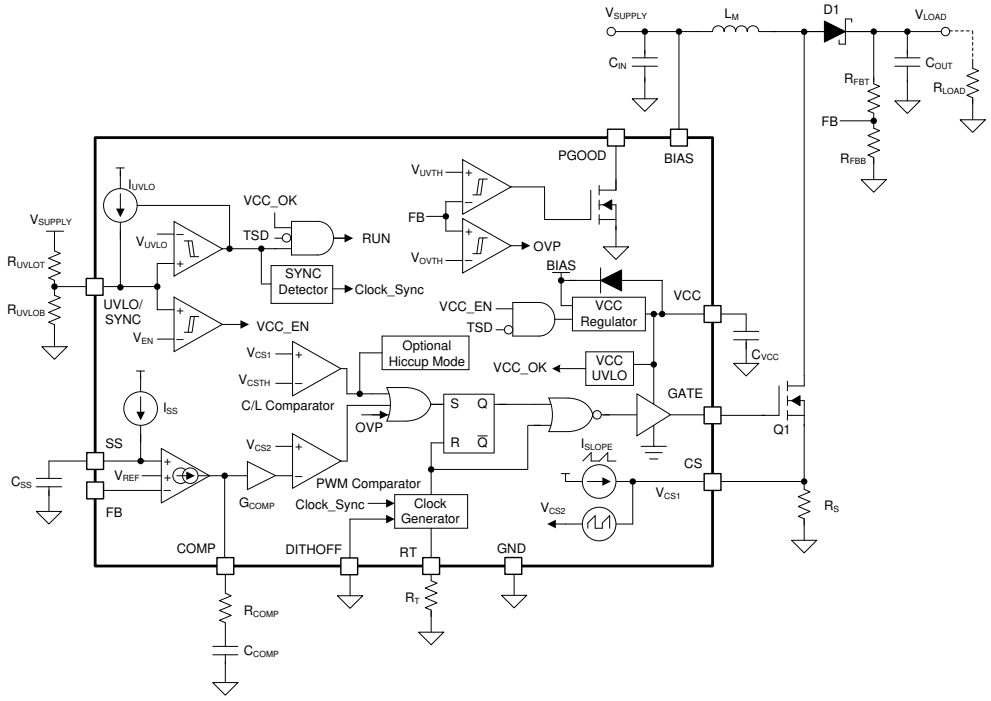

Figure 1-1. Functional Block Diagram (LM5156xH, LM5156xH-Q1)

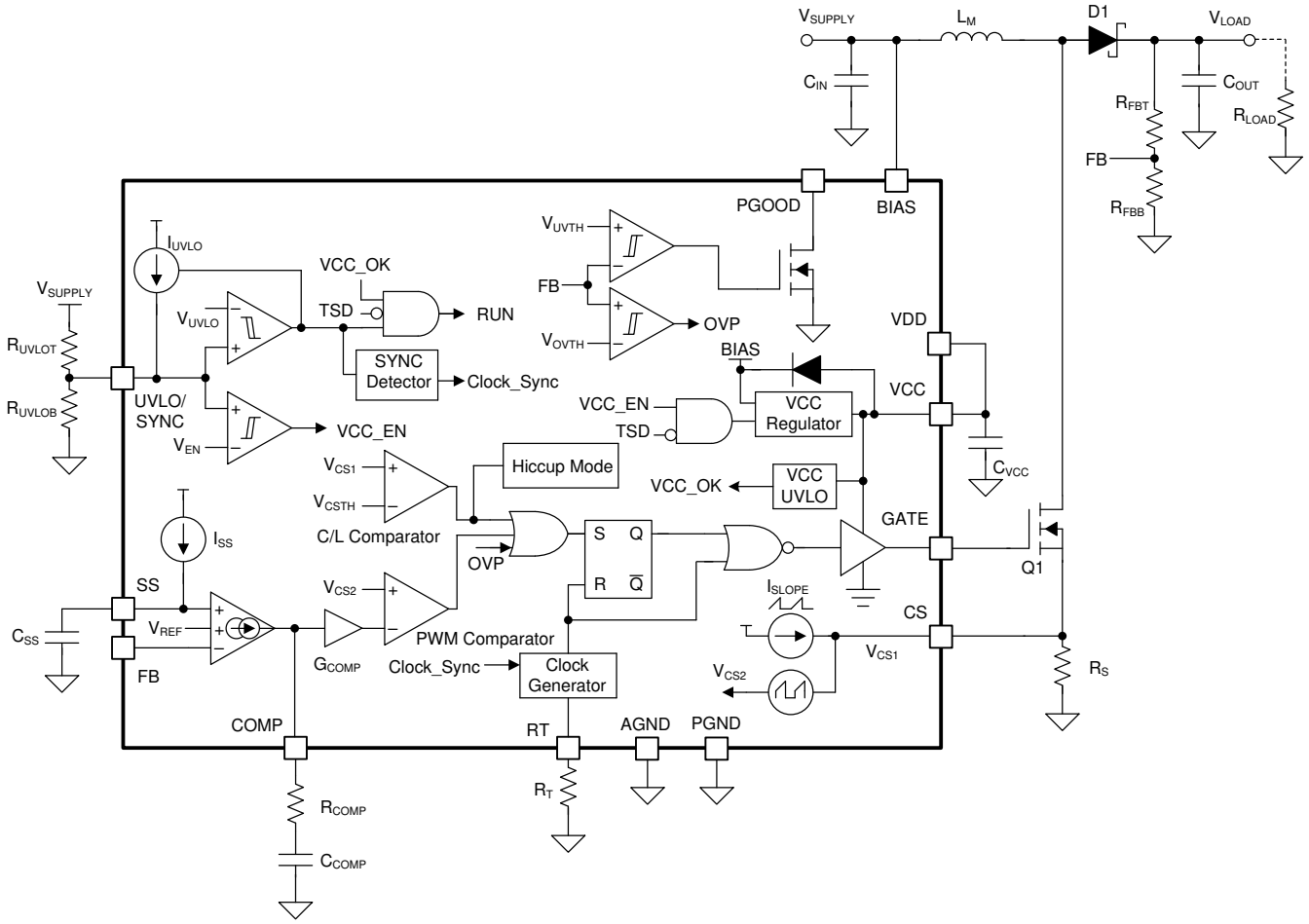

Figure 1-2. Functional Block Diagram (LM34966-Q1)

The LM5156, LM5156-Q1, LM51561, LM51561-Q1, LM5156H, LM5156H-Q1, LM51561H, LM51561H-Q1, and LM34966-Q1 were developed using a quality-managed development process, but were not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for LM5156, LM5156-Q1, LM51561, LM51561-Q1 (package of WSON) based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	6
Die FIT Rate	3
Package FIT Rate	3

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 250 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS/BICMOS ASICs Analog & Mixed HV >50V supply	30 FIT	75°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for LM5156H, LM5156H-Q1, LM51561H, LM51561H-Q1, and LM34966-Q1 (package of HTSSOP) based on two different industry-wide used reliability standards:

- Table 3-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 3-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 3-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	12
Die FIT Rate	4
Package FIT Rate	8

The failure rate and mission profile information in Table 3-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 250 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 3-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS/BICMOS ASICs Analog & Mixed HV >50V supply	30 FIT	75°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 3-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

4 Failure Mode Distribution (FMD)

The failure mode distribution estimation for LM5156, LM5156-Q1, LM51561, LM51561-Q1, LM5156H, LM5156H-Q1, LM51561H, LM51561H-Q1, and LM34966-Q1 (WSON and HTSSOP packages) in Table 4-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 4-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
No Output Voltage	60%
Output not in specification – voltage or timing	30%
Gate Driver stuck on	5%
Power Good – False Trip or Failure to Trip	5%

5 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the LM5156, LM5156-Q1, LM51561, LM51561-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 5-2)
- Pin open-circuited (see Table 5-3)
- Pin short-circuited to an adjacent pin (see Table 5-4)
- Pin short-circuited to BIAS supply (see Table 5-5)

Table 5-2 through Table 5-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 5-1.

Table 5-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 5-1 shows the LM5156, LM5156-Q1, LM51561, LM51561-Q1 (package of WSON) pin diagram. For a detailed description of the device pins please refer to the '*Pin Configuration and Functions*' section in the LM5156, LM5156-Q1, LM51561, LM51561-Q1 data sheet.

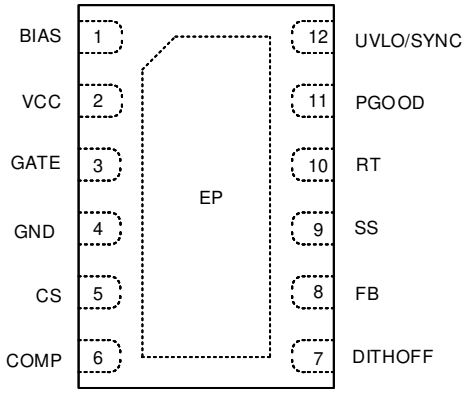

Figure 5-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Device used within the *Recommended Operating Conditions* and the *Absolute Maximum Ratings* found in the LM5156, LM5156-Q1, LM51561, LM51561-Q1 data sheet.
- Configuration as boost converter as shown in the *Application and Implementation* section found in the LM5156, LM5156-Q1, LM51561, LM51561-Q1 data sheet.

Table 5-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
BIAS	1	Device unpowered. Device not functional	B
VCC	2	VCC regulator short circuit. Device shuts down due to VCC undervoltage. VCC regulator may be disabled if thermal shutdown is triggered.	B
GATE	3	Gate driver is not functional. In boost operation, the output voltage is out of regulation. Output voltage is equal to input voltage minus diode forward voltage drop. Potential damage to pin	A
GND	4	No effect. Normal operation	D
CS	5	Loss of current sense information and loss of current limit. Loop is unstable and potential inductor saturation.	B
COMP	6	Device out of regulation. Device is not switching.	B
DITHOFF	7	Spread Spectrum enabled	B/D
FB	8	Output voltage rises uncontrolled. Potential damage to BIAS pin, if BIAS is connected to VOUT.	A
SS	9	During soft start, SS pin stuck low. The device does not start up. The device stops switching during operation.	B
RT	10	Switching frequency increased to > 2.2 MHz. Device may be unstable.	B
PGOOD	11	Correct output voltage. Loss of power good functionality	B
UVLO/SYNC/EN	12	EN stuck low. Device is disabled and in shut down mode.	B

Table 5-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
BIAS	1	Device unpowered. Device is not functional.	B
VCC	2	High ripple on the VCC pin that may trigger VCC UVLO.	B
GATE	3	Possible device damage	A
GND	4	Possible device damage	A
CS	5	Loss of current sense information and loss of current limit. Loop is unstable and potential inductor saturation.	B
COMP	6	Device is unstable.	C
DITHOFF	7	Spread spectrum function in an undefined state	B
FB	8	Output voltage rises uncontrolled. Potential damage to the BIAS pin if BIAS is connected to VOUT.	A
SS	9	During soft start, SS pin pulled high. The device soft start time reduced to 0. High inrush current possible. No effect during operation.	C
RT	10	Internal oscillator not functional. Device stops switching operation.	B
PGOOD	11	Correct output voltage. Loss of power-good functionality	C
UVLO/SYNC/EN	12	State of EN/UVLO/SYNC undetermined. Device may be in shut down or standby mode or enabled.	B

Table 5-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
BIAS	1	VCC	Potential device damage, if BIAS voltage is greater 18 V. Normal operation, if BIAS voltage is below 18 V.	A/D
VCC	2	GATE	Gate driver not functional. Output voltage is out of regulation. Potential damage to pin	A
GATE	3	GND	Gate driver not functional. Output voltage is out of regulation. In boost operation, the output voltage is equal to input voltage minus diode forward voltage drop. Potential damage to pin	A
GND	4	CS	See Table 5-2.	B
CS	5	COMP	Potential damage to part. Absolute maximum voltage for this pin is 0.3 V.	A
COMP	6	DITHOFF	Not considered. Corner pin	D
DITHOFF	7	FB	Spread spectrum functionality undeterminded. Output voltage may be out of regulation.	B
FB	8	SS	COMP pin voltage clamped to 1 V. Device is not switching and out of regulation.	B
SS	9	RT	Output voltage regulates to VOUT/2. Switching frequency may be incorrect.	B
RT	10	PGOOD	If FB < 0.9 V (falling) and PGOOD is active low, the switching frequency increased to > 2.2 MHz. Device may be unstable. If FB > 0.95 V (rising) and PGOOD is pulled up externally, the internal oscillator stops. Potential device damage if pull up voltage is > 3.8 V.	A
PGOOD	11	UVLO/SYNC/EN	Potential damage to device, if pin 12 is directly connected to supply.	A
UVLO/SYNC/EN	12	BIAS	Not considered. Corner pin	D

Table 5-5. Pin FMA for Device Pins Short-Circuited to BIAS supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
BIAS	1	No effect. Normal operation	D
VCC	2	Potential device damage if BIAS voltage is greater 18 V. Normal operation if BIAS voltage is below 18 V.	A/D
GATE	3	External MOSFET is turned on constantly. Potential damage of external component	A
GND	4	Device is unpowered. Device is not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be plausible.	A
CS	5	Potential device damage. Absolute maximum rating for this pin is 0.3 V.	A
COMP	6	Potential device damage if current into pin exceeds 1.6 mA	A
DITHOFF	7	Potential device damage if BIAS voltage is greater 18 V	A
FB	8	Potential device damage if BIAS voltage is greater 4.0 V	A
SS	9	Potential device damage if BIAS voltage is greater 3.8 V	A
RT	10	Potential device damage if BIAS voltage is greater 3.8 V	A
PGOOD	11	Potential device damage if BIAS voltage is greater 18 V or current into pin exceeds 1 mA	A
UVLO/SYNC/EN	12	No effect. Normal operation	D

6 Pin Failure Mode Analysis (Pin FMA) – HTSSOP

This section provides a Failure Mode Analysis (FMA) for the pins of the LM5156H, LM5156H-Q1, LM51561H, LM51561H-Q1, and LM34966-Q1 (and HTSSOP package). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 6-2)
- Pin open-circuited (see Table 6-3)
- Pin short-circuited to an adjacent pin (see Table 6-4)
- Pin short-circuited to BIAS supply (see Table 6-5)

Table 6-2 through Table 6-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 6-1.

Table 6-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 6-1 shows the LM5156H, LM5156H-Q1, LM51561H, LM51561H-Q1, and LM34966-Q1 (package of HTSSOP) pin diagram. For a detailed description of the device pins please refer to the '*Pin Configuration and Functions*' section in the LM5156H, LM5156H-Q1, LM51561H, LM51561H-Q1, and LM34966-Q1 datasheet.

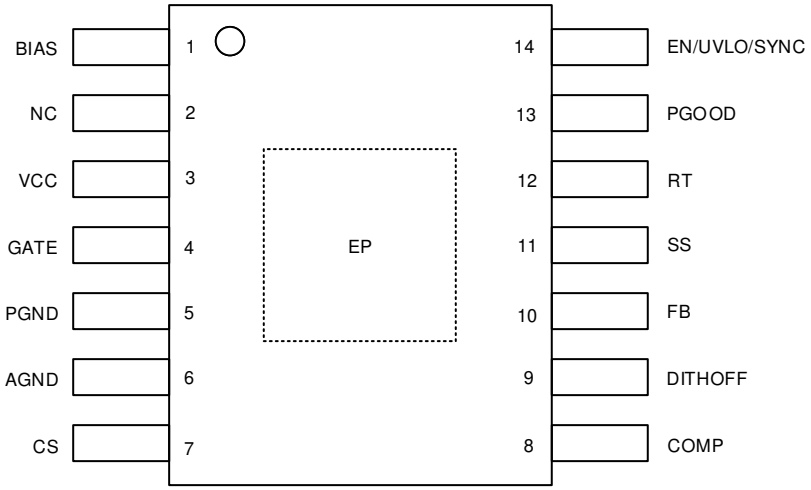

Figure 6-1. Pin Diagram LM5156H, LM5156H-Q1, LM51561H, LM51561H-Q1

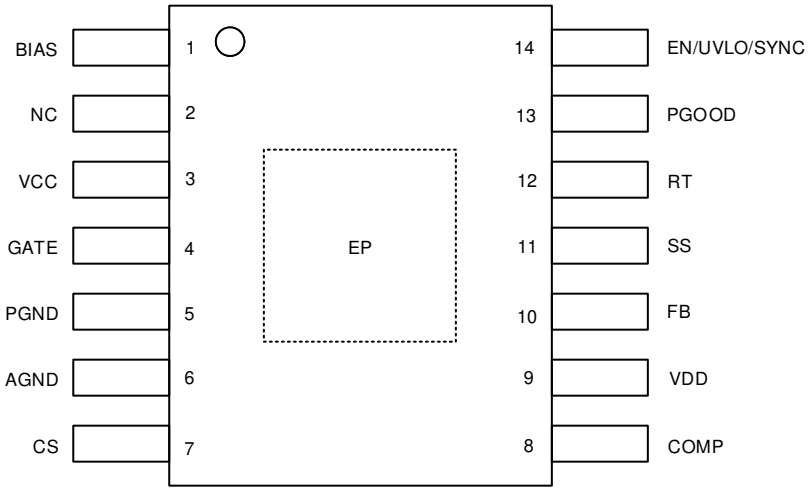

Figure 6-2. Pin Diagram LM34966-Q1

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Device used within the *Recommended Operating Conditions* and the *Absolute Maximum Ratings* found in the LM5156H, LM5156H-Q1, LM51561H, LM51561H-Q1, and LM34966-Q1 data sheet.
- Configuration as boost converter as shown in the *Application and Implementation* section found in the LM5156H, LM5156H-Q1, LM51561H, LM51561H-Q1, and LM34966-Q1 data sheet.

Table 6-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
BIAS	1	Device unpowered. Device is not functional.	B
NC	2	No effect. Normal operation	D
VCC	3	VCC regulator short circuit. Device shuts down due to VCC undervoltage. VCC regulator may be disabled if thermal shutdown is triggered.	B
GATE	4	Gate driver not functional. In boost operation, the output voltage is out of regulation. Output voltage is equal to input voltage minus diode forward voltage drop. Potential damage to pin	A
PGND	5	No effect. Normal operation	D
AGND	6	No effect. Normal operation	D
CS	7	Loss of current sense information and loss of current limit. Loop is unstable and there is potential inductor saturation.	B
COMP	8	Device out of regulation. Device is not switching.	B
DITHOFF	9	LM5156H, LM5156H-Q1, LM51561H, LM51561H-Q1: Spread Spectrum enabled.	B/D
VDD	9	LM34966-Q1: Switching frequency may be impacted.	B
FB	10	Output voltage rises uncontrolled. Potential damage to BIAS pin, if BIAS is connected to VOUT.	A
SS	11	During soft start, SS pin stuck low. The device does not start-up. The device stops switching during operation.	B
RT	12	Switching frequency is increased to > 2.2 MHz. Device may be unstable.	B
PGOOD	13	Correct output voltage. Loss of power good functionality	B
UVLO/SYNC/EN	14	EN stuck low. Device is disabled and in shut down mode.	B

Table 6-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
BIAS	1	Device unpowered. Device is not functional.	B
NC	2	No effect. Normal operation	D
VCC	3	High ripple on VCC pin that may trigger VCC UVLO	B
GATE	4	Possible device damage	A
PGND	5	Possible device damage	A
AGND	6	Possible device damage	A
CS	7	Loss of current sense information and loss of current limit. Loop is unstable and potential inductor saturation.	B
COMP	8	Device may be unstable.	C
DITHOFF	9	LM5156H, LM5156H-Q1, LM51561H, LM51561H-Q1: Spread spectrum in an undefined state	B
VDD	9	LM34966-Q1: Switching frequency may be impacted.	B
FB	10	Output voltage rises uncontrolled. Potential damage to BIAS pin if BIAS is connected to VOUT.	A
SS	11	During soft start, SS pin pulled high. The device soft start time reduced to 0. High inrush current possible. No effect during operation.	C
RT	12	Internal oscillator not functional. Device stops switching operation.	B
PGOOD	13	Correct output voltage. Loss of power-good functionality.	C
UVLO/SYNC/EN	14	State of EN/UVLO/SYNC undetermined. Device may be in shut down or standby mode or enabled.	B

Table 6-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
BIAS	1	NC	No effect. Normal operation	D
NC	2	VCC	No effect. Normal operation	D
VCC	3	GATE	Gate driver not functional. Output voltage is out of regulation. Potential damage to pin	A
GATE	4	GND	Gate driver not functional. Output voltage is out of regulation. In boost operation, the output voltage is equal to input voltage minus diode forward voltage drop. Potential damage to pin	A
PGND	5	AGND	Normal operation	D
AGND	6	CS	See Table 6-2.	B
CS	7	COMP	Not considered. Corner pin	D
COMP	8	DITHOFF	LM5156H, LM5156H-Q1, LM51561H, LM51561H-Q1: Potential damage to part if current into pin exceeds 1.6 mA.	A
DITHOFF	9	FB	LM5156H, LM5156H-Q1, LM51561H, LM51561H-Q1: Spread spectrum functionality undeterminded. Output voltage may be out of regulation.	B
COMP	8	VDD	LM34966-Q1: Potential damage to part if current into pin exceeds 1.6 mA.	A
VDD	9	FB	LM34966-Q1: FB regulates to 1 V and output voltage may be out of regulation.	B
FB	10	SS	COMP pin voltage is clamped to 1 V. Device is not switching and out of regulation.	B
SS	11	RT	Output voltage regulates to VOUT/2. Switching frequency may be incorrect.	B
RT	12	PGOOD	If FB < 0.9 V (falling) and PGOOD active low, the switching frequency increased to > 2.2 MHz. Device may be unstable. If FB > 0.95 V (rising) and PGOOD is pulled up externally, the internal oscillator stops. Potential device damage if pull up voltage is > 3.8 V.	A
PGOOD	13	UVLO/SYNC/EN	Potential damage to device if pin 14 is directly connected to supply.	A
UVLO/SYNC/EN	14	BIAS	Not considered. Corner pin	D

Table 6-5. Pin FMA for Device Pins Short-Circuited to BIAS supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
BIAS	1	No effect. Normal operation	D
NC	2	No effect. Normal operation	D
VCC	3	Potential device damage if BIAS voltage is greater 18 V. Normal operation if BIAS voltage is below 18 V.	A/D
GATE	4	External MOSFET turned on constantly. Potential damage of external component	A
PGND	5	Device is unpowered. Device is not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be plausible.	A
AGND	6	Device is unpowered. Device is not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be plausible.	A
CS	7	Potential device damage. Absolute maximum rating for this pin is 0.3 V.	A
COMP	8	Potential device damage if current into pin exceeds 1.6 mA.	A
DITHOFF	9	LM5156H, LM5156H-Q1, LM51561H, LM51561H-Q1: Potential device damage if BIAS voltage is greater 18 V	A
VDD	9	LM34966-Q1: Potential device damage if BIAS voltage is greater 18 V	A
FB	10	Potential device damage if BIAS voltage is greater 4.0 V	A
SS	11	Potential device damage if BIAS voltage is greater 3.8 V	A
RT	12	Potential device damage if BIAS voltage is greater 3.8 V	A
PGOOD	13	Potential device damage if BIAS voltage is greater 18 V or current into pin exceeds 1 mA	A
UVLO/SYNC/EN	14	No effect. Normal operation	D

7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (January 2021) to Revision C (April 2021)	Page
• Added pin FMA	7

Changes from Revision A (September 2020) to Revision B (January 2021)	Page
• Updated overview to clarify information	2

Changes from Revision * (June 2020) to Revision A (September 2020)	Page
• Added LM34966-Q1 (HTSSOP)	2

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