OPTIMIZING PERFORMANCE OF THE DCP01B, DVC01 AND DCP02 SERIES OF UNREGULATED DC/DC CONVERTERS.

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The DCP01B, DCV01, and DCP02 are three families of miniature DC/DC converters providing an isolated unregulated voltage output. All are fabricated using a CMOS/DMOS process with the DCP01B replacing the familiar DCP01 family that was fabricated from a bipolar process. The DCP02 is essentially an extension of the DCP01B family providing a higher power output with a significantly improved load regulation, and the DCV01 is tested to a higher isolation voltage.

TECHNOLOGICAL IMPROVEMENTS

Transformer drive circuit

The new CMOS/DMOS process represents an improvement over the bipolar process as the internal circuits can switch much faster. Additionally, the transformer drive transistors have a characteristically low value of transistor 'on' resistance, (R_{DS}), thus more power is transferred to the transformer. With the Bipolar process, the transformer drive circuit was limited by the base current available to switch on the power transistors driving the transformer, and their characteristic current gain (beta) resulting in a slower turn-on time. Consequently, more power was dissipated within the transistor. This resulted in a lower overall efficiency, particularly at higher output load currents.

Self synchronization

The input synchronizations facility, ($SYNC_{IN}$) has been improved over the bipolar devices. If two to eight devices (maximum) have their respective $SYNC_{IN}$ pins connected together, then all devices will be synchronized.

Each device has its own onboard oscillator. This is generated by charging a capacitor from a constant current and producing a ramp. When this ramp passes a threshold, an internal switch is activated that discharges the capacitor to a second threshold before the cycle is repeated.

When several devices are connected together, all the internal capacitors are charged simultaneously.

The improvements within the new process are such that when one device passes its threshold during the charge cycle, it starts the discharge cycle. All the other devices sense this falling voltage and likewise initiate a discharge cycle so that all devices discharge together. A subsequent charge cycle is only restarted when the last device has finished its discharge cycle.

OPTIMIZING PERFORMANCE

The optimum performance can only be achieved if the device is correctly supported. By the very nature of a switching converter, it requires power to be instantly available when it 'switches' on. If the converter has DMOS switching transistors, the fast edges will create a high current demand on the input supply. This transient load placed on the input is supplied by the external input decoupling capacitor, thus maintaining the input voltage. Therefore, the input supply does not see this transient (this is an analogy to high-speed digital circuits). The positioning of the capacitor is critical and must be placed as close as possible to the input pins and tracked via a low impedance path.

The optimum performance is primarily dependent on two factors:

1) Tracking of the input and output circuits for minimal loss.
2) The ability of the decoupling capacitors to maintain the input and output voltages at a constant level.

PCB Tracking

The losses due to resistance and inductance caused by tracking can be minimized by the use of a ground and power plane where possible. If that is not possible, use wide tracks to reduce the losses. If several devices are being powered from a common power source, a 'star' connected system for the tracking must be deployed; devices must not be tracked in 'series', as this will cascade the losses. The position of the decoupling capacitors is important. They must be as close to the devices as possible in order to reduce losses.

Decoupling capacitors

All capacitors have losses due to their internal Equivalent Series Resistance, (ESR) and to a lesser degree their Equivalent Series Inductance (ESL). Values for the latter are not always easy to obtain, however, some manufacturers provide graphs of Frequency versus Capacitor Impedance. These will show the capacitors impedance falling as frequency is increased. As the frequency is increased the impedance will stop decreasing and begin to rise. The point of minimum impedance indicates the capacitors resonant frequency. This frequency is where the components of capacitance and inductance reactance are of equal magnitude. Beyond this point the capacitor is not effective as a capacitor.

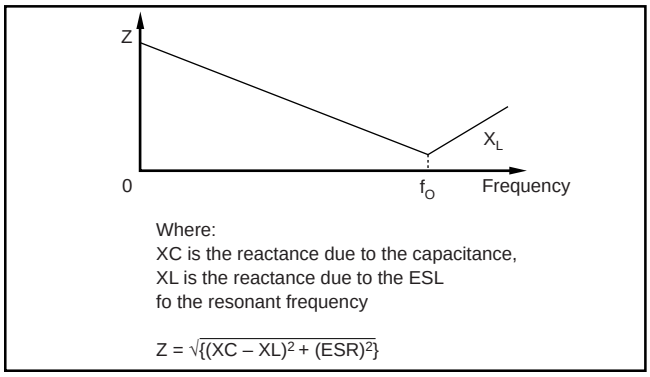


FIGURE 1. Capacitor Impedance versus Frequency.

At f_o, $X_C = X_L$, however, there is a 180° phase difference resulting in cancellation of the imaginary component. The resulting effect is the impedance at the resonant point is the real part of the complex impedance namely the value of the ESR. The resonant frequency must be well above the 800kHz switching frequency of the DCP and DCVs.

The effect of the ESR is to cause a voltage drop within the capacitor. The value of this voltage drop is simply the product of the ESR and the transient load current:

$$V_{IN} = V_{PK} - (ESR \bullet I_{TR})$$

Where V_{IN} is the voltage at the device input, V_{PK} is the maximum value of the voltage on the capacitor during charge, and I_{TR} is the transient load current.

The other factor that effects the performance is the value of the capacitance. However, for the input and the full wave outputs (single output voltage devices) the ESR is the dominant factor.

Input Capacitor and the effects of ESR

If the input decoupling capacitor does not have a low value of ESR, then at the instant the power transistors switch on, the voltage at the input pins will fall momentarily. Should the voltage fall below approximately 4V, the DCP will detect an under voltage condition and switch the DCP drive circuits to the off state. This is carried out as a precaution against a genuine low input voltage condition that could slow down or even stop the internal circuits from operating correctly. This would result in the drive transistors being turned on too long, causing saturation of the transformer and destruction of the device.

Following detection of a low input voltage condition, the device switches off the internal drive circuits until the input voltage returns to a safe value. Then the device tries to restart. If the input capacitor is still unable to maintain the input voltage, shutdown reoccurs. This process is repeated until the capacitor is charged sufficiently to start the device correctly. Otherwise, the device will be caught up in a loop.

Normal start up should occur in approximately 1ms from power being applied to the device. If a considerably longer start up duration time is encountered, it is likely that either (or both) the input supply or the capacitors are not performing adequately.

For 5V input devices a 2.2µF ceramic capacitor will ensure a good start up performance, and for the remaining input voltage ranges, 0.47µF ceramic capacitors are good. If tantalum capacitors are being considered, close attention must be paid to the ESR value specified, as most tantalum capacitors do not have low ESR values.

Output Ripple Calculation Example

DCP020505: Output voltage 5V, Output current 0.4A. At full output power, the load resistor is 12.5Ω. Output capacitor of 1µF, ESR of 0.1Ω. Capacitor discharge time 1% of 800kHz (ripple frequency):

$$t_{DIS} = 0.0125\mu s$$

$$\tau = C \bullet R_{LOAD}$$

$$\tau = 1 \bullet 10^{-6} \bullet 12.5 = 12.5\mu s$$

$$V_{DIS} = V_O(1 - EXP(-t_{DIS}/\tau))$$

$$V_{DIS} = 5mV$$

By contrast the voltage dropped due to the ESR:

$$V_{ESR} = I_{LOAD} \bullet ESR$$

$$V_{ESR} = 40mV.$$

Ripple voltage = 45mV.

Clearly, increasing the capacitance will have a much smaller effect on the output ripple voltage than reducing the value of the ESR for the filter capacitor.

DUAL OUTPUT VOLTAGE DCP AND DCV'S

The voltage output for the dual DCPs is half wave rectified, therefore, the discharge time is 1.25µs. Repeating the above calculations using the 100% load resistance of 25Ω (0.2A per output), the results are shown below:

$$\tau = 25\mu s$$

$$T_{DIS} = 1.25\mu s.$$

$$V_{DIS} = 244mV$$

$$V_{ESR} = 20mV.$$

Ripple Voltage = 266mV.

This time it is the capacitor discharging that is contributing to the largest component of ripple. Changing the output filter to 10µF, and repeating the calculations:

Ripple Voltage = 45mV.

This value is composed of almost equal components.

The above calculations are given only as a guide, capacitor parameters usually have large tolerances and can be susceptible to environmental conditions.

OTHER DOCUMENTS RELATING TO THE DCP01B, DCV01 AND DCP02

AB-153: External Synchronization of the DCP01, 02 Series of DC/DC Converters (SBAA035).

PCB LAYOUT NOTES

Figures 2 and 3 illustrate a printed circuit board layout tracked for the two conventional (DCP01/02, DCV01), and two SO-28 surface mount packages (DCP02U).

Input power and ground planes have been utilized providing a low impedance path for the input power. For the output the common or 0V has been tracked via a ground plane while the tracking for the positive and negative voltage outputs are conducted via wide tracks in order to minimize losses.

The location of the decoupling capacitors in close proximity to their respective pins ensures low losses due to the effects of tracking inductance thus improving the ripple performance. This is of particular importance to the input decoupling capacitor as this supplies the transient current associated with the fast switching waveforms of the power drive circuits.

The Sync pin when not being used is best left as a floating pad. A ground ring or annulus connected around the pin will prevent noise being conducted onto the pin. If the Sync pin is being connected to one or more Sync pins then the linking track should be narrow and must be kept short in length, also no other track should be in close proximity to this track as this will increase the stray capacitance on this pin, that will effect the performance of the oscillator.

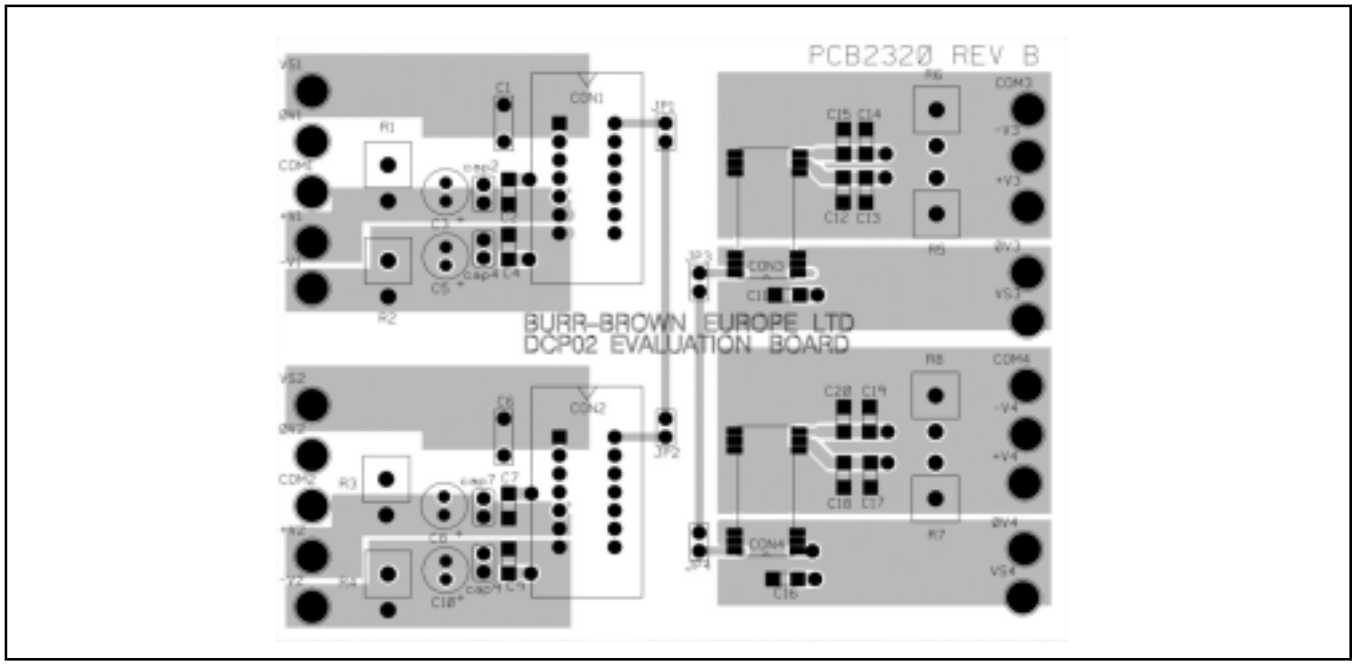


FIGURE 2. Example of PCB Layout, View on Component Side.

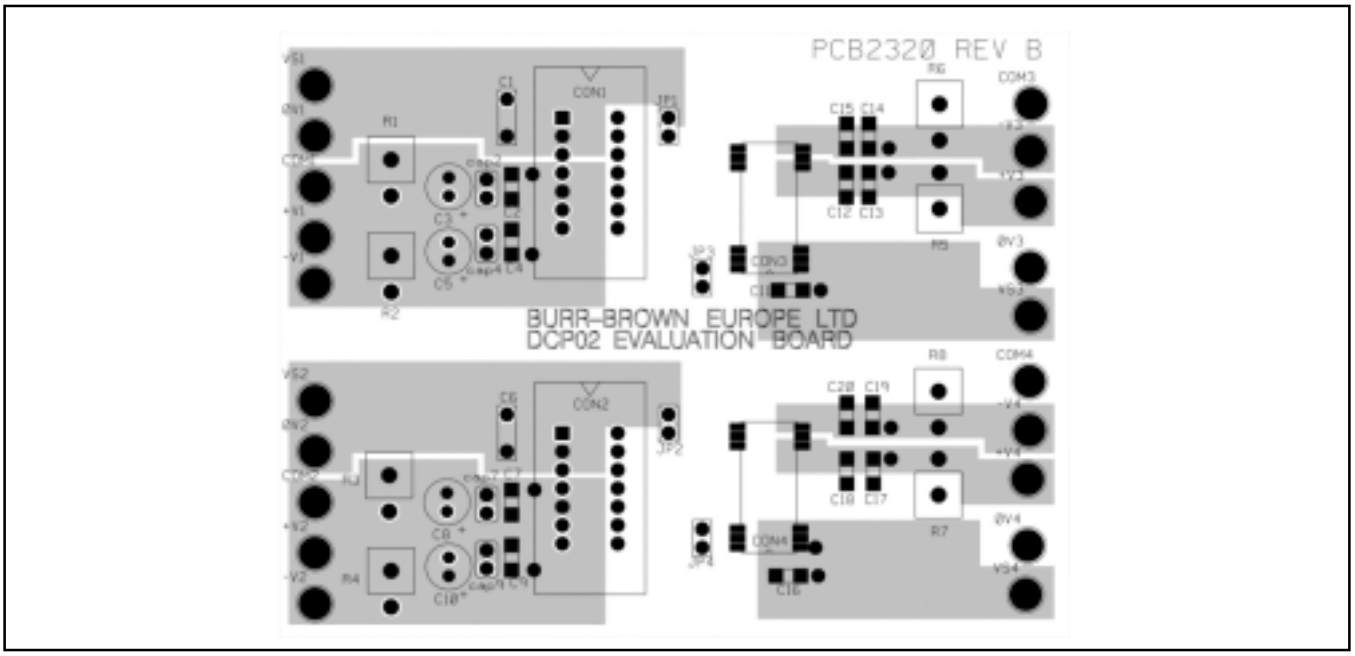
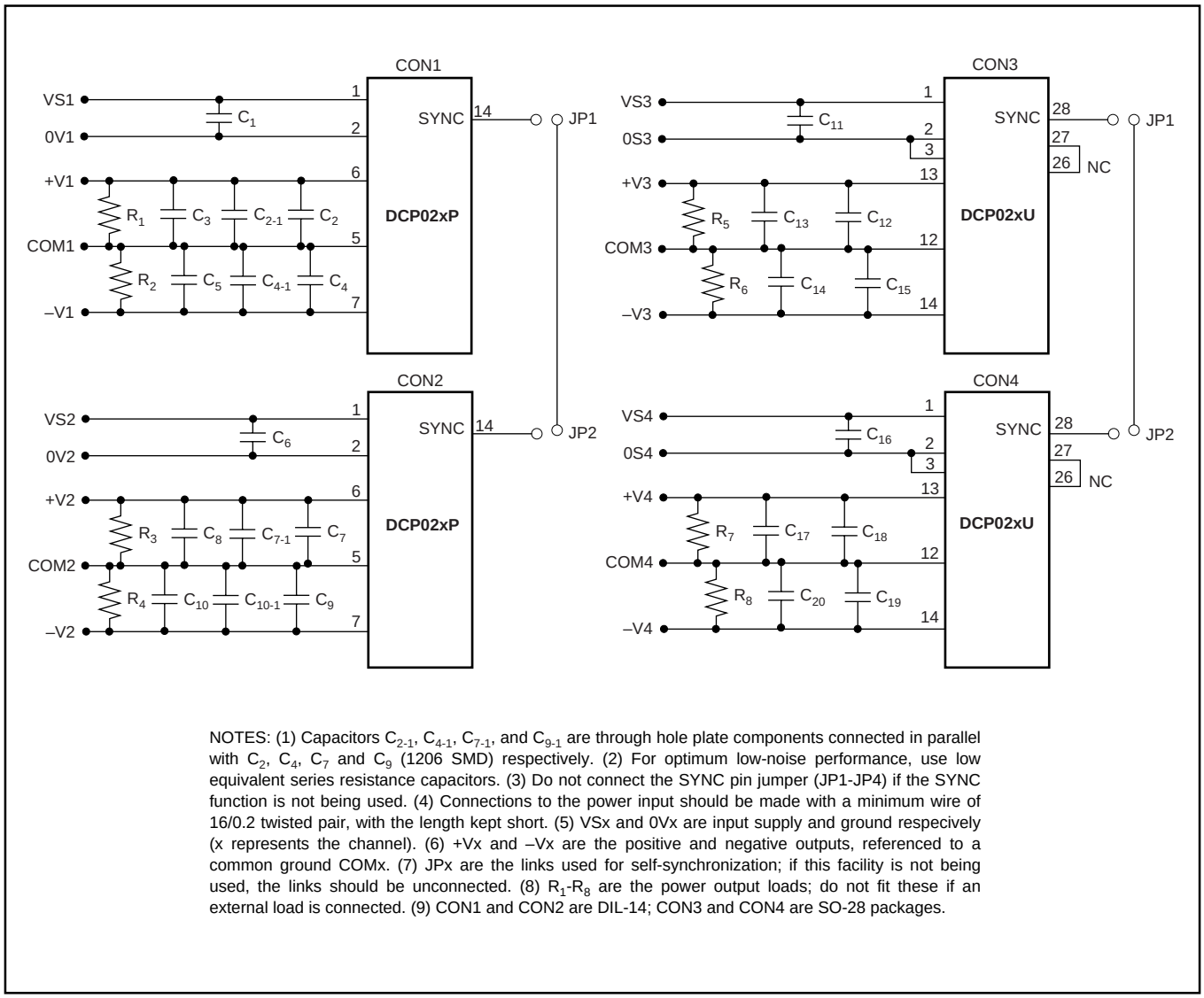


FIGURE 3. Example of PCB Layout, Non Component Side.



NOTES: (1) Capacitors C_{2-1}, C_{4-1}, C_{7-1}, and C_{9-1} are through hole plate components connected in parallel with C_2, C_4, C_7 and C_9 (1206 SMD) respectively. (2) For optimum low-noise performance, use low equivalent series resistance capacitors. (3) Do not connect the SYNC pin jumper (JP1-JP4) if the SYNC function is not being used. (4) Connections to the power input should be made with a minimum wire of 16/0.2 twisted pair, with the length kept short. (5) VSx and 0Vx are input supply and ground respecively (x represents the channel). (6) +Vx and –Vx are the positive and negative outputs, referenced to a common ground COMx. (7) JPx are the links used for self-synchronization; if this facility is not being used, the links should be unconnected. (8) R_1-R_8 are the power output loads; do not fit these if an external load is connected. (9) CON1 and CON2 are DIL-14; CON3 and CON4 are SO-28 packages.

FIGURE 4. Example of PCB Layout, Schematic Diagram.

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