Power Supply Design for the ADS41xx

Thomas Neu — *HSP - High Speed Data Converters*

ABSTRACT

System designers traditionally power the high-speed data converter in their systems from a low-noise, low-dropout linear regulator (LDO) in order to achieve the performance described in the analog-to-digital converter (ADC) data sheet. However, LDOs inherently are not very power efficient. Switching regulators, on the other hand, offer good power efficiency but typically come with higher output noise due to the switching nature of the dc/dc converter.

The ADS4149 converter is the low-power successor to the ADS6149 and was designed specifically for power-sensitive applications. This application report examines different options for powering the ADS4149 and compares the measured ac performance along with the power efficiency between them.

1 Power Supply Options

The ADS41xx evaluation module (EVM) is designed to allow the user to provide the 1.8-V supply voltage to the analog (1.8V VDDA) and digital (1.8V DVDD) supply pins of the ADS4149 in three different ways.

For best performance measurements without distortion of the power supply, the ADS4149EVM can be directly connected to an external 1.8-V power source. For a more system-like environment, it can be generated onboard from a 3.3-V rail using either the low-noise LDO (TPS79618) or the switching regulator (TPS62590) as shown in Figure 1. This allows the user to quickly change between configurations. The TPS62590 was chosen for low-output noise and small component size due to higher switching frequency and very high efficiency.

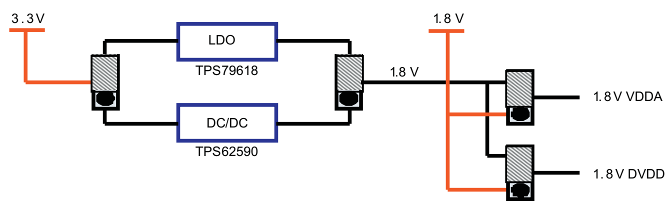


Figure 1. Power Supply Options on the ADS41xxEVM

2 Measurement Setup

The ac performance (i.e., SNR and SFDR) of the three different power supply configurations was measured by sweeping the input frequency from 10 MHz to 300 MHz. The sampling rate was set to 250 Msps, and the input signal path was configured as illustrated in Figure 2.

The ADS4149 was set up in serial mode (SPI) with LVDS output. Furthermore, "high-performance mode 1" (HP1, x03/x03) was enabled, and the internal ADC gain was set to 1 dB. In the FFT, 15 bins around dc were ignored because the close-in 1/f noise of the ADC artificially distorts the SNR measurement.

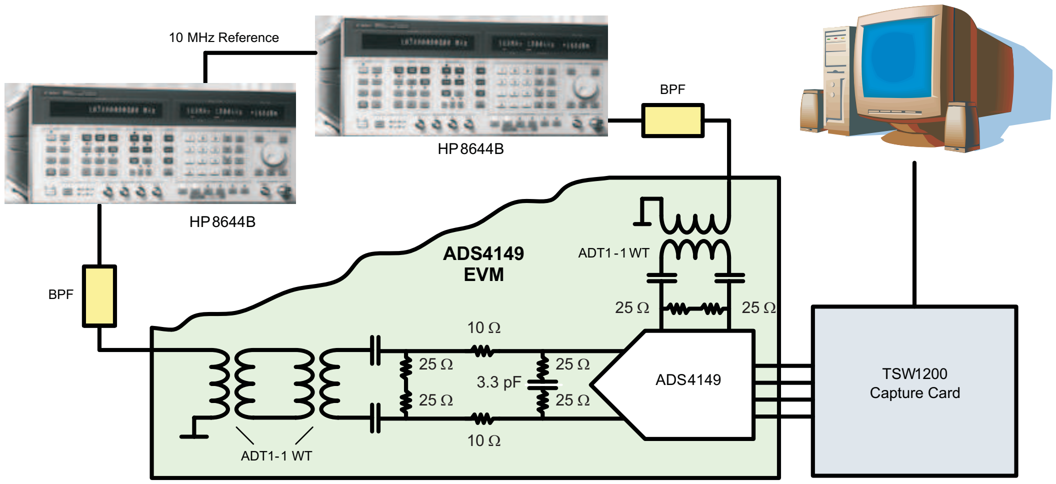
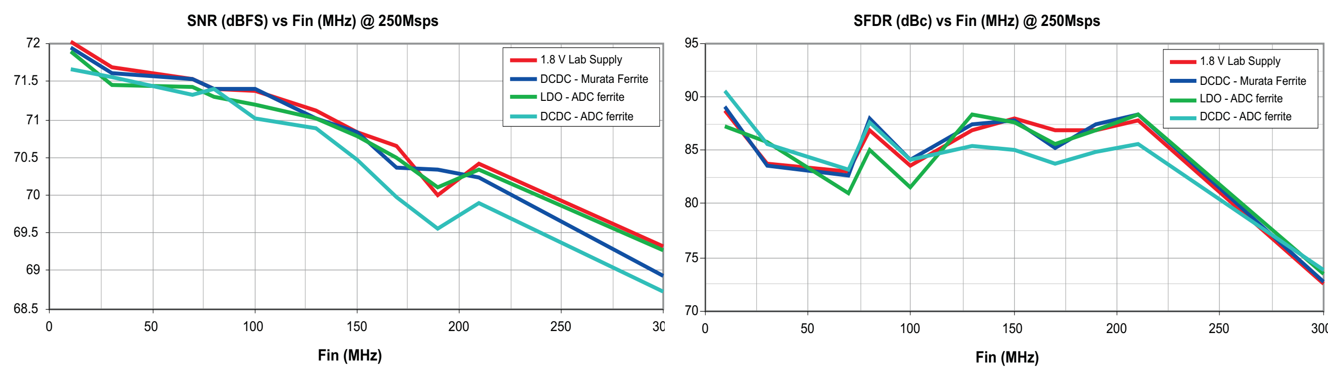


Figure 2. Measurement Setup With ADS4149 EVM

3 Test Results

Signal-to-noise ratio (SNR) and spur-free dynamic range (SFDR) sweeps across input frequencies are demonstrated in Figure 3. The experiment was repeated on two additional EVMs with similar results.

Best results were achieved when using an external 1.8-V supply although the performance with the low-noise LDO was nearly identical. Initially, the switching regulator showed degraded SNR and SFDR performance. However, after replacing the original ferrite bead, the SNR performance was similar up to an input frequency of approximately 200 MHz and degraded about 0.3 dB at 300 MHz. SFDR with the new bead matched the baseline very well across input frequencies.



ADC ferrite: original ferrite bead on ADS4149 EVM (EXC-ML32A680U)
Murata Ferrite: NFM31PC276B0J3

Figure 3. SNR and SFDR Sweeps With Three Different Power Supply Configurations

4 Ferrite Bead Selection

When choosing the ferrite bead, it is important to select one that has good wideband noise rejection and low dc resistance. Most importantly, it must have a high impedance (greater than approximately 25 Ω to 50 Ω) at the switching frequency of the dc/dc regulator.

The switching frequency of the TPS62590 is at 2.25 MHz and the Murata ferrite bead data sheet advertises very high insertion loss in that frequency range. Furthermore, it lists a maximum dc resistance of 5 mΩ, which corresponds well with the measured voltage drop of approximately 1 mV across the ferrite bead.

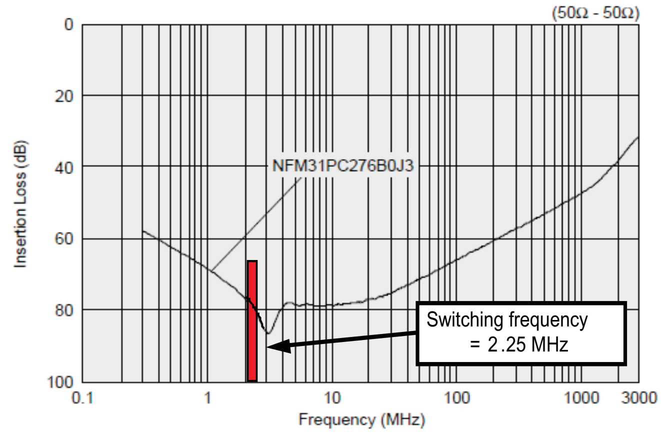


Figure 4. Impedance Characteristics of Murata Ferrite Over Frequency

The FFT plot comparisons in Figure 5 with an input signal of 10 MHz as well as in Figure 6 with an input signal of 170 MHz show no significant differences between the three power options.

When examining the normalized FFT plots, no evidence is visible of a spur at an offset equivalent to the switching frequency of 2.25 MHz from the TPS62590.

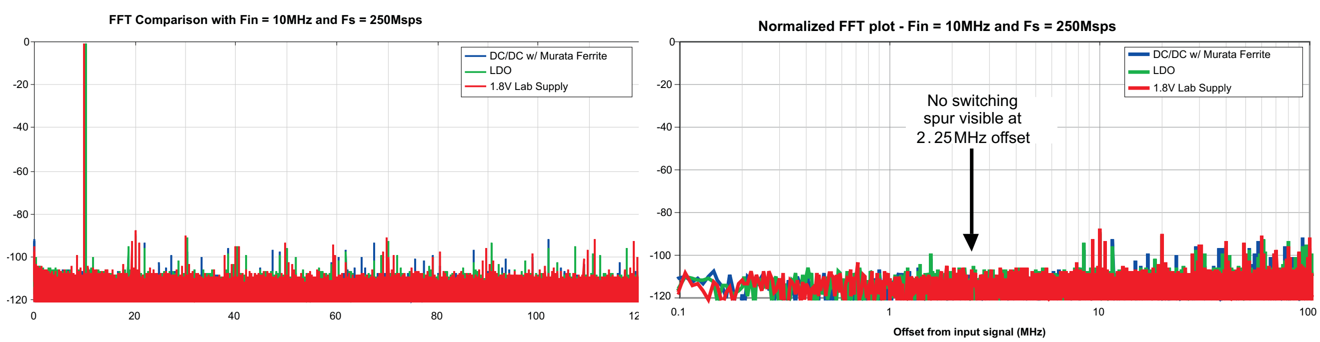


Figure 5. FFT (Left) and Normalized FFT (Right) Comparison Between Three Different Power Options With Input Signal of 10 MHz

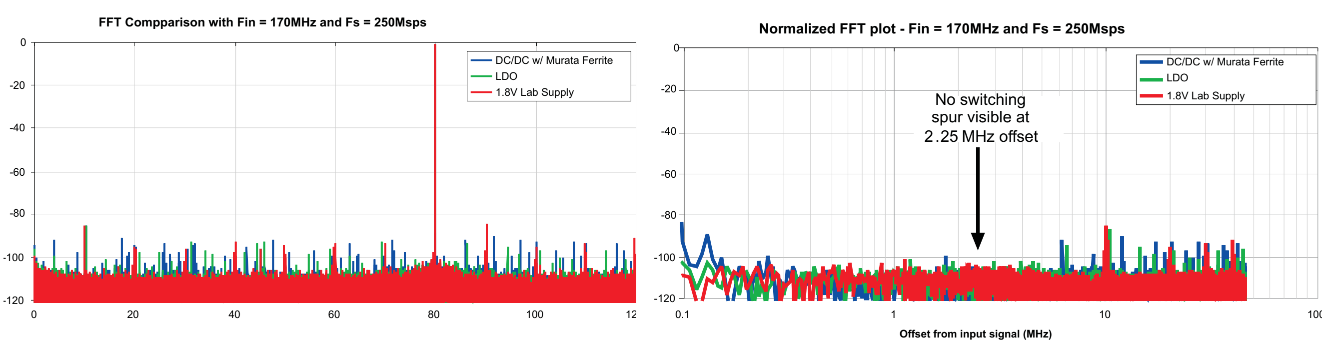


Figure 6. FFT (Left) and Normalized FFT (Right) Comparison Between Three Different Power Options With Input Signal of 170 MHz

5 Power Efficiency

The measured power consumption for the three power options is shown in Table 1. This power consumption depends on the sampling rate but is unaffected by the frequency of the input signal. The current numbers in Table 1 have the internal gain set to 1 dB and high-performance mode 1 enabled. LDO and dc/dc converter values also include their inherent quiescent current.

Table 1. Measured Power Consumption for Three Power Options

Setup	Current From Supply (mA)	Power Dissipation (mW)	Power Efficiency (%)
1.8-V Laboratory Supply	171 (from 1.8 V)	308	100
LDO	173 (from 3.3 V)	571	55.8
dc/dc	104 (from 3.3 V)	343	90.9

This comparison shows that when using the LDO, the LDO itself dissipates almost as much power as the ADS4149. The switching regulator option only wastes about 32 mW and achieves a very efficient power design.

The efficiency with the LDO can be further improved by stepping the input voltage down first from 3.3 V to 2.5 V or 2.2 V, for example. However, this increases system cost as well as size.

6 Further Optimization

To further reduce the switching noise generated by the TPS62590, a RC snubber was added between the switching output node and the inductor. The scope plot in Figure 8 shows output of the switching regulator with and without the RC snubber connected.

For proper component sizing when designing a RC snubber, see application report *Snubber Circuits: Theory, Design and Application* (SLUP100).

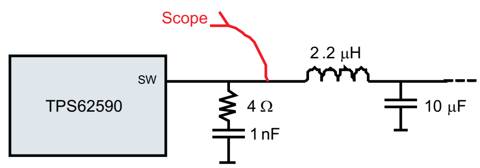


Figure 7. Placement of RC Snubber at dc/dc Converter Output

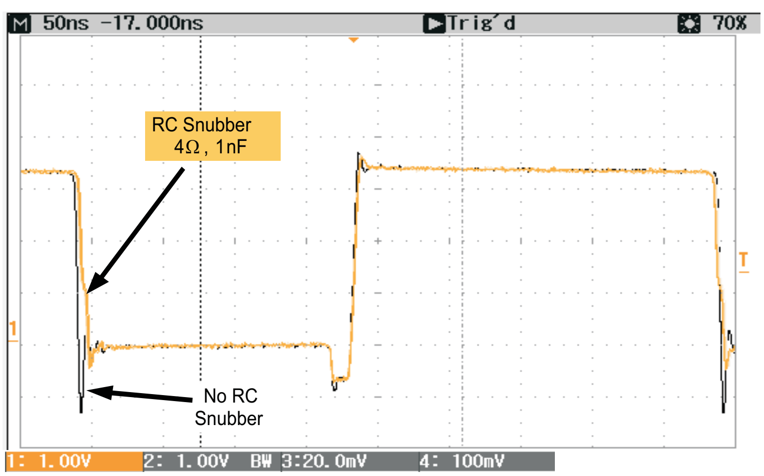


Figure 8. Scope Shot Comparison With and Without RC Snubber (R = 4 Ω, C = 1 nF)

Typically, reducing the overshoot and ringing at the output of the regulator also reduces the reactive energy that gets passed into the high-speed ADC. This reduces the magnitude of the switching spurs visible in the ADC FFT output spectrum while also lowering the close-in elevated noise around the fundamental.

In this case with the TPS62590, however, no significant change in SNR and SFDR performance was observed.

7 Summary

Best ac performance across input frequencies is achieved when using a low-noise LDO to power the ADS4149.The system designer, however, has to add significant extra headroom in the power budget of the high-speed data converter.

A design with a switching regulator can be optimized (right ferrite bead filter and possibly RC snubber) to closely match the ac performance with the LDO. The measurements in this application report show that when using a switching regulator to power the ADS4149 instead, the SNR degrades approximately 0.3 dB above an input frequency of 200 MHz, whereas the SFDR is fairly matched to the LDO. The overall design from a power perspective, however, runs about 35% more efficient – a tradeoff that may be well worth giving up less than half a dB of SNR.