TPD12S016 PCB Layout Guidelines for HDMI ESD

Roger Liang *High Volume Linear*

ABSTRACT

TPD12S016 is a multifunction ESD protection device that integrates a HDMI compliant 55mA load switch, three level shifting buffers, and hot plug detect function along with ESD protection for all pins connected to the HDMI connector, including four pairs of high speed differential lines. This device targets the mobile sector with the µQFN package and the set-top-box sector with the TSSOP package. This app note discusses optimized PCB design guidelines for both packages. With good layout design practice, TPD12S016 can fully support HDMI1.4 data rate at 3.4Gbps and minimize PCB real estate. In addition to using differential lines, other compensation structures for parasitic capacitance are presented as well.
In order to understand layout optimization, HDMI signals are explained in detail. TPD12S016's TSSOP and µQFN packages both take advantage of the single straight line TMDS pin-outs, which allow for simple 45° angle routings.

1 Introduction

TPS12S016 offers eight ultra low-capacitance ESD clamps, which allow HDMI 1.4 data rates to pass through while simultaneously providing IEC61000-4-2 (Level 4) ESD protection for all pins connected to the HDMI connector. The integrated ESD circuits provide good matching between each differential signal pair (data and clock); this is an advantage over discrete ESD solutions where variations between ESD protection clamps degrade the differential signal quality. TPD12S016 provides a current limited 5V output (5V_OUT) at 55mA for sourcing the HDMI power line. 5V_OUT and the hot plug detect (HPD) circuitry are controlled by the CT_HPD pin, which is independent of the level shifting buffer's control signal LS_OE. An internal 3.3V node powers the CEC pin, eliminating the need for a 3.3V on board supply. TPD12S016 integrates all the external termination resistors on the HPD, CEC, SCL, and SDA lines. The HPD_B port has a glitch filter to avoid false detection due to plug bouncing during HDMI connector insertion. Figure 1 shows a simplified circuit schematic and Figure 2 shows an application schematic using two GPIO for HDMI interface control.

Key features and benefits of the TPD12S016 include:

- Supports HDMI1.4 Data Rate
- Built-in HDMI compliant current limiting load switch
- Built-in pull-up and pull-down resistors compliant with HDMI1.4 spec
- Built-in hot-plug-detect
- Match Class D and Class C pin mapping
- Auto direction sensing level shifting buffer with integrated pull-ups and a one-shot circuit (drives at least 750pF load).

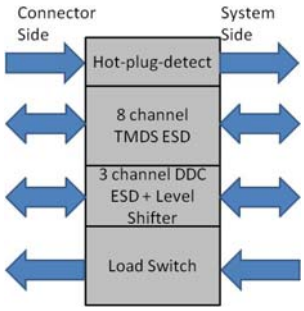

Figure 1. Circuit Schematic

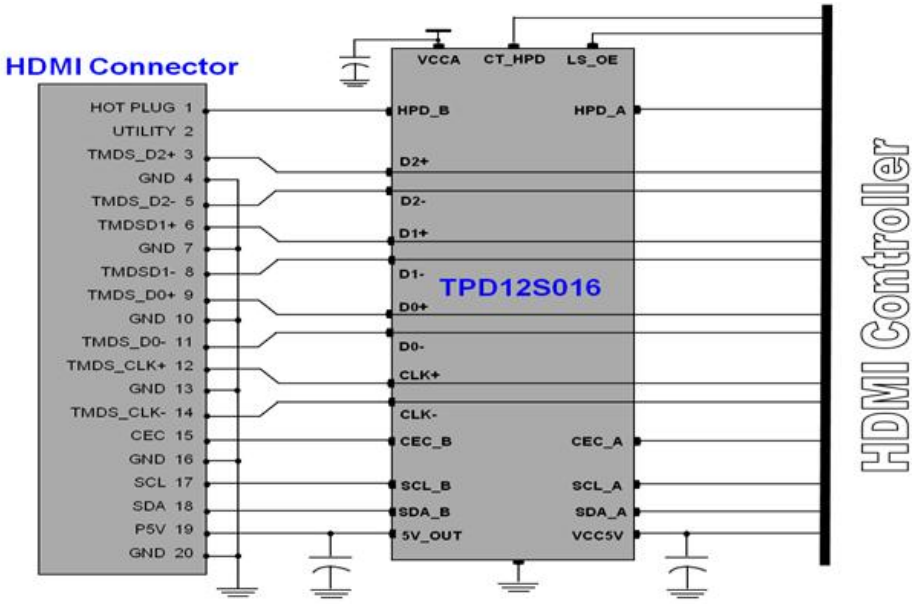

Figure 2. Application Schematic for HDMI controllers using two GPIO for interfacing

2 HDMI Signal Types

2.1 TMDS

There are four sets of high-speed Transition Minimalized Differential Signal (TMDS) lines in HDMI application, which include data lines D0±, D1±, D2±, and clock lines CLK±. According to HDMI 1.4 specification, CLK can reach a maximum speed of 340MHz, with maximum data throughput reaching 3.4Gbps on the data lines. During each clock cycle, a package of 10 bits of information is exchanged on the TMDS lines. The relatively high frequency of these signals makes routing of the lines critical. There a several things to keep in mind:

- The number of stubs should be kept to a minimum.
- Trace lengths should be kept to a minimum.
- Special care needs to be made to match length in all these lines.

Any significant trace length difference among the differential pairs will introduce signal skew, which could violate HDMI specification. Long trace lengths can increase time delay, increase EMI radiation, and corrupt signal integrity. The high speed lines can be routed differentially or separately. If the lines are routed through a noisy environment or if they have to be routed relatively long, it may be beneficial to route them differentially and make the pair 100Ω with respect to each other (not with the ground plane underneath). Otherwise, 50Ω trace impedance can be used and made with respect to the ground plane underneath.

2.2 DDC, HPD, CT_HPD/LS_OE, VCC5V/5V_OUT

The display data channel lines (DDC) are made up of SDA, SCL, and CEC. These lines have internal pull-up resistors and run at 400 kHz or less. The hot plug detect (HPD) signal is a single direction signal that indicates to a transmitter the presence of a receiver connected on the line. The CT_HPD and LS_OE control lines enable the HPD scheme and level shifters respectively. They are referenced to VCCA and have internal pull-down resistors. VCC5V and 5V_OUT are the input and output of the load switch respectively.

High speed trace consideration is not needed in routing any of these lines. Traces to and from these pins should be routed after those from the TDMS lines are routed first.

3 RKT package considerations

The RKT package is suitable for mobile applications where board space is a premium. The package length (4mm) closely matches that of the HDMI Type D receptacle footprint; placing TPD12S016RKT close to the HDMI connector not only makes routing easy but also increases system level ESD protection robustness. In an ESD event, the bulk of the energy would be dissipated through the ESD diodes inside TPD12S016RKT before excess energy has time to damage to other ICs on the board. Figure 3 shows the pin outs of the RKT package. Three routing layers are needed: one layer for the Transition Minimalized Differential Signal (TMDS) lines, Dx± and CLK±, and a pair of layers for other signal and power traces.

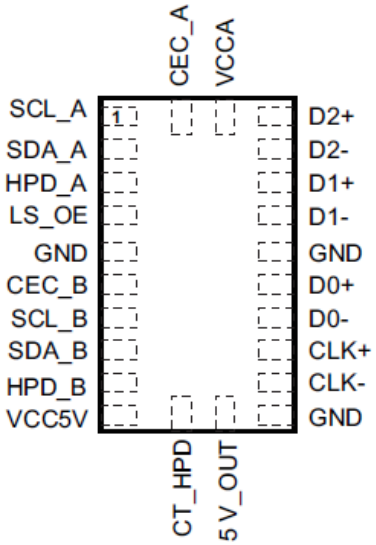

Figure 3. TPD12S016RKT Package pin out

An example RKT routing to a Type D receptacle pin out is discussed below. Figure 4 shows both the TPD12S016RKT and the Type D footprint on the top layer and the TMDS lines running through vias and routed on the bottom layer. Notice that since Type D receptacles have two rows of pins and that D1 and CLK has to be routed through the bottom layer in order to minimize trace length, it is good practice to route all differential pairs the same way in order to minimize signal skew between the pairs. When routing the differential traces to the HDMI controller, keep good differential trace practices as outlined in the appendix.

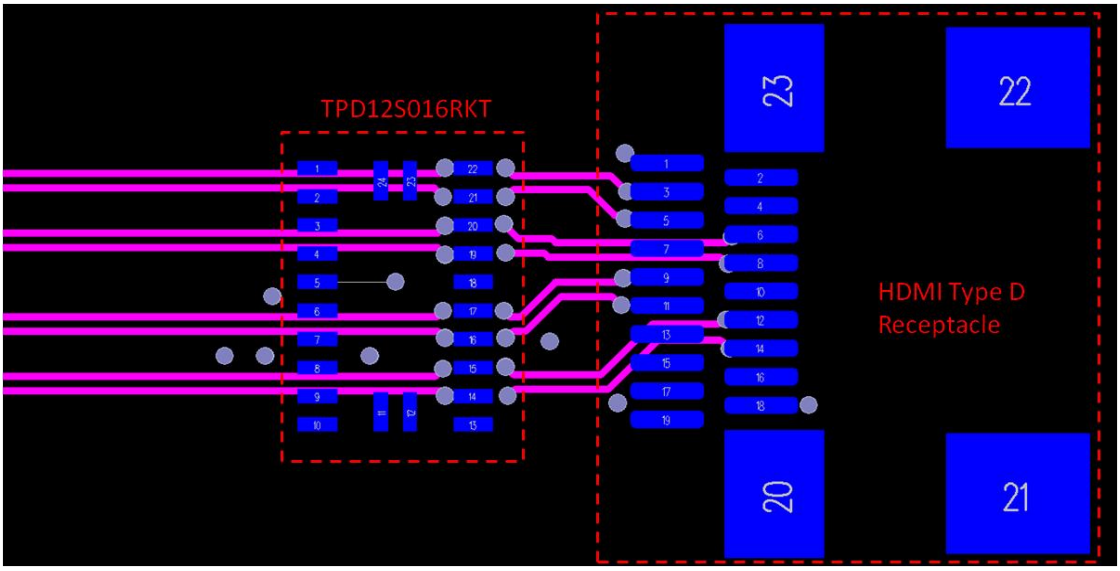

Figure 4. Layout of TMDS Lines Routed on the Bottom Layer

Figure 5 shows routing of the non-TMDS lines. Since these do not carry high speed signals, they can be routed with flexibility. Figure 6 shows a hybrid view, combining all three routing layers.

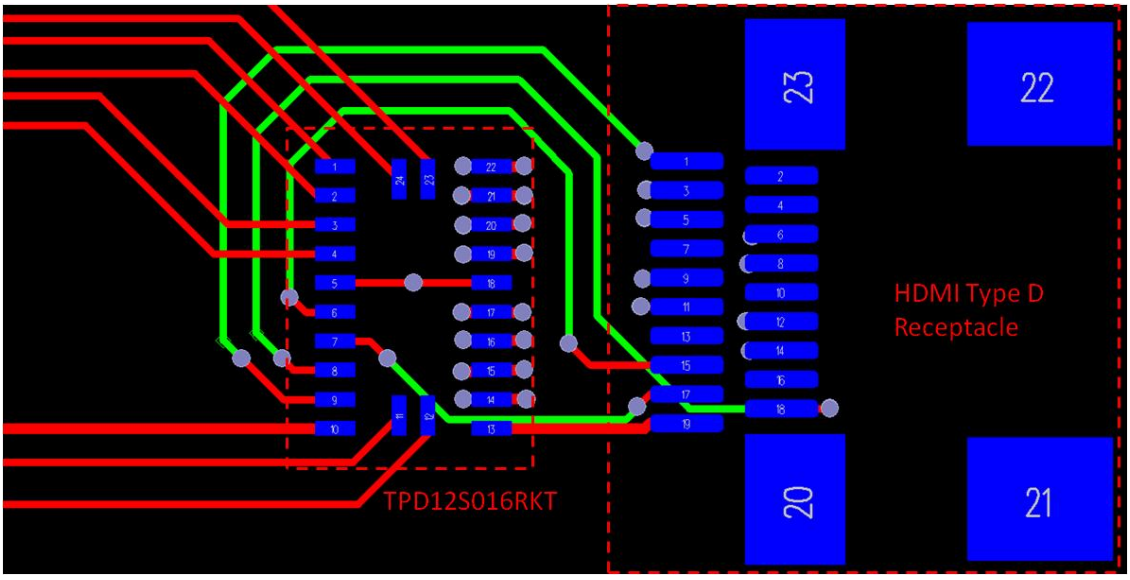

Figure 5. Layout of non-TMDS Lines

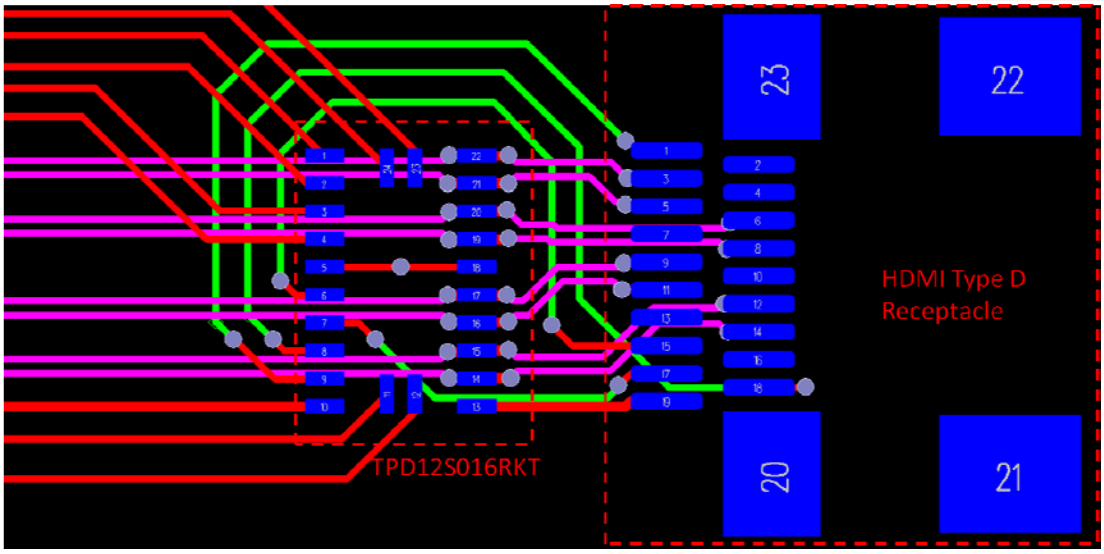

Figure 6. Layout of Hybrid Lines

4 PW package considerations

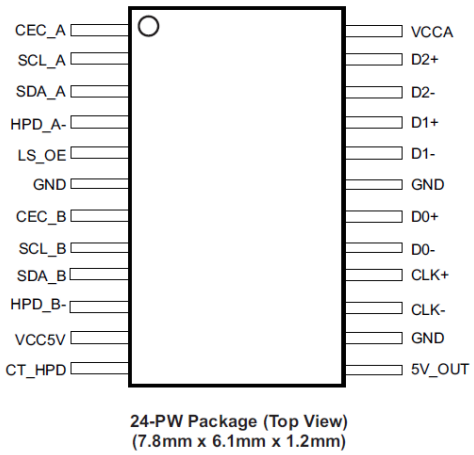

Figure 7. TPD12S016PW Package Pin Out

Figure 8 shows a layout example for the TPD12S016PW with HDMI Type A receptacle. Type C receptacle routing is done in a similar fashion; the TMDS lines would have to be brought in closer together because of the smaller pitch of the Type C receptacle. Since the PW package is larger and has no top or bottom pins on the footprint, TMDS traces can be routed straight through on the top layer and only two layers are needed for routing TMDS plus all other pins. When routing TMDS lines from the HDMI transmitter, through the TPD12S016PW, and to the HDMI connector, one needs to keep differential pairs tight and width gap consistent. Minimize trace lengths and do not create angles sharper than 45°. Refer to the appendix for differential routing guidelines.

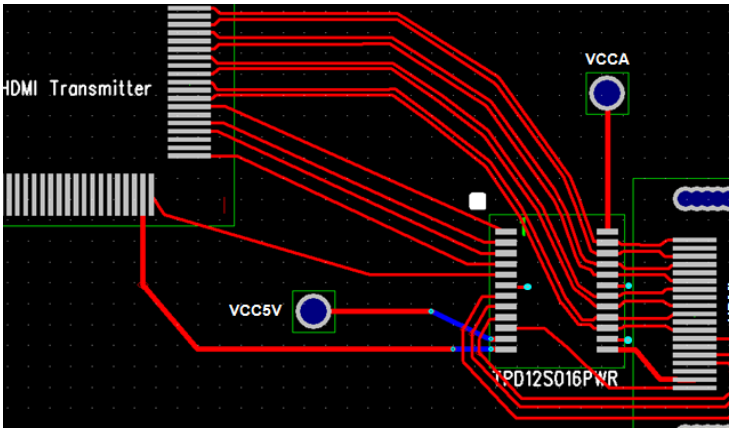

Figure 8. TPD12S016PW routing with Type A Receptacle

5 TPD12S016PW EVM Board

An EVM (evaluation module) was created for testing the TPD12S016PW package. This four layer board is shown below in Figure 9.

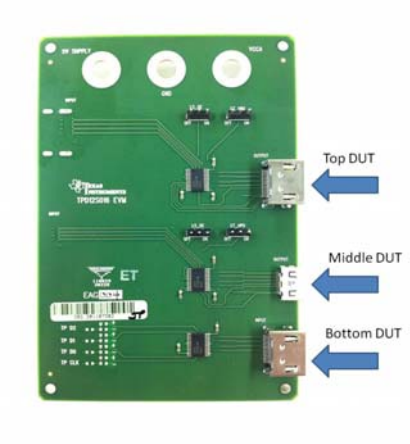

Figure 9. TPD12S016EVM

This EVM has three segments. The top segment of the layout uses HDMI Type A connectors. The middle segment has 2 HDMI Type C connectors. The connectors on the left side of the EVM are on the bottom of the board. The bottom segment is designed for user specified additional RC networks. This bottom board segment includes an HDMI Type A connector on one side and high speed traces fanned out for probe testing and loading on the other. Eye pattern testing is done for the top DUT; results are shown in Figure 10 and 11.

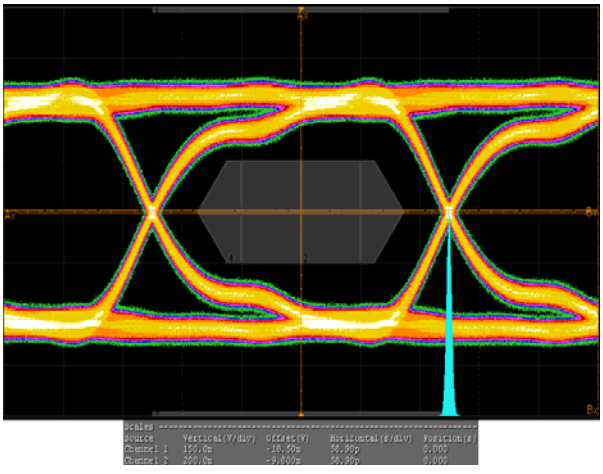

Figure 10. Eye diagram using EVM without TPD12S016 for the TMDS Lines at 1080p, 340MHz pixel clock, 3.4Gbps

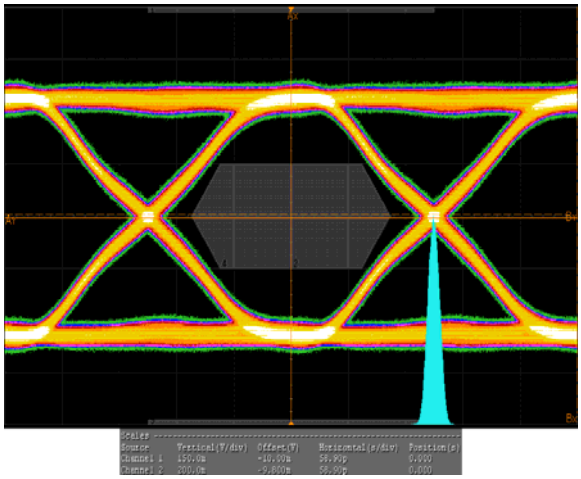

Figure 11. Eye diagram using EVM with TPD12S016 for the TMDS Lines at 1080p, 340MHz pixel clock, 3.4Gbps

5.1 Skinny Traces

Following HDMI compliance, differential impedance on the TMDS traces is fixed at 100Ω. Figure 12 shows a schematic representation of the elementary components of a lossless transmission line; in this case the differential trace is the transmission line. Shown in Equation 1, Z_O is the characteristic impedance of the line, L is the inductance per unit length, and C is the capacitance per unit length. Our goal is to keep Z_O at a constant 100Ω throughout the entirety of the differential traces.

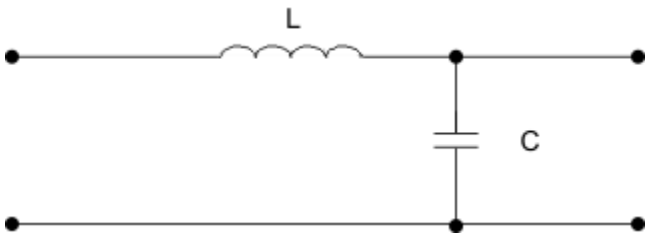

Figure 12. Lossless Transmission Line Circuit Representation

$$Z_O = \sqrt{\frac{L}{C}} \qquad \textit{Equation 1}$$

Unfortunately, IC pads add capacitive coupling, which decreases Z_O in that general region. This undesirable effect can be fixed by adding inductive components. One solution to increase inductance is implementing special differential traces with higher Z_O called “skinny traces”, which not only provide the inductive effect but also decrease capacitive coupling between the differential trace. Skinny traces help increasing the effective Z_O near the IC back to 100Ω. As a rule, skinny traces Z_O should be designed to be 150Ω in simulation and their length should be one to two times that of the IC pads. Given the exact parasitic IC pad capacitance value, TDR simulation tools such as Hyperlynx should give optimum skinny trace impedance and length. TPD12S016PW EVM is designed using skinny traces and Figure 13 shows the dimensions.

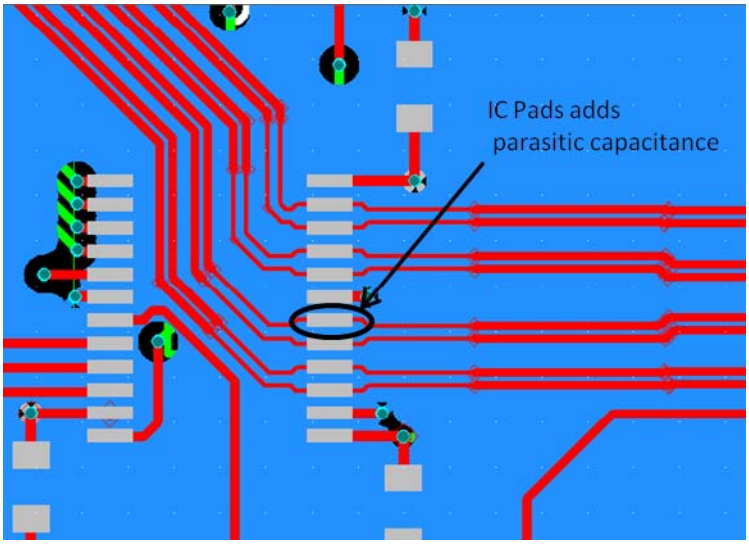

Figure 13. Skinny traces for TMDS lines

During simulation, parasitic capacitance of the IC pad is combined with 150Ω of skinny trace to produce equivalent impedance at 100Ω. As shown in the eye diagram in Figure 14, skinny traces make the edges faster and the eye open wider.

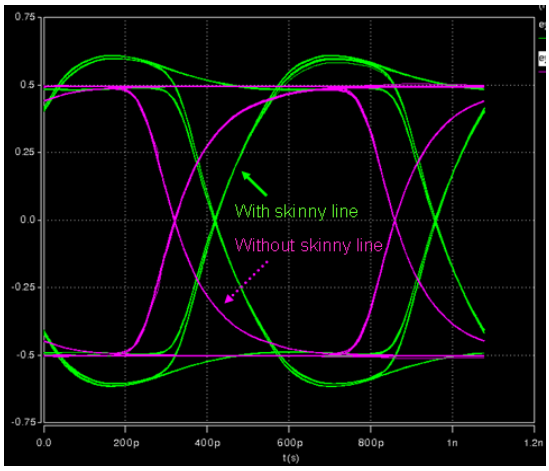

Figure 14. Simulated Eye-diagrams with and without Skinny Traces

A.1 Appendix

Differential Traces

When designing differential traces for a certain characteristic impedance, a number of design software tools can be used to obtain a reasonable estimate of the trace widths, separations, and thickness for any given impedance. Since trace thickness is not an input for most PCB layout tools, it could be entered into an attached ReadMe file when submitting the design to the board shop. Another method would be not to submit a thickness dimension; instead, with a given width and spacing derived from simulation, ask manufacturer to "bake" the board to the right amount of thickness for a given characteristic impedance. The latter method is preferred. Table 1 shows the original dimensions calculated from SaturnPCB design tools and the returned dimensions from board shop. Most board shops have impedance matching capabilities of +/- 10%.

Table 1. Manufacturer's Differential Traces Recommendations

Impedance (Ω)	Tolerance (Ω)	Type	Org Line Width	Org Spacing	Finished Line Width	Finished Line Spacing	Simulated Z (Ω)
100	+/-10	Differential	9.01	4	8.25	4.76	100.136
150	+/-15	Differential	5.15	7.85	3.625	9.38	149.759

Via and Corners and other Considerations

There are four sets of high-speed TMDS lines per each IC. Since data on these lines reach a max of 3.4Gbps, routing is critical. The number of vias should be minimized on TMDS lines. If a via has to be used, its pad size should be the same as that of the trace width. For example, a via on the 9.1 mils differential trace in TPD12S016PWREVM has a pad size of 9 mils and a drill size of 4 mils. As a rule-of-thumb, anti-pads of radii 15 mils (separation between via pad and surrounding copper in the ground and power layer) are used to decrease parasitic capacitance, which is inversely proportional to the radius of the anti-pad. Using oversized anti-pads takes away the ground layer's shielding ability. This trade off can be best estimated in simulation tools like Hyperlynx. In Figure 15, the ground layer is shown in blue and TMDS traces are shown in red.

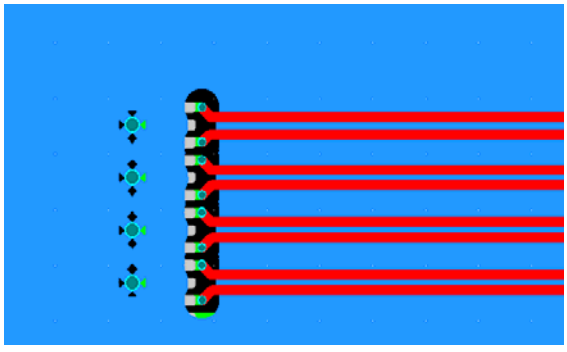

Figure 15. High speed TMDS lines routing to HDMI Connector

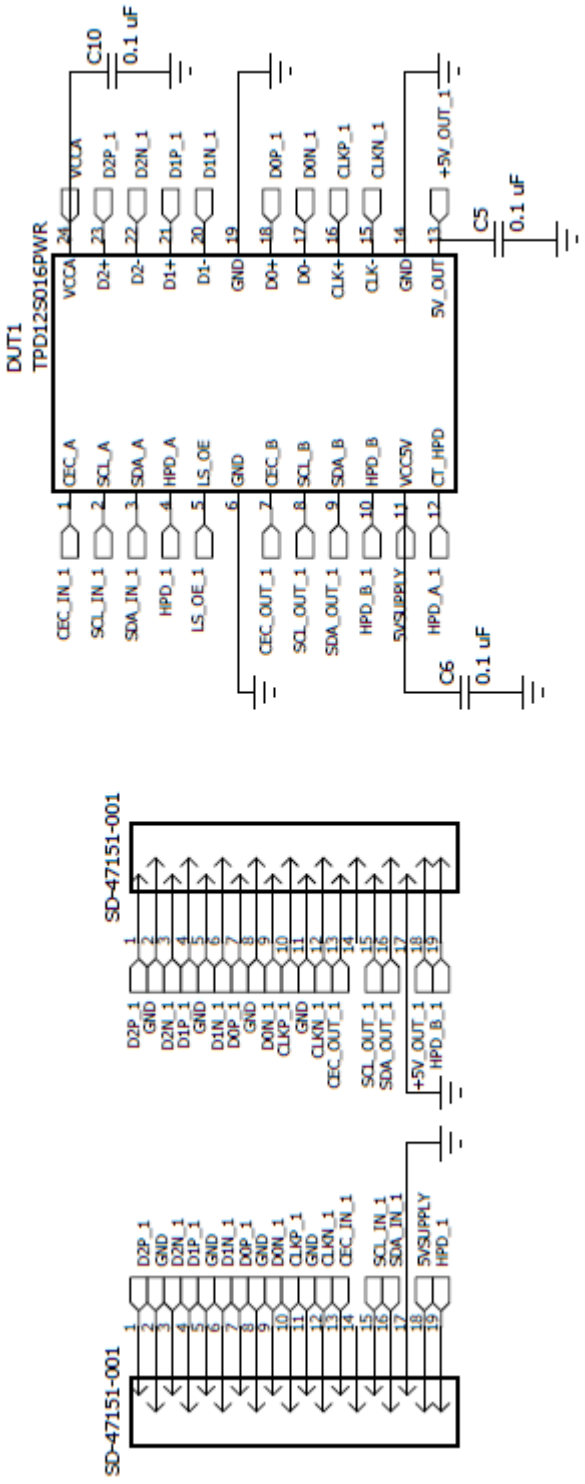

Figure 16. EVM Top Segment Schematic

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Mobile Processors	www.ti.com/omap		
Wireless Connectivity	www.ti.com/wirelessconnectivity		
	TI E2E Community Home Page		e2e.ti.com

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265