Application Report
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Configuring the bq27010/210 for Gas Gauge Applications

Battery Management

ABSTRACT

Accurate performance of the bq27x10 gas gauge requires that the 10 user-configurable EEPROM coefficients be programmed to values that reflect the appropriate host system and battery characteristics. This application report provides the basis for determining the optimal EEPROM coefficients from the host system operational characteristics and battery characterization data. Appendix A specifically addresses how to determine the EDV1 threshold compensation with load and temperature from battery characterization data. Appendix B shows how to determine the capacity compensation with load, temperature, and age from battery characterization data.

Contents

List of Figures

1 Programming the EEPROM

A user can program 10 EEPROM locations to optimize the setup for the specific battery and host characteristics. These EEPROM locations are mapped directly to RAM locations 0x76 to 0x7f. These locations cannot be written by the host except during a special test mode. This test mode can be entered by writing 0xdd to address 0x6e. This action will allow write access to these RAM locations and subsequent transfer of the RAM content into EEPROM. The bq27x10 processing is inhibited while 0x6e contains 0xdd. When EEPROM programming is complete, address 0x6e must be written back to 0x00.

The actual EEPROM programming is accomplished by reading each address (after previously writing it with the desired data) and then applying a programming pulse of 21-V amplitude for 10-to-100 ms to the

PGM pin on the bq27x10. The programming pulse must meet the 0.5- to 1.5-ms rise-time and fall-time requirements for accurate programming. After all programming changes have been accomplished, 0x00 must be written to address 0x6e. This action disables write access to the EEPROM values, resets the bq27x10, and allows normal execution to resume. This action does not force the new EEPROM values to take effect. A full reset command (FRST) should be sent to force the gauge to use the new EEPROM values.

When the gauge executes a reset, it first loads the RAM locations 0x76 to 0x7f from the EEPROM and then verifies the values of various checksums. If they are correct, a partial reset is performed. If they are incorrect, or a full reset is forced, the coefficients in 0x76 to 0x7f are copied into mirrored locations 0x46 to 0x4f. The gauge then executes normally, using the coefficients located in the 0x46 to 0x4f RAM space. The bq27x10 has special commands that allow the host to update the 0x46 to 0x4f RAM space to allow operation with different coefficients than those programmed in EEPROM. The gauge preserves these updated values if at all possible and regularly performs a checksum on the 0x46 to 0x4f RAM values. If the checksum ever fails, the gauge is reset, and the 0x46 to 0x4f RAM values are reloaded with the EEPROM values. The gauge notifies the host that the values have been updated by setting the INIT bit in the MODE register. The host can ignore the INIT bit if no coefficients need to be set differently than the original EEPROM values.

1.1 Initial Last Measured Discharge (ILMD)

This value is the design capacity (DC) of the battery. The high byte of Last Measured Discharge (LMD) is set equal to ILMD and the low byte of LMD is set to zero on a full reset. LMD is then used for the 100% full capacity reference. LMD is the no-load (or light-load) capacity of the battery and can be set to the manufacturer's C/5 rated value. The bq27x10 subsequently updates LMD with the learned capacity of the battery. A reset without RAM corruption (RBI maintains the RAM content) leaves the LMD value at its learned value and does not cause it to be reinitialized to ILMD. Units for ILMD are 256×3.57 μVh per least significant bit (LSB).

The EEPROM value for ILMD is programmed in address 0x76. The formula for determining the EEPROM value for ILMD is:

$$\text{ILMD} = \text{DesignCapaciaty(mAh)} \times \frac{R_S(\text{m}\Omega)}{256 \times 3.57\ \mu\text{Vh}} \quad (1)$$

Example: If the battery design capacity is 1000 mAh and the sense resistor is 20 mΩ, the value to be programmed in ILMD would be: 1000 mAh × 20 mΩ/(256 × 3.57μVh) = 21.9. The next smaller value is 21 decimal, or 15 hexadecimal. Setting ILMD to 0x15 initializes LMD to 0x1500 (5376 decimal), or 960 mAh with a 20-mΩ sense resistor.

1.2 Scaled End-of-Discharge Voltage Final (SEDVF)

The end-of-discharge voltage final (EDVF) threshold is established by the value programmed into the SEDVF location in EEPROM. This value should be set to the voltage that the host system requires for minimum operating voltage plus some safety factor if not already built into the system minimum voltage requirement. This is the voltage threshold where the gauge should report that the battery has zero remaining capacity. NAC is adjusted to zero during a discharge if this voltage threshold is reached. EDVF is a fixed value and is not compensated with discharge rate or temperature. Units for SEDVF are 8 mV, with a 2048-mV offset.

The EEPROM value for SEDVF is programmed in address 0x77. The formula for determining the EEPROM value for SEDVF is:

$$\text{SEDVF} = \frac{\text{EDVF (mV)}}{8} - 256 \quad (2)$$

Example: To set the EDVF threshold to 3000 mV, the value to be programmed in SEDVF is: 3000mV/8 – 256 = 119 decimal or 77 hexadecimal.

1.3 Scaled End-of-Discharge Voltage First (SEDV1)

The EDV1 threshold used by the bq27x10 gauge is compensated as a function of discharge rate and temperature. The EDV1 threshold is equal to the no-load value programmed in SEDV1 minus a reduction that varies linearly with load current. The rate that EDV1 is reduced with load current is determined by the DEDV and EDVT compensation coefficients described later in this document. The SEDV1 no-load threshold and the DEDV and EDVT compensation coefficients should be derived from actual cell discharge data and is discussed in Appendix A. A proper choice of these values will adjust the EDV1 threshold so that 6.25% of design capacity remains when this threshold is reached, regardless of discharge rate or temperature. This threshold is used to terminate a learning cycle. The additional capacity remaining after the EDV1 threshold is reached is not measured. The learned capacity is adjusted to include the DC $\times$ 6.25% unmeasured capacity remaining; so, setting the EDV1 threshold to a value appropriate to 6.25% of design capacity remaining is important for good gauge accuracy. Units for SEDV1 are 8 mV, with a 2048-mV offset.

The EEPROM value for SEDV1 is programmed in address 0x78. The formula for determining the EEPROM value for SEDV1 is:

$$\text{SEDV1} = \frac{\text{No-load EDV1(mV)}}{8} - 256 \tag{3}$$

Example: To set the no-load EDV1 threshold to 3400 mV, the value to be programmed in SEDV1 is: 3400mV/8 – 256 = 169 decimal or a9 hexadecimal.

1.4 Initial Standby Load Current and EDV1 Temperature Compensation (ISLC/EDVT)

The initial standby load current (ISLC) value programmed in EEPROM should be the estimated host system standby load current, but must be less than half the minimum expected operational load current. The bq27x10 takes any non-zero current value that is less than or equal to two times the programmed standby load current value and computes a weighted average with the previous standby load current calculation. This allows the reported standby current to reflect the actual measured average standby current, and the value is used to compute Standby Time-to-Empty. The bq27x10 also disables learning a new LMD if a learning discharge cycle terminates at EDV1 when the average discharge current is less than or equal to two times the programmed standby load current value. This prevents learning an inflated capacity value during a standby load condition. Units for ISLC are 57.1 μV per LSB.

The EEPROM value for ISLC is programmed in the upper nibble of address 0x79. ISLC has a maximum value of 7. The formula for determining the EEPROM value for ISLC is:

$$\text{ISLC[2 : 0]} = \frac{\text{DesignStdbyCurrent(mA)} \times R_S(\text{m}\Omega)}{57.1\ \mu\text{V}} \tag{4}$$

The end-of-discharge temperature (EDVT) coefficient determines the affect of temperature on the EDV1 compensation. If EDVT=0, there is no adjustment of EDV1 with temperature. The temperature compensation adjustment is made by increasing the programmed EDV1 discharge rate compensation, so that the temperature adjustment of EDV1 is proportional to AI. The EDVT compensation increases the EDV1 rate compensation gain (DEDV) programmed in 0x7D in increments of 0.78% (EDVT/128) per degree for each degree below the TOFF threshold programmed in TCOMP. How to determine the appropriate EDVT coefficient from the battery characterization data is discussed in Appendix A.

The EEPROM value for EDVT is programmed in the lower nibble of address 0x79. The formula for determining the EEPROM value for ISLC is:

EDVT[3:0] = 1.28 $\times$ [%DEDV.incr.per.degC]

The EEPROM values for EDVT and ISLC are combined into a single byte and programmed in address 0x79.

Example: To set the ISLC value to 20 mA with a 20-mΩ sense resistor, the value to be programmed in the upper nibble of ISLC/EDVT is: 20 mA $\times$ 20 mΩ/57.1 μV = 7. The bq27x10 disqualifies a learning cycle if the measured discharge current is less than or equal to 40 mA when EDV1 is detected. To set the EDVT coefficient to increase the EDV1 discharge rate compensation by 6.25% per degree, the lower nibble of ISLC/EDVT should be set to 1.28 $\times$ 6.25 = 8. ISLC/EDVT would be programmed to 0x78 for ISLC of 20 mA and EDVT of 6.25% rate reduction increase of EDV1 per degree. Bit 7 of ISLC/EDVT should always be zero.

1.5 Digital Magnitude Filter and Self-Discharge Rate (DMFSD)

The Digital Magnitude Filter (DMF) threshold sets the minimum signal level across the sense resistor that is to be measured. If the signal level measured by the bq27x10 is less than this threshold, the signal is ignored and assumed to be zero. If the signal level is greater than or equal to this threshold, the signal is accepted as a valid measurement. The DMF prevents a small measurement offset due to IC characteristics as well as any additional offset due to PCB layout from accumulating to a large error over a long period of time. If the DMF value is set to zero, then all signal levels are treated as valid. A typical value for the DMF threshold is 15 μV. The formula for determining the EEPROM value for DMF is:

$$DMF[3:0] = \frac{DesignThreshold}{4.9\ \mu V} \quad (5)$$

The self-discharge rate sets the self-discharge capacity loss per day in a temperature window of 20°C to 30°C when the battery is not being charged. This rate is automatically compensated for temperature by doubling the programmed rate for every 10°C decade hotter or halving the programmed rate for every 10°C decade colder. A typical value for lithium-ion batteries is 0.2% per day at 25°C. The formula for determining the EEPROM value for SD is:

$$SD[3:0] = \frac{1.61}{DesignSD} \quad (6)$$

The EEPROM values for DMF and SD are combined into a single byte and programmed in address 0x7a.

Example: To set the DMF threshold to 14.7 μV and the self-discharge rate to 0.2% per day, the value to be programmed in the upper nibble of DMFSD is: 14.7 μV/4.9 μV = 3, and the value to be programmed in the lower nibble of DMFSD is: 1.61/0.2 = 8. Setting DMFSD = 0x38 sets the DMF threshold to 14.7 μV and the self-discharge rate to 0.2% per day at 25°C.

1.6 Taper Current (TAPER)

The taper current threshold sets the threshold that charging current must fall below for the bq27x10 to detect that the battery has received a full charge. Voltage must also meet the qualifying threshold that is set in PKCFG to qualify as a valid taper current charge termination. Typical values for the taper threshold are in the range of DC/20 to DC/10. The value programmed in the bq27x10 should be a little higher in value than the expected charge termination current of the charger. If the charger terminates before the bq27x10 can detect the charge termination, the bq27x10 does not adjust the displayed capacity to the full (NAC=LMD) condition. Units for TAPER are 228 μV per LSB.

The taper current threshold is programmed in bits 6–0 of TAPER in address 0x7b. Bit 7 of address 0x7b is reserved for enabling the capacity fade estimate algorithm. The formula for determining the EEPROM value for TAPER is:

$$TAPER[6:0] = \frac{DesignTaperCurrent(mA) \times R_S(m\Omega)}{228\ \mu V} \quad (7)$$

Bit 7 of TAPER is used to enable or disable application of a capacity fade estimate. This is useful if the battery spends considerable time without a capacity learning cycle. If bit 7 = 0, capacity aging is disabled. If bit 7 = 1, two separate aging estimates are made. The primary adjustment is made if substantial charge and discharge activity occurs without a learning cycle. Every time CYCL (cycle count since last learning cycle) is incremented by 2, LMD is reduced by ILMD × 256/1024 (0.1% of design capacity). A secondary adjustment is made if considerable time passes with no significant charge or discharge activity. LMD is reduced by ILMD × 256/1024(0.1% of design capacity) every time that NAC is reduced by 1.56% due to self-discharge. For example, if the self-discharge estimate is programmed for 0.2%/day, LMD is reduced by 0.1% of design capacity every 8 days of idle operation at 25°C. The rate will double or half every 10°C temperature change, just like the self-discharge estimate. Whenever a learning cycle occurs, LMD is replaced with the new learned value, CYCL is cleared, and the aging computations start over using the new learned LMD value as a starting point.

Example: To set the taper charge termination threshold to 100 mA: TAPER=100 mA × 20 mΩ/228 μV = 8.8. The EEPROM value for TAPER should be programmed to 0x09 or 0x89, depending on whether the capacity fade option is to be enabled. This programs the taper current threshold to 102.6 mA.

1.7 Pack Configuration (PKCFG)

The pack configuration value is used to set five different user options.

PKCFG[7]: Bit 7 sets the initial state of the GPIO pin when power is applied to the bq27x10. The host can write to the MODE register to change the GPIO configuration at any time if the GPIO configuration needs to be dynamically changed. If bit 7 = 0, then the GPIO is initialized as an open-drain output. If bit 7 = 1, then the GPIO is initialized as an input. If the GPIO pin is unused, the preferred setup is to program bit 7 = 0 to set the GPIO pin as an output. The GPSTAT bit in MODE register is set to a 1 on POR and turns the open-drain FET output *off*.

PKCFG[6:5]: Bits 6 (QV1) and 5 (QV0) are used to set the qualification voltage threshold for a current taper charge termination. VOLT must be greater than or equal to the threshold determined by the QV1 and QV0 setup. The qualification voltage can be programmed to 3968 mV, 4016 mV, 4064 mV, or 4112 mV (see Table 3 in data sheet SLUS707). The qualification voltage chosen should be as high as possible to minimize the chance for any premature termination due to a reduction in charge current from some system or charger issue that may occur before the battery is full. For example, if the system has an operating mode that robs the charger of most of its available power and the remaining charge current for the battery is less than the taper current termination threshold, the taper qualification voltage threshold can prevent a possible false charge termination detection. The qualification voltage threshold should not be set so high that the tolerance of the charger voltage and measurement accuracy of the bq27x10 can prevent the reported voltage from exceeding the taper qualification voltage threshold.

Example: If the charger were set for 4200 mV nominal, with a ±2% tolerance, the minimum charger voltage would be 4116 mV. The voltage measurement accuracy of the bq27x10 is ±20 mV; so, an applied 4116-mV source could be measured as low as 4096 mV. The taper qualification threshold should be set to 4064 mV, as the highest 4112-mV setting is too high with worst-case tolerances. This selection requires setting QV1 (bit 6) = 1 and QV0 (bit 5) = 0.

PKCFG[4-2]: These bits are used to store an average board offset value. The value of the board offset is largely determined by the PCB layout. This offset value is added to the internal compensated offset to achieve a more accurate measurement of the voltage across the sense resistor. The board offset value is a signed number with a resolution of 2.45 µV per bit. The maximum positive offset value that can be stored is 7.35 µV with PKCFG[4-2] = 011. The maximum negative offset value that can be stored is –9.8 µV with PKCFG[4-2] = 100. The offset can be computed by measuring the total offset of the board plus gauge with no charge or discharge current flowing and subtracting the offset of just the gauge alone. Built-in offset commands in the bq27x10 allow measurement of these values. The total board plus gauge offset can be measured by performing a Compute External Offset (CEO) command. The user must first ensure that no charge or discharge current is flowing. Then set MODE[5]=1 and write the command key of 0x56 to address 0x00 to perform the CEO command. The result can be read after about 5.5 seconds in 0x5f-5e. The value is a signed number with LSB resolution of 1.225 µV. The gauge offset value can be similarly obtained by performing a Compute Internal Offset (CIO) command. This command is performed by setting MODE[4]=1 and then writing the command key of 0x56 to address 0x00. After about 5.5 seconds, the result can be read from 0x5f-5e and subtracted from the CEO reading to obtain the board offset value. If the board offset exceeds the compensation range, use the maximum positive or negative compensation value as appropriate for maximum accuracy. An excessive board offset indicates that a better board design could be achieved with some improvement in measurement accuracy, especially of small charge and discharge currents. The board offset value should be measured several times on each of several different boards to determine a good average value to use for the production lot. Measurement of board offset for each unit should not be required.

PKCFG[1]: This bit (DCFIX) can be used to select a fixed discharge rate compensation value and to allow the DCOMP location in EEPROM to be used for a customer identification or serial number. If DCFIX = 0, DCOMP specifies the discharge compensation value to be used in computing CAC and ARTTE. If DCFIX = 1, then a fixed default compensation value for DCOMP is used and the DCOMP location in EEPROM is free for the user to program to any desired value. The fixed default compensation value is equal to 5.08% of the discharge current that exceeds C/2. If DCFIX = 1, the corresponding DCOMP value of 0x6C initializes the 0x4e RAM address and the value in 0x7e is ignored.

PKCFG[0]: This bit (TCFIX) can be used to select a fixed temperature compensation value and to allow the TCOMP location in EEPROM to be used for a customer identification or serial number. If TCFIX = 0, TCOMP specifies the temperature compensation value to be used in computing CAC and ARTTE. If TCFIX = 1, then the TCOMP location in EEPROM is free for the user to program to any desired value. The default temperature compensation value is a 25% increase in the discharge compensation gain (DCGN) per °C below 12°C. If TCFIX = 1, the corresponding TCOMP value of 0x46 initializes the 0x4f RAM address and the value in 0x7f is ignored.

The EEPROM bit values for the desired PKCFG options should be combined into a single hexadecimal value and then programmed in address 0x7c.

Example: To program PKCFG for unused GPIO pin, 4064-mV taper qualification voltage, board offset of –4.9 μV, and use TCOMP and DCOMP for customer identification information, the programming should be set to 01011011 binary, or 0x5b.

1.8 Gain Age Factor and Delta EDV1 (GAF/DEDV)

The gain age factor (GAF) adjusts the rate at which CAC and FCAC are reduced from NAC and LMD respectively with age (Cycle Count Total). It does not have any affect on the EDV1 threshold compensation. The capacity compensation with age is accomplished by linearly increasing the discharge compensation gain factor (DCGN) programmed in DCOMP with cycle count. If GAF=1, the compensation increases with cycle count at a rate such that when CYCT=192, the capacity reduction is the same as that due to the programmed cold temperature compensation at a temperature of 12°C below the TOFF value programmed in TCOMP. The age compensation occurs 2 or 3 times faster with cycle count if GAF equals 2 or 3, respectively. Programming GAF=1 should give reasonably conservative results for most applications. There is no compensation with cycle count if GAF=0. The age compensation method is based on equating the capacity reduction due to the expected impedance increase with cycle count with the expected increase in impedance due to operation at cold temperature. The compensation equations and methodology for determining the various compensation coefficients are found in Appendix B. GAF is programmed in the upper 2 bits of EEPROM address 0x7d.

The delta end-of-discharge (DEDV) compensation factor adjusts the compensation of the EDV1 threshold with load current. The EDV1 threshold will be a fixed (uncompensated) value if DEDV = 0. Determination of the appropriate DEDV compensation factor is discussed in Appendix A. The value programmed in EEPROM is in units of 8 mV reduction in EDV1 per 1C-rate current.

$$\mathrm{DEDV}[6:0] = \frac{\mathrm{EDV1reduction.per.C.rate}}{8\ \mathrm{mV}} \tag{8}$$

The EEPROM values for GAF and DEDV are combined into a single byte and programmed in address 0x7d.

Example: To program GAF = 1 and an EDV1 reduction by 92 mV at a load current of C/2 (at nominal temperatures), then the values to be programmed into the upper 2 bits are 01 binary (GAF = 1) and the lower 6 bits are 010111 binary (DEDV = 184 mV/8 = 23 decimal = 17 hexadecimal = 010111 binary). Combining these values into a single byte yields 01010111 binary or 0x57.

1.9 Discharge Rate Compensation (DCOMP)

The discharge rate compensation (DCOMP) factor adjusts the rate at which CAC and FCAC are reduced from NAC and LMD respectively with Average Current (AI). Appendix B gives the compensation equations and discusses how to establish the best compensation coefficients from battery characterization data. The EEPROM value programmed in 0x7e can alternatively be used for a customer identification or serial number if DCFIX (bit 1 in PKCFG) is set to 1. When this option is used, a default discharge compensation gain (DCGN) of 5.08% of the discharge current that exceeds a discharge compensation offset (DCOFF) of C/2 is used for the discharge rate compensation factor and the value in the DCOMP location is ignored. The default discharge rate compensation is equivalent to programming DCOMP with 0x6C.

The EEPROM value for DCOMP is programmed in address 0x7e. The formulas for determining the EEPROM value for DCOMP are:

$\mathrm{DCGN}[4:0] = 2.56 \times \mathrm{DischargeCompensationGain\%}$

$\mathrm{DCOFF}[2:0] = 8 \times \mathrm{DischargeCompensationOffsetC.rate.Fraction}$

DCGN is programmed in the upper 5 bits and DCOFF is programmed in the lower 3 bits of EEPROM address 0x7e.

Example: To program the capacity compensation due to discharge current to a 6.25% capacity reduction rate for current that exceeds a discharge current of C/4, DCOMP should be programmed with DCGN = 2.56 × 6.25 = 16 decimal = 10000 binary and DCOFF = 8 × 1/4 = 2 = 010 binary. Combining DCGN and DCOFF values yields a value of 10000010 binary or 0x82. With this compensation, a 1000 mAh battery with a discharge load current of 500 mA would have CAC and FCAC reduced from NAC and LMD respectively, by .0625 × (500 – 1000/4) = 15.6 mAh.

1.10 Temperature Compensation (TCOMP)

The temperature compensation (TCOMP) factor adjusts the DCGN value at cold temperatures to increase the rate at which CAC and FCAC are reduced from NAC and LMD respectively with Average Current (AI). Appendix B gives the compensation equations and discusses how to establish the compensation coefficients from battery characterization data. The EEPROM value programmed in 0x7f can alternatively be used for a customer identification or serial number if TCFIX (bit 0 in PKCFG) is set to 1. When this option is used, the default temperature compensation value of a 25% increase in the discharge compensation gain (DCGN) per °C below 12°C is used for the temperature compensation factor and the value in the TCOMP location is ignored. The default temperature compensation is equivalent to programming TCOMP with 0x46.

The EEPROM value for TCOMP is programmed in address 0x7f. The formulas for determining the EEPROM value for TCOMP are:

$$\mathrm{TCGN}[4:0] = 0.32 \times \%\mathrm{DischargeCompensationGainIncreasePerDegree}$$

$$\mathrm{TOFF}[2:0] = \frac{\mathrm{TemperatureOffsetCompensationThreshold}}{2} \tag{9}$$

TCGN is programmed in the upper 5 bits and TOFF is programmed in the lower 3 bits of EEPROM address 0x7f.

Example: To program the capacity compensation due to temperature to a 25% capacity increase in the discharge rate compensation gain for each degree temperature is below 12°C, TCOMP should be programmed with TCGN = 0.32 × 25 = 8 = 01000 binary and TOFF = 12 / 2 = 6 = 110 binary. Combining TCGN and TOFF values yields a value of 01000110 binary or 0x46. With this compensation, operation at 4°C would increase the discharge rate compensation gain by 25% × (12 – 4) = 200%.

Appendix A EDVI Compensation

The EDV1 threshold in the bq27x10 can be compensated with discharge current and temperature. The EDV1 temperature compensation factor adjusts the discharge current compensation gain, so that all EDV1 compensation is impedance-based, or proportional to current. The EDV1 threshold represents 6.25% of design capacity and battery characterization data should be examined to determine the best compensation coefficients to adjust the EDV1 threshold to maintain it at 6.25% × DC above the fixed EDVF zero capacity threshold. The compensation equations for EDV1 are simple and cannot be expected to exactly match the battery characterization data, but use of this compensation can achieve a marked improvement over use of a fixed EDV1 threshold in applications where there can be a large variation in load current and/or temperature in different operational scenarios.

The compensated EDV1 threshold (CEDV) is determined by reducing the EDV1 threshold from its initial value determined by the SEDV1 value in EEPROM by a computed threshold reduction that is directly proportional to the average discharge current. The EDV1 threshold reduction equals DEDV × 8mV when the average discharge current is equal to 1C (AI in mA equals DC in mAh). The DEDV rate compensation value is increased by a factor of EDVT/128 for each degree that temperature (T) is colder than the Toff threshold programmed in TCOMP (Toff = 2 × TOFF). No temperature compensation is applied unless T < Toff. The resulting EDV1 threshold is never allowed to be less than EDVF + 32 mV. The equation for computing CEDV is:

$$CEDV = EDV1 - DEDV \times 8\,mV \times \left(\frac{AI}{DC}\right), \text{ for } T \geq Toff \quad \text{(A-1)}$$

$$CEDV = EDV1 - DEDV \times 8\,mV \times \left(\frac{AI}{DC}\right) \times \left[1 + (Toff - T) \times \left(\frac{EDVT}{128}\right)\right], \text{ for } T < Toff \quad \text{(A-2)}$$

The CEDV threshold can be read at RAM addresses 0x21 and 0x20 if needed for evaluation purposes. The CEDV registers can contain a value less than EDVF + 32 mV at heavy load currents, but the minimum EDV1 detection threshold is limited to EDVF + 32 mV.

The optimal DEDV and EDVT compensation coefficients should be determined by evaluation of battery characterization data over the expected load and temperature operating conditions. The following discourse shows how to derive these coefficients from graphical data that can be available from the manufacturer. It is much easier to determine the coefficients more accurately from logs of actual discharge data taken over the expected load and temperature operating conditions.

SEDV1 and DEDV coefficient derivation:

Figure A-1 shows typical characterization data of discharge capacitance versus load current at 20°C operating temperature for a prismatic lithium-ion battery. If the minimum battery voltage EDVF threshold chosen is 3000mV, the nominal capacitance versus load current can be determined and is marked by letters A (1925 mAh/0.2C), B (1895 mAh/1.0C), and C (1810 mAh/2.0C). The nominal design capacity of this battery at 0.2C load is 1850 mAh. If 1850 mAh is used for design capacity, then the EDV1 threshold should occur with 1850*0.0625=115 mAh remaining. If 115 mAh is subtracted from the capacity measurements at points A, B, and C, the resulting values can be plotted on their respective curve as D, E, and F. The desired EDV1 thresholds at these load conditions can be read from the graph. This example shows the 3 desired EDV1 thresholds as D (1810 mAh/0.2C, 3560 mV), E (1780 mAh/1.0C, 3345 mV), and F (1695 mAh/2.0C, 3150 mV).

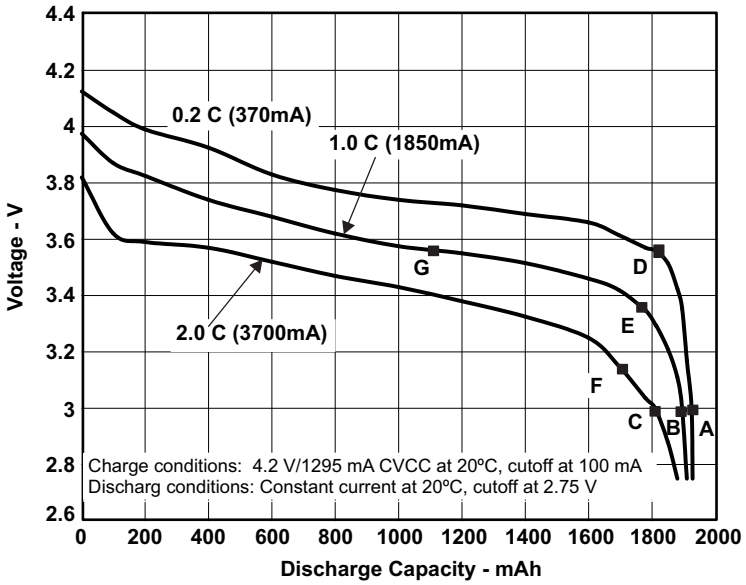

Figure A-1. Discharge Capacity Versus Load Current

The best compromise no-load EDV1 and DEDV coefficients can be determined by choosing values that compute EDV1 thresholds as close as possible to the desired values over the expected operating load conditions. Choosing a DEDV coefficient based on any 2 of the 3 points yields a different answer, but the resulting capacity error with non-optimal coefficients will likely be small. Note that if a fixed EDV1 threshold based on a 0.2C load is used (point D), the capacity error at a 1C load is significant (point G). Using points D and F, 8×DEDV = (3560 mV–3150 mV)/(2.0C-0.2C) = 228 mV/1C-rate. Using points D and E, 8×DEDV = (3560 mV-3345mV)/(1.0C–0.2C) = 268.75 mV/1C-rate. A compromise of 240 mV/1C-rate is chosen. No-load EDV1 = 3560 mV (point D) + (240 mV/1C)×0.2C = 3608 mV. The CEDV values can be back calculated to find D' = 3608 mV – 0.2C×(240 mV/1C) = 3560 mV (exact), E' = 3608 mV – 1.0C×(240 mV/1C) = 3368 mV (23 mV high), and F' = 3608 mV – 2.0C×(240 mV/1C) = 3128 mV (22 mV low).

The no-load EDV1 threshold and DEDV coefficient should be derived from battery discharge data that includes the expected minimum and maximum operating current for the system. They should be chosen to yield a best fit over the expected operating load current. A close fit outside the expected operating load range is not as important. The previous example shows choosing coefficients that fit the entire 0.2C to 2.0C load range shown in the graph. If the expected operating load range is a narrower load range, optimizing coefficients to characterization data taken over the expected load range will allow matching the measured performance even more accurately.

EDVT coefficient derivation:

Figure A-2 shows typical characterization data of discharge capacitance versus temperature at a 1C discharge current for the same prismatic lithium-ion battery. Using the same minimum battery voltage EDVF threshold of 3000 mV used in Figure A-1, the nominal capacitance versus temperature at a 1C load current is marked by letters A (1895 mAh/20°C), B (1780 mAh/0°C), and C (1650 mAh/-10°C). No temperature compensation is applied at warmer temperatures; so, the 45°C curve is not used in determining the EDVT coefficient. The same 6.25% of the 1850-mAh design capacity computed above, or 115 mAh, is subtracted from each of these points and marked at points D (1780 mAh/20°C, 3345 mV), E (1680 mAh/0°C, 3200 mV), and F (1535 mAh/-10°C, 3120 mV). Note that points A and D in Figure A-2 correspond exactly to the points B and E, respectively, in Figure A-1, because they are the same load and temperature conditions.

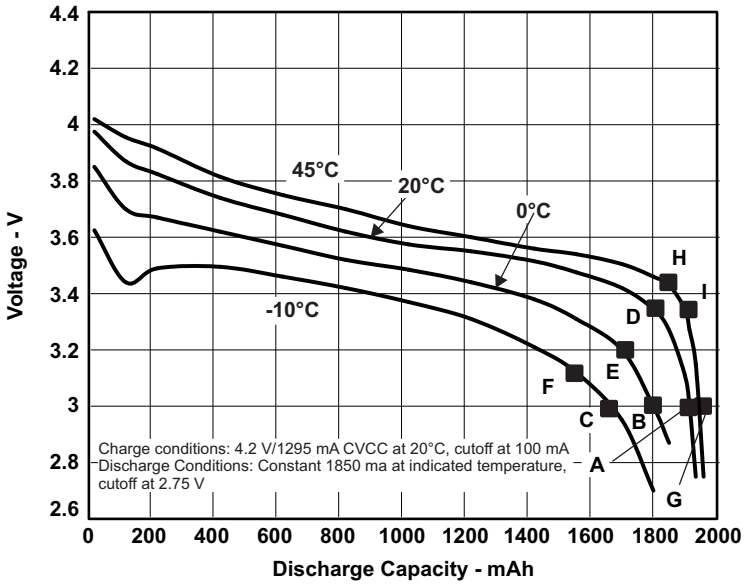

Figure A-2. Discharge Capacity Versus Temperature

The EDV1 reduction at cold temperature does not occur until the temperature falls below the Toff threshold. The Toff threshold typically is 12°C for conventional lithium-ion batteries. The Toff threshold should be evaluated for both the EDV1 compensation discussed here and the capacity compensation coefficient derivation discussed later in Appendix B. If 12°C is assumed, the following computations show how to determine the DEDV coefficient. The DEDV value derived earlier of 240 mV/1C is increased at cold temperature to cause an additional EDV1 threshold reduction. Assuming Toff = 12°C, the DEDV coefficient is increased by (12-0) × EDVT/128 at 0°C and by (12+10) × EDVT/128 at -10°C. Therefore, EDVT = (3368 mV–3200 mV) × (128/12)/240 = 7.5 at 0°C and EDVT = (3368 mV–3120 mV) × (128/22)/240 = 6.0 at –10°C would be the optimum values. The 3368-mV value is the nominal EDV1 threshold at a 1C load at 20°C when using the 240 mV/1C DEDV coefficient determined earlier. If a value of 7 is used, CEDV computes to 3368 mV – (240 mV/C) × (12-0) × (7/128) = 3368 mV–158 mV = 3210 mV at 0°C (10 mV high) and 3368 mV–(240 mV/C) × (12+10) × (7/128) = 3368 mV–289 mV = 3079 mV (41 mV low) at –10°C. If EDVT=6 is used, CEDV computes to 3233 mV at 0°C (33 mV high) and 3120 mV at –10°C (exact). If a Toff value of 10°C is used instead of 12°C, the CEDV computations with DEDV=7 result in EDV1 thresholds of 3237 mV (37 mV high) at 0°C and 3106 mV (14 mV low) at –10°C. The EDV1 compensation is not exact, but the performance is significantly improved over use of a fixed EDV1 threshold. The designer may elect to use the EDVT=6 and Toff=12°C values that compute the EDV1 threshold a little higher to ensure that the gauge does not overstate the actual remaining capacity at colder temperatures.

Because there is no increase in EDV1 threshold at warmer temperatures, the CEDV computation at 45°C with a 1C load does not approximate the desired value marked H in Figure 2, but computes the same threshold as it does at 20°C, or point I. The actual remaining capacity between points I and G is about 1940 mAh–1875 mAh = 65 mAh instead of the 115 mAh expected amount. This means that the gauge could be showing 115 mAh–65 mAh = 50 mAh when the EDVF threshold is reached at 45°C. CAC is immediately reduced to 0 when the EDVF threshold is detected. The designer may want to set the EDVF threshold high enough to allow enough residual capacity for an orderly shutdown without data loss if system shutdown is initiated by a CAC=0 or CSOC=0 report from the gauge. If the load current is reduced during shutdown, the battery voltage would increase and it could provide some additional capacity before the battery voltage drops below the system minimum operating voltage.

Appendix B Capacity Compensation

Compensated Available Capacity (CAC) and Full Compensated Available Capacity (FCAC) are the compensated capacity counterparts of Nominal Available Capacity (NAC) and Last Measured Discharge (LMD) uncompensated values, respectively. CAC and FCAC are both reduced from NAC and LMD by the same compensation capacity value. This compensation capacity value is a function of the average discharge load current, temperature, and age (cycle count). If the discharge load current decreases, the compensated capacity reduction also decreases. FCAC is allowed to increase immediately, but CAC is not allowed to increase as long as a discharge load is present. This prevents the host from seeing remaining capacity increase while there is still a discharge load applied and there is no charger connected. CAC and FCAC equal NAC and LMD while charging. If a no-load condition with open or low SCL or SDA lines allows the bq27x10 to go to sleep, CAC is allowed to increase even without charge current.

CAC and FCAC are determined by reducing the uncompensated capacity values by the discharge compensation capacity (DCMP). DCMP is determined by multiplying the discharge compensation gain factor (DCGN/256) with the average discharge current and subtracting an offset compensation value. There is no compensation if the product does not exceed the offset compensation value. Cold temperature and age increase the DCGN factor to compensate for the increased battery impedance. The formulas for computing the capacity compensation are the following:

Temperature compensation factor (TCMP):

$$TCMP = 1 + \left(\frac{TCGN}{32}\right) \times (Toff - T), \text{ for } T < Toff$$

$$TCMP = 1, \text{ for } T \geq Toff \quad \text{(B-1)}$$

Age compensation factor (ACMP):

$$ACMP = 1 + \left(\frac{TCGN}{32}\right) \times \left(\frac{CYCT}{16}\right) \times GAF \quad \text{(B-2)}$$

Compensated capacity (CAC and FCAC):

$$DCMP = AI \times \left(\frac{DCGN}{256}\right) \times ACMP \times TCMP - \left(\frac{DCOFF}{8}\right) \times DC \times \left(\frac{DCGN}{256}\right)$$

$$CAC = NAC - DCMP, FCAC = LMD - DCMP, \text{ when discharging}$$

$$CAC = NAC, FCAC = LMD, \text{ when charging} \quad \text{(B-3)}$$

The optimal DCGN, DCOFF, TCGN, and TOFF compensation coefficients should be determined by evaluation of battery characterization data over the expected load and temperature operating conditions. Battery cycle life data can be used to select the best GAF compensation coefficient.

DCOMP (DCGN and DCOFF) coefficient derivation:

The best way to determine the DCGN and DCOFF discharge compensation coefficients is to plot the actual full capacity variation of the battery over the expected operating load current at a nominal 20°C operating temperature and determine the best compensation coefficients by choosing coefficients that would generate the compensation values that are closest to the desired values. This is an easy task, because only an offset (in multiples of C/8) and slope (in multiples of 0.39%) need to be determined. As an example, the full capacity values determined by the characterization data shown in Figure A-1, marked A, B, and C, are plotted as *ACTUAL* data in Figure B-1. The *COMP-1* and *COMP-2* curves in Figure B-1 have been drawn by setting the capacity at light load equal to the nominal 20°C light-load capacity and choosing an offset and slope value that comes closest to the expected capacity values at heavier loads. The *COMP-1* curve uses DCOFF=4 (4C/8 = 0.5C offset) with DCGN=9 (9/256 = 3.5%/C-rate slope) and the *COMP-2* curve uses DCOFF=5 (5C/8 = 0.625C offset) with DCGN=11 (11/256 = 4.3%/C-rate slope). The *COMP-2* curve is much closer to all three points, but it is clear that more data between point A at 0.2C and B at 1.0C is needed. If normal operation has load

currents in the vicinity of 0.5C much more often than 2.0C and the data at 0.5C is something like the point marked D, it may be that the *COMP-1* curve is a better fit. If the load current never goes above 1.0C and D accurately represents the 0.5C data, it is clear that setting both DCOFF and DCGN lower yields a better compensation curve. In other words, take data over the exact load range of interest and choose the best compensation coefficients to achieve the best fit over that range.

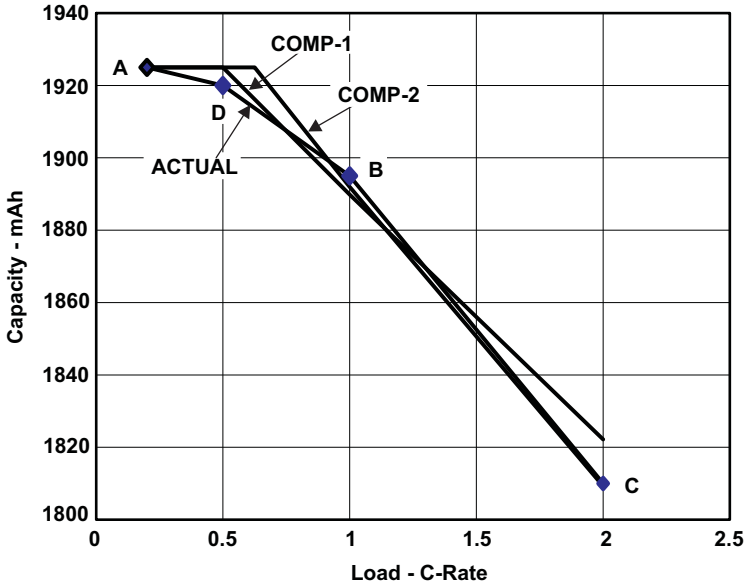

Figure B-1. Capacity Versus Load at 20°C

TCOMP (TCGN and TOFF) coefficient derivation:

The best way to determine the TCGN and TOFF temperature compensation coefficients is to plot the actual full capacity variation of the battery over the expected operating temperature range at the nominal operating load current and then determine the best compensation coefficients by choosing coefficients that would generate the compensation values that are closest to the desired values. The reduction in available capacity at cold temperature is mostly due to increased battery impedance. The computed capacity compensation is proportional to current and should track the actual capacity variation with load current in a cold temperature environment. Figure B-2 shows a plot of the battery capacity versus temperature at a constant 1C load current. This example data is taken from the characterization data shown earlier in Figure A-2. DCOFF=4 and DCGN=9 (COMP-1 curve) coefficients are assumed. The capacity values A, B, and C from Figure A-2 are plotted in Figure B-2 on the curve marked *ACTUAL*. The curve marked *COMPUTED* uses TOFF=6 (Toff = 2×6 = 12°C) and TCGN = 5 (5/32 = 15.6% increase in DCGN per degree below Toff). It is clear that additional data points at temperatures between 20°C and 0°C are desirable.

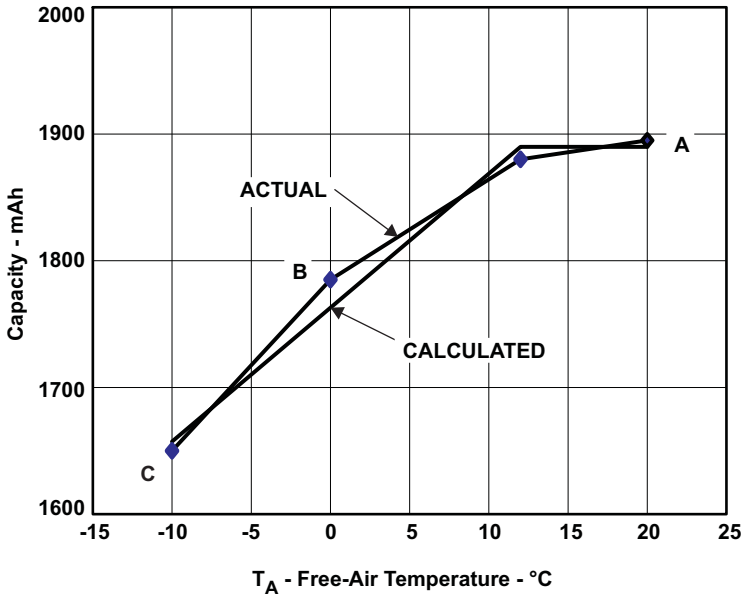

Figure B-2. Capacity Versus Temperature at 1C Load

GAF coefficient derivation:

If cycle life data is available for the battery, then the best gain age factor (GAF) can be chosen. If data is not available, GAF=1 can be used as a good estimate. However, if cold temperature characterization finds a large TCGN factor, it may be that the age compensation is too fast and without any data, the best choice may be to set GAF=0. Figure B-3 shows capacity dropping from 1925 mAh to about 1620 mAh after 500 cycles with a nominal load of 1C at 20°C. If GAF=1. Using previously determined DCOFF=4, DCGN=9, TOFF=6, and TCGN=5, the computed capacity reduction from 1925 mAh for a fresh battery is 1559 mAh after 500 cycles. This is a little faster capacity reduction than the actual data and would typically understate the capacity of an aged battery. Because this compensation, like the temperature compensation, is also impedance-based, the capacity reduction is less at lighter load currents.

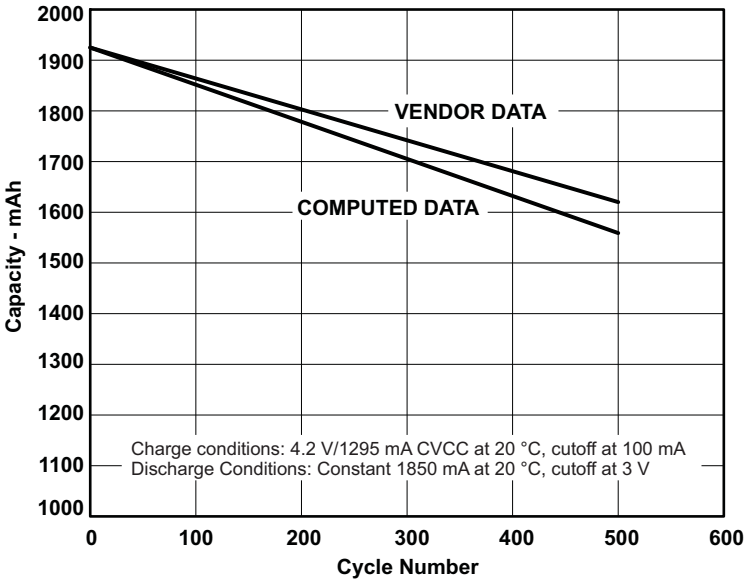

Figure B-3. Battery Capacity Versus Cycle Life

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