Optimal design for an interleaved synchronous buck converter under high-slew-rate, load-current transient conditions

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Introduction

The core voltages and currents of next-generation, high-performance microprocessors are approaching 1 V and 130 A.[1] At the same time, tight steady-state and dynamic tolerance requirements for core voltages present a big challenge for powering this type of load. To decrease the impact of PCB board and component parasitics during high-slew-rate microprocessor transients, the dedicated power supply and decoupling capacitors have to be placed as close as possible to the microprocessor.

The interleaved synchronous buck converter is a popular solution to supply high-current microprocessors because of the lower input and output current ripple and higher operating frequency of input and output capacitors in comparison with the one-channel solution.[2,3] Interleaving also enables spreading components and dissipated power over the PCB area, but it requires equal current sharing between the channels. Different control approaches to achieve good current sharing and fast transient response for interleaved microprocessor power supplies are suggested in References 2–5. Meanwhile, to determine an optimal application area for one-channel and interleaved solutions, an analysis and output filter selection procedure needs to be developed for the interleaved regulator to handle high-slew-rate, load-current transients.

The analysis and optimization procedure for the one-channel synchronous buck converter to handle high-slew-rate, load-current transients is described in References 6–8. This article extends this analysis to n-channel, interleaved synchronous buck converters. The analysis assumes that all channels are phase-shifted and that they share current equally during steady-state operation. During the load-current transient, all channels turn their FETs to the proper state simultaneously, providing the fastest transient response and recovery. This article describes procedures for minimizing cost and optimizing output filter design. A design example illustrates the analysis and compares an output filter selection of interleaved and one-channel converters for popular 12-V-input, 1.5-V, 50-A output applications.

Transient analysis for power systems with an n-channel interleaved buck converter

Model selection

The power delivery system considered in the analysis is shown in Figure 1. The model includes an n-channel, interleaved synchronous buck converter with controller, output inductors L_O...L_N, output bulk capacitor C_O with parasitics ESR and ESL, and supply path parasitics R_B and L_B. The equivalent resistor R_B characterizes resistive voltage drop through the supply paths and is the resistance of traces and connectors. The equivalent inductor L_B characterizes summarized inductive voltage drop through the traces and connectors. For the best transient response of an interleaved power supply, its control signals do not

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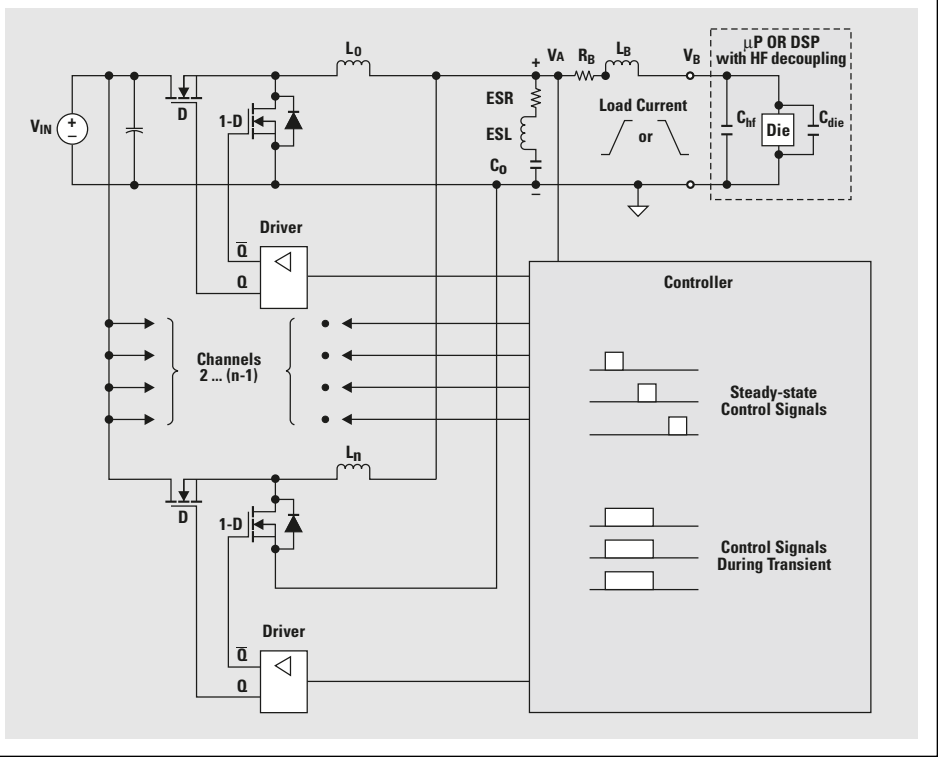
Figure 1. Model of interleaved synchronous buck converter to be analyzed



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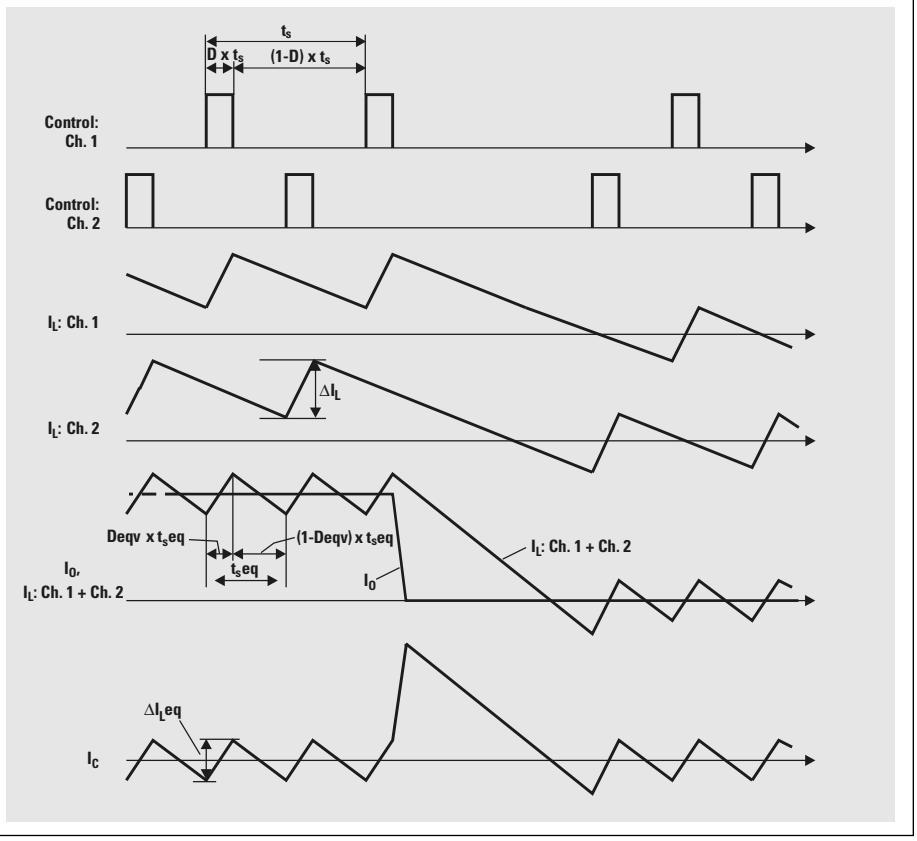
have to have delays and limitations on the duty cycle covering the range from zero to one. The controller operates in a phase-shifted manner under steady-state conditions, sharing current equally between channels. During transients, all channels simultaneously turn the high-side FETs on at load-current step-up or off at step-down, thus allowing the fastest recovery and minimum dynamic tolerance of the output voltage. When the output voltage reverts to the steady-state level, the channels revert to a phase-shifted operation with the same sequence they had before entering the transient. This "ideal" control algorithm for the best transient response is illustrated in Figures 1 and 2.

Figure 2. "Ideal" control algorithm for best transient response



Analysis approach

The analysis is based on an approach described in References 6–8 for a one-channel, synchronous buck converter; but first it is shown that any n-channel, interleaved synchronous buck converter can be considered, for analysis purposes, as some equivalent one-channel converter.

Assume that $1 - D > nD$, where n is the number of channels and $D = V_{OUT}/V_{IN}$ is a duty cycle. This condition is fulfilled for most microprocessor power supplies that have an output voltage below 2 V. For example, the popular 12-V-input and 1.6-V-output synchronous buck converter with four channels has $D = 0.13$, $1 - D = 0.87$, and $nD = 0.52$; thus $0.87 > 0.52$. This example confirms the previous assumption, meaning that for a steady-state analysis, the interleaved converter can be considered an equivalent one-channel converter operating at switching frequency nf_s and having the input voltage V_{IN}/n and output inductor L_O/n. At the same time, each channel of the interleaved converter uses output inductor L_O and operates at input voltage V_{IN}, with switching frequency f_s. The waveforms in Figure 2 illustrate this statement. It can be shown that the current through the inductors and output capacitor of an n-channel, interleaved converter has the same waveforms as an equivalent one-channel converter with the following parameters:

$$Deqv = nD,\ f_seqv = nf_s,\ t_seqv = t_s/n,\ L_Oeqv = L_O/n,$$
$$V_{IN}eqv = V_{IN}/n, \text{ and } \Delta I_Leqv = \Delta I_L(1 - nD)/(1 - D),$$

where D is the duty cycle, f_s is the switching frequency, t_s is the switching period, L_O is the output inductor, V_{IN} is the input voltage, and ΔI_L is the peak-to-peak inductor-current ripple of each channel of the interleaved buck converter. Deqv, $f_s$eqv, $t_s$eqv, $L_O$eqv, V_{IN}eqv, and ΔI_Leqv are, respectively, the duty cycle, switching frequency, switching period, output inductor, input voltage, and peak-to-peak inductor-current ripple of a one-channel, equivalent buck converter. Because all channels turn to the same state simultaneously in accordance with the proposed control algorithm, during the transients the interleaved converter can be considered to have one channel, with the input voltage V_{IN} as the original interleaved one and the output inductor L_O/n. Considering parameters of an equivalent one-channel converter helps the reader understand what advantages to expect from the interleaved converter. The interleaving gives the same effect as the one-channel converter operating at higher frequency and at lower input voltage with the lower ripple and inductor value. All this works only if a good current sharing is provided between the channels both at steady-state and dynamic conditions.

The control signals, inductor currents through each channel and summarized inductor current, along with the capacitor and load current under the load-current step-down transient conditions, are shown in Figure 2.

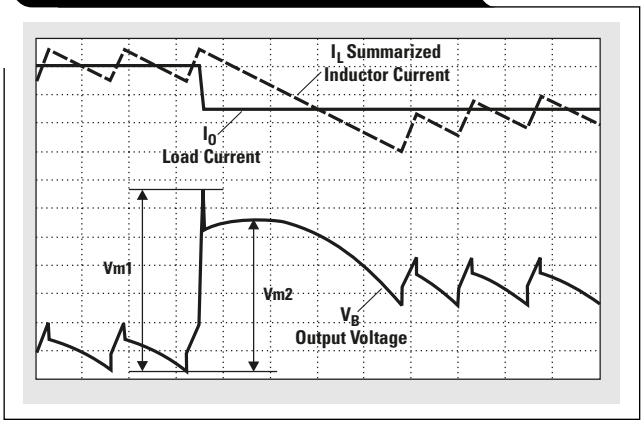
For analysis it is assumed that the output current has a linear waveform with a constant slew rate (SR) during the transient and that it changes between $I_{O(max)}$ and $I_{O(min)}$ (see Figure 2 for the current I_O). The analytical equations for the voltages and currents were derived through the main components of the equivalent one-channel model as a function of time for both the load-current step-down and step-up transients. Assuming an "ideal" control, the transient response of an interleaved converter is defined by the output filter characteristics, including the inductor-current slew rate. It is important to mention that for the step-down

transient, when all the low-side switches are turned on, the inductor current has the same slew rate as during the 1 – Deqv part of the switching cycle and equals $(V_{OUT} \times n)/L_O$. For the step-up transient, however, when all the high-side switches are turned on, the inductor-current slew rate is $[(V_{IN} - V_{OUT}) \times n]/L_O$, which is much higher than in steady-state operation during the Deqv part of the switching cycle, where the slew rate is only $(V_{IN} - V_{OUT} \times n)/L_O$.

Optimal output filter selection

Typical waveforms during the load-current step-down transient are shown in Figure 3. Usually there are two peak-to-peak values, Vm1 and Vm2. The first peak-value, Vm1, depends on ESR, R_B, ESL, and L_B (Figure 1) but not on the controller, because usually the controller's transient response is much slower than the duration of the first peak. The second peak value, Vm2, depends on ESR, R_B, L_O, C_O, and controller characteristics. References 6–8 show that the transient response depends on the position of the switching cycle when the load-current transient occurs. The worst case for the step-down transition is if the transient occurs at the end of an upper FET conduction time when the inductor current and output ripple are at their maximum. In contrast, the worst case for the step-up transition is if the transient happens at the end of the switching cycle while the inductor current and output voltage ripple are at their minimum. The same conclusion applies to the interleaved converter. The only difference is

Figure 3. Typical waveforms during load-current step-down transient



that the summarized inductor current and lower output voltage ripple need to be considered as they relate (in this analysis) to the equivalent one-channel converter. For accurate analysis, the worst condition of the transient has to be estimated.

The following equations have been derived for the number of output paralleled capacitors, N1 and N2, to meet the conditions Vm1 = ΔVreq and Vm2 = ΔVreq, respectively, as a function of switching frequency f_s, equivalent output inductor $L_O$eqv, and number of interleaved channels n:

$$N1 = \frac{\frac{ESL1}{t_O} + ESR1 + \frac{t_O}{2 \times C_O1} + \left(ESR1 + \frac{t_O}{2 \times C_O1}\right)\left(1 - \frac{t_O f_s n}{m}\right)KL}{\frac{\Delta Vreq}{\Delta I_O} - \frac{L_B}{t_O} - R_B}, \text{ and} \quad \textbf{(1)}$$

$$N2 = \frac{\frac{1}{2}\left[\frac{m}{C_O1 \times f_s \times n} - \frac{t_O}{C_O1} + \left(ESR1 + \frac{ESR1^2 \times C_O1 \times f_s \times n}{m} + \frac{m}{4 \times C_O1 \times f_s \times n}\right)KL + \frac{m}{C_O1 \times f_s \times n} \times \frac{1}{KL}\right]}{\frac{\Delta Vreq}{\Delta I_O} - R_B}, \quad \textbf{(2)}$$

where

$$KL = \Delta I_L eqv/\Delta I_O \text{ or} \quad \textbf{(3)}$$

$$KL = \frac{V_{OUT}(1 - Dn)}{L_O eqv \times \Delta I_O \times f_s \times n}. \quad \textbf{(4)}$$

Parameter m depends on the type of transient:

$$m = 1 - nD \quad \textbf{(5)}$$

for the worst-case step-down transient, and

$$m = \frac{D(1 - nD)}{n(1 - D)} \quad \textbf{(6)}$$

for the worst-case step-up transient.

The second peak-to-peak value, Vm2, exists only if the following condition is fulfilled:

$$\frac{m}{f_s \times n}\left(\frac{1}{KL} + \frac{1}{2}\right) - ESR \times C_O > t_O, \quad \textbf{(7)}$$

where t_O is load-current transition time.

If the second peak Vm2 does not exist, only the first peak Vm1 has to be considered during the selection of output capacitors. It might happen that N1 is significantly higher than N2, which means that the parasitic inductance ESL and L_B are too large for this application. In this case, the converter has to be located closer to a microprocessor, or an additional high-frequency decoupling is required. For the optimal design, the values N1 and N2 have to be almost equal.

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Design examples using different types of capacitors

To illustrate the theoretical analysis, different types of capacitors (aluminum electrolytic, OS-CON, specialty polymer, and ceramic) are compared in Table 1.

The design is satisfied for the following requirements, which are typical for a modern, high-end microprocessor: V_{IN} = 12 V, V_{OUT} = 1.5 V, $I_O(max)$ = 50 A, $I_O(min)$ = 0 A, ΔI_O = 50 A, ΔV_{req} = 100 mV, SR_{IO} = 50 A/µs, R_B = 0.4 mΩ, and L_B = 0.2 nH.

It is obvious that, for this application, the output filter design depends primarily on load-current step-down transients. This is because the inductor current has a much lower slew rate during the step-down transient than during step-up. Use of voltage positioning or droop compensation techniques only verifies this statement. Therefore, the following design example is focused on the load-current step-down transient.

The output filter selection curves have been plotted based on Equations 1 and 2 for different numbers of channels and different types of capacitors as a function of an equivalent output inductance $L_O$eqv (Figures 4-7). To obtain the actual inductance value for each channel of the interleaved converter, the equivalent inductance needs to be multiplied by the number of channels. The step in the curves for the number of capacitors N2 identifies the boundary where the peak Vm2 does not exist (Figure 3). If, for the selected type of capacitor and equivalent inductor, the number of capacitors N1 related to the peak Vm1 (Figure 3) is much greater than the number N2, parasitic ESL and L_B are significant. The additional high-frequency decoupling might help in this situation by decreasing the load-current slew rate applied to the output bulk capacitors.[8] The other solutions are layout improvement to decrease L_B or choosing the different capacitors with the lower ESL.

The number of capacitors has been obtained for the "ideal" controller, assuming that it has equal current sharing, the optimal control algorithm described earlier, and no delays. The practical implementation might require additional capacitors, but this analysis sets the target to achieve and show the relationship between the number of capacitors; the number of channels; the switching frequency; and the inductance value, including parasitics.

The curves are shown for 1-, 2-, 3-, and 4-channel interleaved converters (from top to bottom) for the aluminum electrolytic (Figure 4), OS-CON (Figure 5), specialty polymer (SP) (Figure 6), and ceramic (Figure 7) capacitors. Table 1 shows the required number of capacitors N2 and the inductance value L_O at different switching frequencies for this application. The following is a comparison summary:

1. The aluminum electrolytic and OS-CON capacitors require significant additional high-frequency decoupling at a slew rate of 50 A/µs because N1 >> N2.
2. Interleaving for aluminum electrolytic and OS-CON capacitors does not significantly decrease the number of output capacitors; only its lowering of the input filter ripple needs to be considered.
3. The 2-channel interleaving is optimal for the SP capacitors. They require much lower high-frequency decoupling at a 50-A/µs load-current slew rate.
4. The most significant effect of interleaving is that the required number of ceramic capacitors drops in inverse proportion to the number of interleaved channels. Ceramic capacitors do not require additional decoupling at a 50-A/µs load-current slew rate.

Table 1. Comparison of capacitor types

TYPE	VENDOR	PART NUMBER	f_s PER CHANNEL (kHz)	PARAMETERS OF EACH CAPACITOR			NUMBER OF CAPACITORS FOR DIFFERENT NUMBERS OF INTERLEAVED CHANNELS/L_O PER CHANNEL			
				C_O1 (µF)	ESR1 (mΩ)	ESL1 (nH)	1 CHANNEL	2 CHANNELS	3 CHANNELS	4 CHANNELS
Aluminum electrolytic	Rubycon	6.3ZA1000	200	1000	24	4.8	18/0.8 µH	16/1.6 µH	16/2.4 µH	15/3.2 µH
OS-CON	Sanyo	4SP820M	200	820	8	4.8	8/0.25 µH	7/0.5 µH	6/0.75 µH	6/1.0 µH
Specialty polymer (SP)	Panasonic	EEFCD0D101R	300	100	20	3.2	28/0.1 µH	18/0.2 µH	15/0.3 µH	13/0.4 µH
Ceramic, 1210	Murata	GRM235Y5V226Z10	400	22	20	0.5	60/0.05 µH	30/0.1 µH	20/0.15 µH	16/0.2 µH

Figure 4. Number of aluminum electrolytic capacitors as function of $L_O$eqv

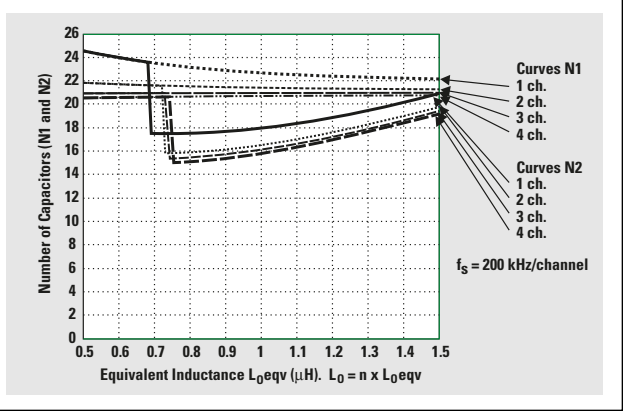


Figure 5. Number of OS-CON capacitors as function of $L_O$eqv

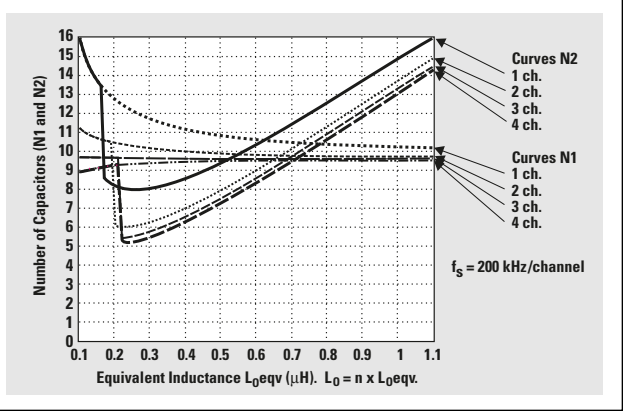


Figure 6. Number of SP capacitors as function of L_Oeqv

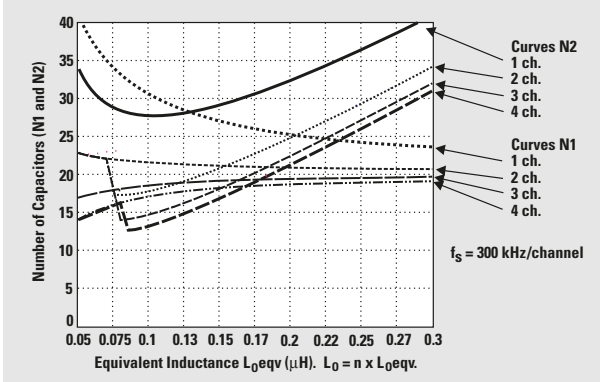
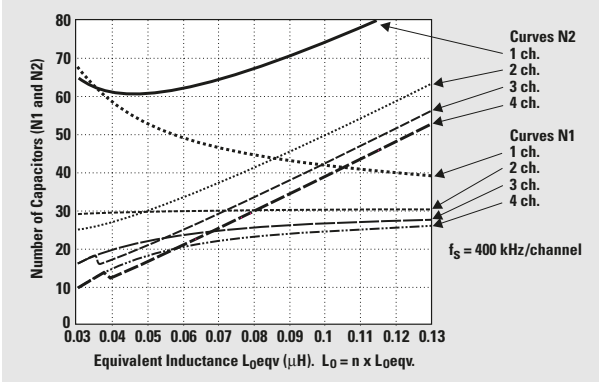


Figure 7. Number of ceramic capacitors as function of L_Oeqv

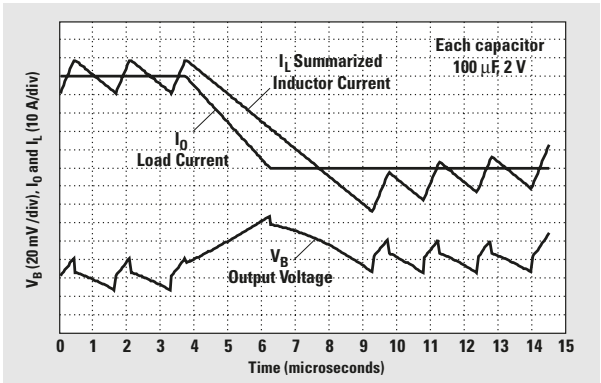


A transient example for the 2-channel interleaved buck converter based on the suggested optimization procedure is shown in Figure 8. The switching frequency of each channel is 300 kHz. Eighteen SP capacitors (100 µF) have been used in parallel in this example in accordance with Table 1. The output inductance of each channel is 0.2 µH.

Conclusion

Power-supply systems for high-slew-rate transient loads like microprocessors using an interleaved synchronous buck converter are analyzed. The selected model, based on practicality and sufficient accuracy, includes an interleaved synchronous buck converter with optimal control, output inductors L_O...L_N, output bulk capacitors, and power-supply plane parasitics. Analytical equations for the voltages and currents through components of the model were derived for any number of interleaved channels. An optimal output filter selection procedure is suggested based on the presented analysis and optimization curves for different types of capacitors and any number of interleaved channels. The design example compares aluminum electrolytic, OS-CON, SP, and ceramic capacitors for powering a 50-A microprocessor with an interleaved regulator.

Figure 8. Step-down transient for 2-channel converter with 18 SP capacitors in parallel



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