

Automating circuit designs for photodiode amplifiers

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Introduction

A wide variety of circuits use photodiodes to sense the intensity and characteristics of light. In these systems, a silicon sensor converts light into charge, which is an electrical current in the time domain. These silicon sensors are one example of “eyes” in the electronic world that can be used to analyze blood, non-invasively detect tumors, detect smoke, position equipment or perform chromatography, to name a few. The phenomenon of converting light into charge is well understood. The real challenge put before the system designer is how to convert the low-level currents from the photodiode into a useful voltage.

There are several analog front-end circuits that effectively capture the small signal level that is generated from the photodiode in these applications. The classical design topologies shown in Figure 1 are discrete solutions that use an operational amplifier (op amp) with a resistor in parallel with a capacitor in the feedback loop.^[1] These circuit designs use resistance to provide a real-time linear representation of the light source and capacitance to stabilize the output signal.

Photodiode amplifier topologies are the latest addition to the WEBENCH® Amplifier Designer suite. In a previous article in the Analog Applications Journal (AAJ), *Automating amplifier circuit design*,^[2] I provided an overview of the basic operation of the Amplifier Designer online design tool. As with the previous releases, an expert flow for automating photodiode amplifier designs calls for a combination of hard-specification requirements and judgement margins. This kind of tool uses these techniques to show the most appropriate op amps and external components that are suitable for the specifications provided.

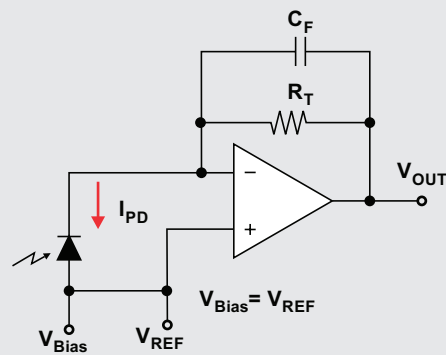
Photodiode amplifier topologies

Figure 1 shows three standard topologies for a photodiode amplifier: zero reverse bias, negative reverse bias, and positive reverse bias.

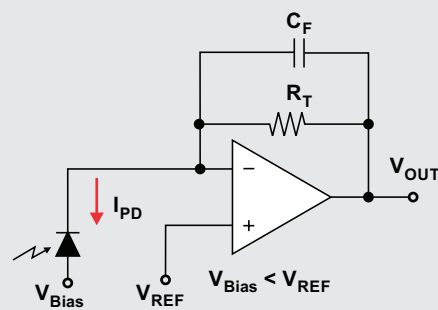
In the zero reverse-bias topology (Figure 1a), the anode of the photodiode connects to the non-inverting amplifier input (IN+) and the cathode connects to the inverting amplifier input (IN-). In this manner, there is a theoretical zero bias voltage across the photodiode because the anode voltage approximately equals the cathode voltage.

As light impinges on the photodiode, the photodiode current (I_{PD}) flows from the cathode to the anode. As the luminance becomes brighter on the photodiode, there is an increase in the photodiode current (I_{PD}). Therefore, the amplifier output (V_{OUT}) increases in voltage.

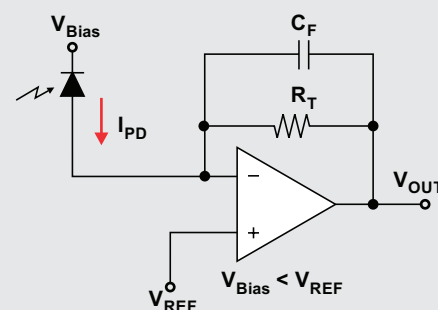
Figure 1. Photodiode amplifier topologies from WEBENCH® Amplifier Designer



(a) Zero reverse bias



(b) Negative reverse bias



(c) Positive reverse bias

In the negative reverse-bias topology (Figure 1b), the anode of the photodiode connects to the negative bias voltage (V_{BIAS}) and the cathode connects to the inverting amplifier input ($IN-$). In this manner, there is a negative voltage across the photodiode (anode-to-cathode). The application of the negative V_{BIAS} voltage causes the photodiode's junction capacitance to decrease.

As light impinges on the photodiode, the photodiode current (I_{PD}) flows from the cathode to the anode. With increased brightness on the photodiode, there is an increase in the I_{PD} current. With this occurrence, the amplifier output (V_{OUT}) increases in voltage.

In the positive reverse-bias topology (Figure 1c), the photodiode anode connects to the inverting amplifier input ($IN-$) and the cathode connects to the positive bias voltage (V_{BIAS}). In this manner, there is a positive voltage across the photodiode (cathode-to-anode).

The application of the V_{BIAS} voltage (reverse bias) causes the photodiode's junction capacitance to decrease. As light impinging on the photodiode becomes brighter, the photodiode current (I_{PD}) flows from the cathode to the anode. As the luminance increases on the photodiode, the I_{PD} current also increases. With this occurrence, the amplifier output terminal decreases in voltage.

Table 1 summarizes the operation of these three topologies, which are used in the WEBENCH Amplifier Designer.

Finding the best amplifier

The ultimate task is to find the best op amp for the photodiode amplifier circuit. This challenge requires sorting through more than 1,400 op amps. Amplifiers offered by Texas Instruments come with many variations in their electrical performance and specifications. The key specifications include power-supply ranges, bandwidth, input/output swing limits, input bias current, offset voltage and others. On top of these hard constraints, most amplifier choices use a series of overlapping issues, such as output DC error, noise, power and/or integrated circuit (IC) cost.

Step one is to find amplifiers according to basic suitability for the final design. In this step, the DC- and AC-circuit operational values are identified. Figure 2 shows an example of the initial design process for a photodiode amplifier with the WEBENCH Amplifier Designer tool.

On the Amplifier Designer requirements screen (Figure 2), data fields that must be completed are:

- Desired power supply voltages
- Desired input/output
- Design targets: peaking or bandwidth
- Small-signal specifications and peaking
- Photodiode specifications

Table 1. Summary of three transimpedance amplifier topologies

Topology	Advantage	V_{OUT} versus light
Zero reverse bias	Simplest circuit	Increases
Negative reverse bias	Reduced photodiode junction capacitance, faster response	Increases
Positive reverse bias	Reduced photodiode junction capacitance, faster response	Decreases

Figure 2. Amplifier Designer screen for data-entry activities

The screenshot displays the WEBENCH Amplifier Designer interface. It is divided into several sections:

- Power Supply:** Includes 'Desired Power Supply Voltage' with options for Dual or Single supply, and 'Desired Input/Output' with Vref/Vout and Vout Max fields.
- Design Targets:** Features 'Create Design with' options for Target Peaking or Target Bandwidth.
- Small-Signal Specifications and Peaking:** Includes 'Small Signal Specification' (TIA Bandwidth, Rise/Fall Time) and 'Peaking' (Phase Margin, Overshoot).
- Photodiode Specifications:** Contains 'Photodiode Specification' (Negative Reverse Bias), 'Specify Details' (Capacitance, Shunt Resistor, Part Number, Manufacturer), a schematic diagram of the photodiode model (Ideal Diode, Cpd, Rsh), and 'Reverse Bias Voltage (Vbias)', 'Max Photodiode Current (IpdMax)', and 'PCB Input Parasitic Cap (Cstr)' fields.
- DC Transfer Characteristic:** A graph showing Vout (V) on the y-axis (ranging from -4 to 4) versus Photodiode Output Current, Ipd (uA) on the x-axis (ranging from 0 to 50). The graph shows a linear relationship with a positive slope.

Red arrows on the left side of the interface point to 'Design Targets', 'Small-Signal Specifications and Peaking', 'Photodiode Specifications', and 'Proceed to Visualizer page'.

Initially, the power supply voltages are chosen from the list provided for the dual supply or single supply. If the dual-supply option is chosen, the pull-down menu provides seven options: ±1.5 V, ±1.65 V, ±2.5 V, ±5 V, ±6 V, ±12 V and ±15 V. If the single-supply option is chosen, the pull-down menu provides four options: +3.3 V, +5 V, +10 V and +12 V.

Design targets: constant peaking or bandwidth

Amplifier Designer uses the TIA small signal (or rise/fall time) value in conjunction with the phase margin (or overshoot) inputs to select appropriate amplifiers for your circuit. From the more than 1,400 op amps in the product line, the choices shown in Figure 3 are to keep the phase margin or overshoot as a constant (Target Peaking), or keep small-signal bandwidth or rise/fall times as a constant (Target Bandwidth).

If target peaking is chosen, the entered phase margin will remain relatively constant and the photodiode amplifier circuit bandwidth will be equal to or greater than the entered value for TIA bandwidth.

If target bandwidth is chosen, the TIA small signal bandwidth will remain close to the entered TIA bandwidth value, however, the phase margin will be equal to or greater than the entered value.

Figure 3. Select target peaking (overshoot) or target bandwidth (rise-fall time)

Create Design with Target Peaking Target Bandwidth

Small-signal specification and peaking

The menu options shown in Figures 4 and 5 allow entry of the small-signal specification and peaking requirements.

Inputs to the small signal specification boxes (Figure 4) determine the minimum signal bandwidth of the photodiode amplifier circuit.

As shown in Figure 4a, the expected TIA small-signal bandwidth may be entered. TIA stands for transimpedance amplifier, which is analogous to photodiode amplifier. The TIA small-signal bandwidth defines the first-order signal bandwidth of the photodiode amplifier.

Figure 4b shows the entry of rise/fall time as an alternative specification instead of TIA bandwidth.

If the menu is toggled between the TIA small signal bandwidth and rise/fall time, the values will follow each other according to the following equations.

$$\text{TIA small signal} = 1 / (2\pi \times R_f \times C_f) \tag{1}$$

$$\text{TIA small signal} = 0.35 / (\text{rise/fall time}) \tag{2}$$

$$(\text{rise/fall time}) = 0.35 / (\text{TIA small signal}) \tag{3}$$

Inputs to the peaking control (Figure 5) determine the photodiode amplifier circuit’s signal phase margin or overshoot.

Choosing phase margin as shown in Figure 5a specifies that the phase margin will track the overshoot percentage. The alternative is to specify overshoot as shown in Figure 5b.

The phase margin and overshoot of the transimpedance amplifier are inversely related. Phase margin (degrees) is defined at the intercept of the noise gain and the amplifier’s open-loop gain curves. As phase margin decreases, the percentage of overshoot will increase. The phase margin and overshoot values track.

Figure 4. Small-signal specifications for photodiode amplifier

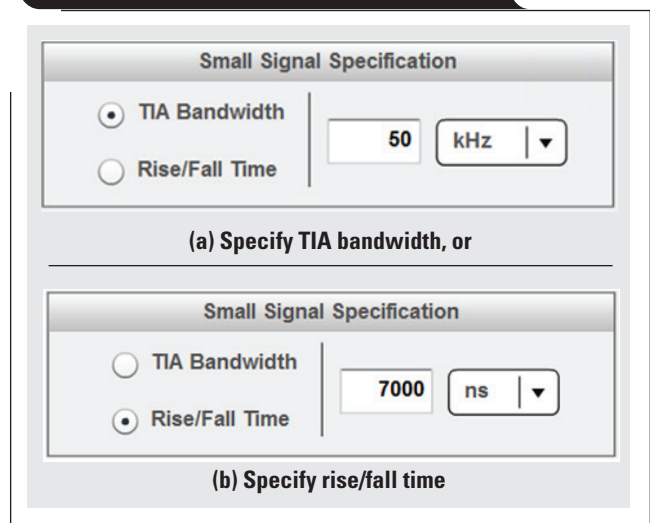
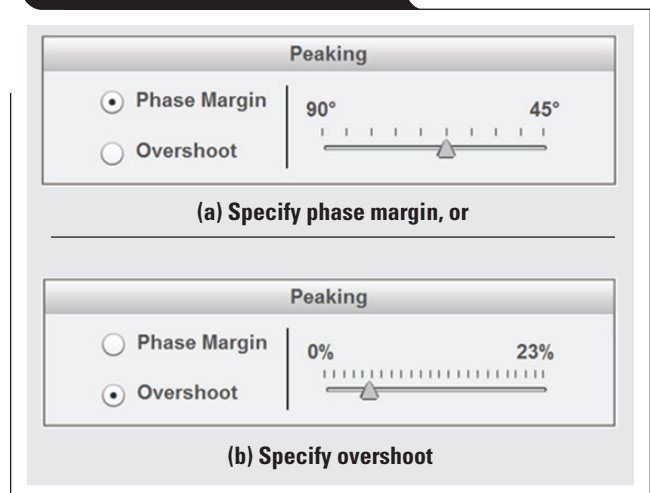


Figure 5. Peaking options for photodiode amplifier



Photodiode specifications

Figure 6 shows three menu areas for entering the photodiode specifications. The first menu option is to select the amplifier topology. The second area is for defining photodiode parasitics. The bottom area is for entering details about externally applied values that affect the photodiode.

In Figure 6, the capacitance (Cpd) and shunt resistor (Rsh) describe the photodiode parasitics.

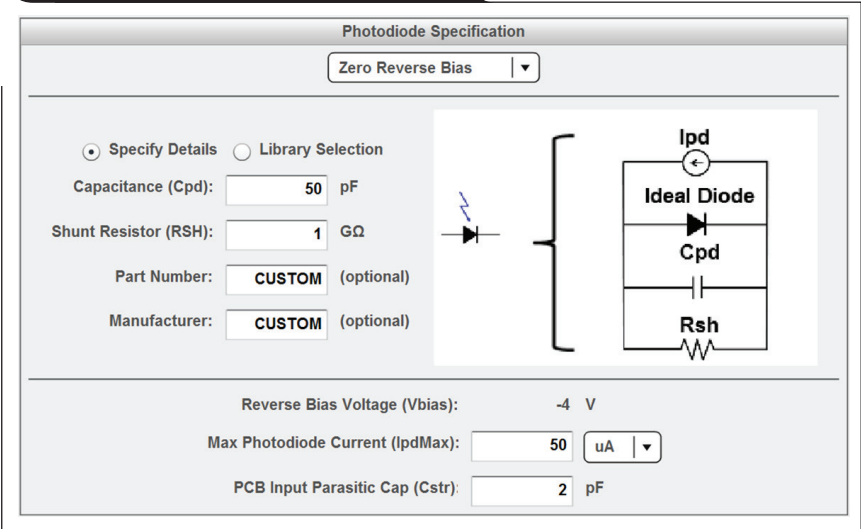
With photodiodes, there is a voltage-dependent, parasitic junction capacitance across the depletion region. Cpd represents the photodiode's n-type/p-type parasitic junction capacitance. This capacitance reduces with the applied voltage bias (Vbias) across the photodiode anode and cathode terminals as the depletion region diminishes.

Proceed to the next menu screen Create Amplifier Design by clicking the Create Amplifier Design button.

Screening op amps to target: Visualizer

During the transition from the view in Figure 2 to Figure 7, the design tool determines the R_F and C_F values. Figure 7 shows a snapshot of the Amplifier Designer Visualizer. On the top left of the screen is a list of the input design

Figure 6. Photodiode specifications



criteria. Towards the top right is the optimizer box where design priorities can be selected.

The optimizer box has three pull-down menus with the following options for design priorities: noise, output DC error, TIA bandwidth, slew rate, supply current, and cost. After selecting three design priorities, devices in the solution-table area will be resorted to match the optimizer selections.

The last menu in the top right area of Figure 7 can further refine the results to select certain amplifier

Figure 7. Amplifier Designer visualizer screen

Design Criteria
Optimizer
Refine Results

Design Criteria

Topology: Negative Reverse Bias

Dual Supply: +/-5 V

Vref/Vout: -4 V Vout Max: 4 V

TIA Bandwidth: 50 kHz Phase Margin: 65 deg

Max Photo Current: 50 uA

Edit Inputs

Schematic

Components

OpAmp IC: OPA2703UA

Photodiode: CUSTOM

Rf: 160 kΩ

Cf: 7.628 pF

Rb: 10 Ω

Cb: 10 uF

Optimizer

Very important: Noise

Important: Output DC Error

Less important: TIA Bandwidth

Refine Results

Package Group: All

No. of Channels: All

Shutdown Pin:

Solutions

Part	Create	Simulation	No. of Channels	Package	Amplifier Gain Bandwidth Product (MHz)	TIA Bandwidth (kHz)	Rise and Fall Time (uSec)	Overshoot (%)	Phase Margin (degrees)	StewRate (V/us)	Output DC Error (typ. mV)	Total Output Noise (uVrms)	Quiescent Current (mA)	Output Temperature Delta (typ. mV)	Max IC Power Supply (V)	Min IC Power Supply (V)	1k Price (USD)
OPA2703UA	Open Design		2	SOIC	1	130.39	2.684	6.197	63.09	0.6	0.16	8.522e+1	0.16	4	12	4	\$2.85
OPA2703PA	Open Design		2	DIP	1	130.39	2.684	6.197	63.09	0.5	0.16	8.522e+1	0.16	4	12	4	\$3.20
OPA2703EA/250	Open Design		2	MSOP	1	130.39	2.684	6.197	63.09	0.6	0.16	8.522e+1	0.16	4	12	4	\$2.74
OPA703PA	Open Design		1	DIP	1	130.39	2.684	6.197	63.09	0.6	0.16	8.522e+1	0.16	4	12	4	\$1.68
OPA703NA/250	Open Design		1	SOT.23	1	130.39	2.684	6.197	63.09	0.6	0.16	8.522e+1	0.16	4	12	4	\$1.68
OPA4703EA/250	Open Design		4	TSSOP	1	130.39	2.684	6.197	63.09	0.5	0.16	8.522e+1	0.16	4	12	4	\$5.20
OPA4703UA	Open Design		4	SOIC	1	130.39	2.684	6.197	63.09	0.6	0.16	8.522e+1	0.16	4	12	4	\$5.42
OPA703UA	Open Design		1	SOIC	1	130.39	2.684	6.197	63.09	0.6	0.16	8.522e+1	0.16	4	12	4	\$1.73
LMP7702MM	Open Design		2	MSOP	2.5	167.11	2.094	5.871	63.5	1	0.03	4.953e+1	0.85	1	12	2.7	\$1.84
LMP7702MM/N...	Open Design		2	VSSOP	2.5	167.11	2.094	5.871	63.5	1	0.03	4.953e+1	0.85	1	12	2.7	\$1.30
LMP7702MAN...	Open Design		2	SOIC	2.5	167.11	2.094	5.871	63.5	1	0.03	4.953e+1	0.85	1	12	2.7	\$1.56
LMP7701MF	Open Design		1	SOT.23	2.5	167.11	2.094	5.871	63.5	1	0.03	4.953e+1	0.79	1	12	2.7	\$1.40
LMP7701MAN...	Open Design		1	SOIC	2.5	167.11	2.094	5.871	63.5	1	0.03	4.953e+1	0.79	1	12	2.7	\$1.19
LMP7701MA/N...	Open Design		1	SOT	2.5	167.11	2.094	5.871	63.5	1	0.03	4.953e+1	0.79	1	12	2.7	\$0.99

Solution Table

Texas Instruments

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features. The choices available in this area are: package, number of channels, and shut down. Selections in this area will further reduce the list of amplifiers shown in the solution table area.

With the optimizer, by selecting output DC error as most important, supply current as important, and noise as less important, the solution table should show the OPA244 family of devices at the top of the list. The design summary description in the following section is based on selecting the Open Design button for the OPA244.

Open Design

Design summary

At this point, after selecting the options previously described, the circuit is fully defined. The screen for the amplifier designer summary is shown in Figure 8, which allows exploring the theoretical feasibility of the design.

The menu bar midway down in Figure 8 allows selecting detailed information screens for calculated performance analysis, performance values, and the bill of materials (BOM).

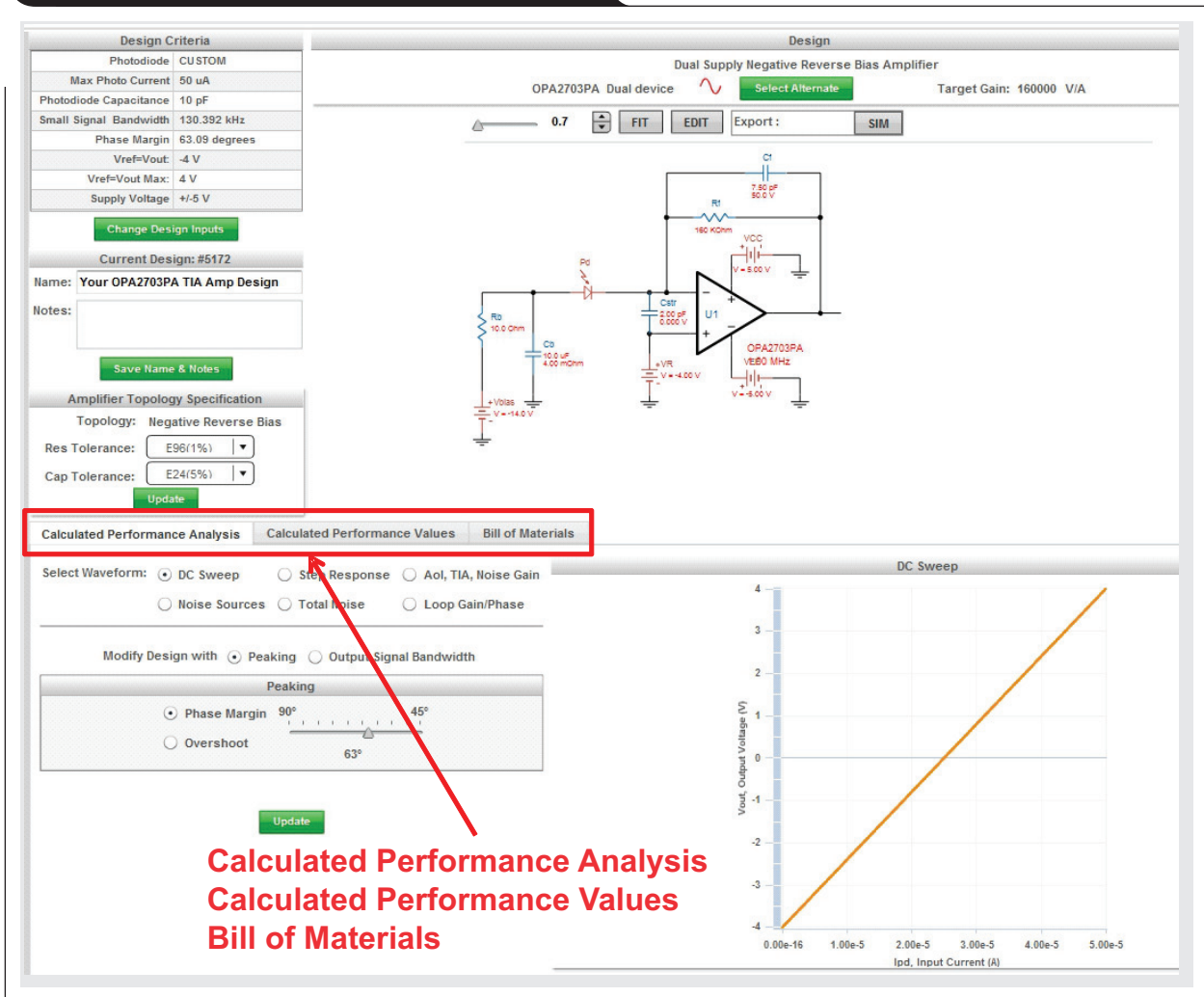
The calculated performance analysis segment produces six graphs: 1) DC sweep; 2) step response; 3) Aol, TIA, noise gains; 4) noise sources; 5) total noise; and 6) loop gain/phase. These curves are not the result of a simulation; rather, they are calculated theoretical graphs. The intent is to provide a quick look at the circuit's behavior before proceeding any further.

The calculated performance-values screen lists circuit characteristics in seven categories:

1. Design criteria
2. Operating frequency values
3. Power requirements
4. Input offset voltage/input bias current errors
5. V_{OUT} gain versus resistor/capacitor tolerance
6. Error over temperature
7. Total output noise

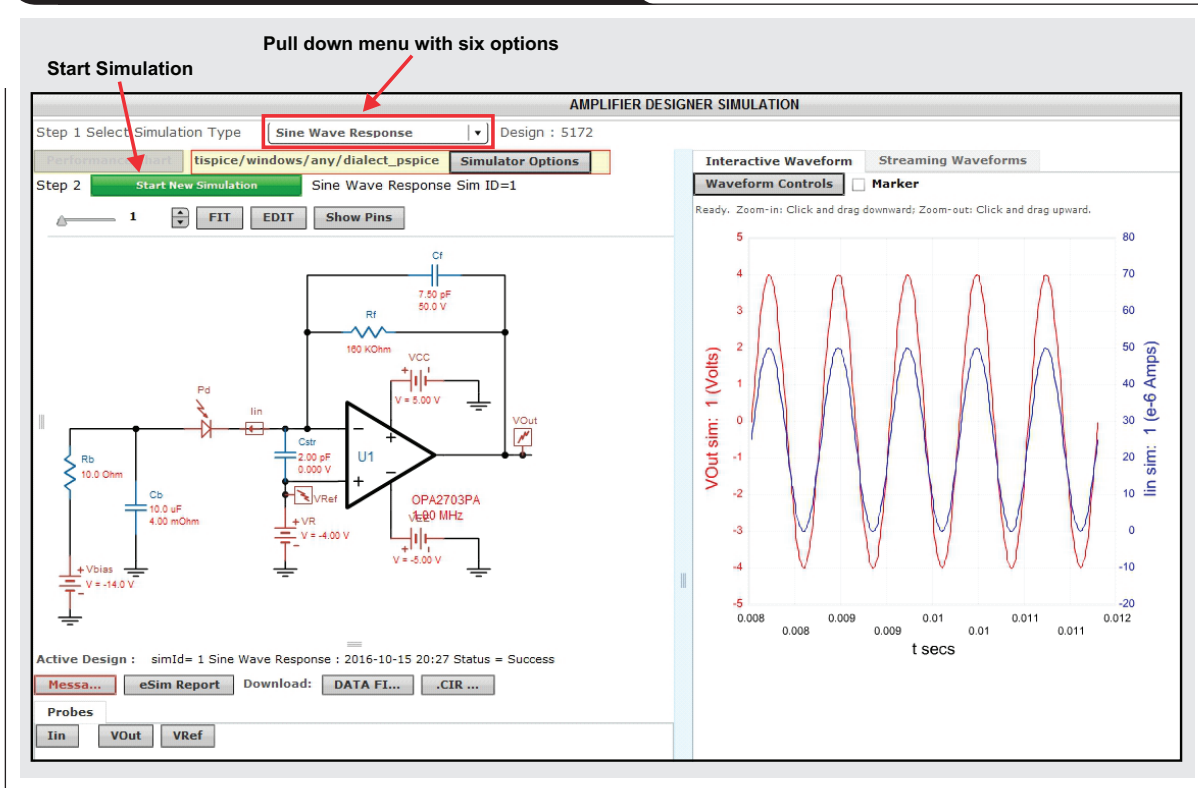
Within these seven categories, there are calculated performance values. For instance, the last category (Total Output Noise) shows the RF noise, op-amp voltage noise, op-amp current noise, total rms noise, total peak-to-peak

Figure 8. Amplifier Designer summary screen



Calculated Performance Analysis
Calculated Performance Values
Bill of Materials

Figure 9. Amplifier Designer simulation screen



noise, signal-to-noise ratio (SNR) and effective number of bits (ENOB).

For the following description, click on the SIM icon at the top of the screen to open the TI-SPICE simulation screen.



Circuit simulation with online TI-SPICE

The Amplifier Designer can export the complete circuit for TI-SPICE simulation. The amplifier simulation environment (Figure 9) uses Texas Instruments PSPICE models while providing six simulation options:

1. Sine wave response
2. Closed-loop frequency response
3. Step response
4. DC sweep
5. Output noise
6. Loop gain

With all of these simulation options, Amplifier Designer provides the appropriate signal sources. If required, it is possible to modify the magnitudes, frequency, or timing of the input sources.

For an alternative simulation environment, it is possible to download the circuit into the TINA-TI™ environment. The Amplifier Designer offers this export option by clicking the Sim Export button at the top of the screen.



Conclusion

The WEBENCH Amplifier Designer tool automatically performs the basic analysis and product selection activities that would normally be performed in photodiode circuit-design activities—but it goes a step further. It offers a comprehensive evaluation of the new circuit, making it easy to fit a design into the rest of an existing circuit. Find out more by visiting the Amplifier Designer Web site.

References

1. John Caldwell, “What op amp bandwidth do I need?” Part I, Part II and Part III. TI Precision Hub blog, May, 2014
2. Bonnie Baker, “Automating amplifier circuit design,” Analog Applications Journal (SLYT662), 1Q 2016

Related Web sites

Design tools:

WEBENCH Amplifier Designer
TINA-TI SPICE-Based Analog Simulation Program

Product Information:

OPA244

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