Application Report
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Clocking High Speed Serial Links with LMK033x8

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ABSTRACT

This application report outlines the advantages of using ultra-high performance clock generators from Texas Instruments to generate system clocks needed for high-speed serial links. A methodology for deriving reference clock jitter requirements for high-speed Ethernet link is described, and the advantages of clocking such a system with LMK03328 or LMK03318 as opposed to discrete crystal oscillators are outlined.

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1 Introduction

Any digital logic in the system requires a clock for proper operation and the clock uncertainty in high-performance systems should be as low as possible. This is to ensure that the key timing parameters like setup and hold times and propagation delay are within allowable limits. In communication systems, the clock signal regulates the speed of synchronized data transmission over the link. It is common place for these systems to carry multiple serial links that conform to different data rates and standards and each requires a pristine clock for correct operation. Tight control of phase and frequency relationship, synchronization to external frequency sources, and redundant switching might be additional system requirements.

1.1 Discrete Resonators (Crystal Oscillators)

Discrete crystal based solutions have traditionally been used in systems that carry low-speed serial links due to cost benefits and overall frequency stability. As data rates in such serial links have risen dramatically in recent years, the reference clock frequencies for such serial links have risen as well. Discrete oscillators can be used to achieve such frequencies higher than 100 MHz in a single package that contains a quartz crystal resonator oscillating at an overtone frequency along with a bandpass filter and gain circuit. However, such oscillators are expensive.

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1.2 Phase Locked Loop (Silicon-Based Clock Devices)

An alternate way of generating system clock signals is using a silicon based device comprised of a phase locked loop (PLL). A phase-locked loop (PLL) is a closed-loop frequency-control system based on the phase difference between the input clock signal and the feedback clock signal of a controlled oscillator. The PLL responds to variations in frequency and phase of the input by automatically increasing or decreasing the frequency of the controlled oscillator through feedback until the output is aligned in phase and frequency of the system. PLLs are widely used for synchronization purposes in several communication and consumer domains, radio transmitting, clock recovery and deskewing, spread spectrum, clock jitter reduction, clock generation and clock distribution.

1.3 Disadvantages of Crystal Oscillators

Crystal Oscillator based solutions have several disadvantages as listed below and as a result, a more robust hardware design tends to limit their usage. They suffer from the following:

- **Cost:** When multiple high-frequency crystal oscillators are needed, it is generally more cost effective to use a PLL device with an input crystal to generate all the system frequencies needed.
- **Jitter:** Commonly available high-frequency crystal oscillators tend to have very good close-in phase noise (at lower offset frequencies, like < 10 kHz), but often suffer from excessive jitter due to high thermal noise, which limits the broadband phase noise floor at higher offset frequencies. For communication systems, the overall jitter requirement on the system clocks is reliant on having low phase noise on both the close-in and the broadband noise floor. To solve this problem, there are specialized high-frequency oscillators that offer good phase noise at all bands but they tend to be expensive and not readily available.
- **Reliability:** Crystals have a higher failure rate than silicon based devices. Each crystal removed from the system can help increase overall system reliability. Integration also reduces component count on the board, leading to higher stability and lower product return rates.
- **Availability:** High-frequency high-performance crystal oscillators above 100 MHz are more difficult to manufacture and procure. In such a scenario, a crystal oscillator with a higher-order overtone crystal is used but is more expensive. PLL devices can use a single low-frequency, low-cost crystal (or an available clock reference) to generate several high-frequency high-performance outputs.
- **Programmability:** PLL devices have built-in programmable features that provide flexibility during design. Programmable features can include changing output clock frequencies and/or signaling formats through external control pins. Programming can also be done “on-the-fly” during system operation to tweak the device configuration by modifying its control registers, typically via an I2C serial interface. Discrete resonators only offer one frequency and have very limited flexibility.
- **Component reduction and board space savings:** PLL devices have the ability to generate several outputs from a single crystal, thereby reducing the number components used in a system and conserve board space.
- **Synchronized Outputs:** Certain serial link applications may require clock signals to be synchronized to each other. This feature is possible with PLL devices, but may not be achievable with discrete oscillators only.

2 Clocking High-Speed Serial Links With LMK033x8

TI offers a broad portfolio of Clocking ICs designed to meet the diverse needs of customers. Depending on the customer system requirements on the number of output clock signals and their quality (in terms of jitter and stability), an appropriate device from the TI clocking portfolio can be selected. LMK03328 and LMK03318 each contains ultra-high performance PLLs capable of producing very low-jitter clock outputs and are typically used to replace high-performance crystal or SAW oscillators intended for clocking high-speed asynchronous serial links. LMK03318 contains one ultra-high performance PLL and LMK03328 contains two ultra-high performance PLLs providing the flexibility to generate two independent frequency domains that are more commonly found in wired communication systems. LMK03328 and LMK03318 can also be used to generate clock outputs that are synchronized to backplane reference inputs for line cards of synchronous systems like SONET/SDH.

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2.1 Clocking Requirements for High-Speed Serial Links

Table 1 lists the integrated phase noise and jitter requirements for the reference clock in high-speed serial IO applications that are commonly addressed by fixed-frequency crystal oscillators.

Table 1. Reference Clock Requirements for Common High-Speed Serial Link Standards (Total jitter requirements for each standard is assumed to be 20% of the valid bit period)

Standard	Ref Clock Frequency (MHz)	Signal Rate (Gbps)	Max Ref Clock Jitter (% of TX Jiitter, ps, p-p)	Max Ref Clock Stability (ppm)	Offset Frequencies (MHz)	
					RX – Minimum CDR bandwidth	TX – Maximum PLL bandwidth
					(hgh-pass char)	(low-pass char)
Fibre Channel (SAN)	106.25	4.25	12.2	+/- 100	0.637	10
	132.8125	8.5	7.3			
	212.5	14.025	6.4			
Serial ATA (SATA) Serial SCSI (SAS)	75	3	16	+/- 100	1.8	7.5
	150	6	8		1.8	7.5
10Gb Ethernet	156.25	10.3125	22	+/- 100	0.001	5
	161.1328125		5.4		0.012	20
25Gb Ethernet	156.25	25.78125	4.4	+/- 100	0.001	5
	161.1328125				0.012	20
Infiniband	100	2.5	24	+/- 100	1.5	10
	200	5	12			
XAUI	156.25	3.125	22	+/- 100	1.875	20
RapidIO	156.25	3.125	32	+/- 100	1.875	20
PCI Express	100	2.5	43 (Gen 2)	+/- 300	1.5	Fref/2
	200	5	14 (Gen 3)		1	20
	400	8	7 (Gen 4)(1)		1(1)	20(1)

The overall allowable jitter in a serial link is dictated by IEEE or other relevant standards. For example, IEEE 802.3ba states that the maximum transmit jitter (peak-peak) for 10-Gbps Ethernet should be no more than 0.28 * UI. This equates to a 27.1516 ps, pp for the overall allowable transmit jitter. The jitter contributing elements are made up of the reference clock, derived potentially from a device like LMK03328, the transmit medium, transmit driver etc. Only a portion of the overall allowable transmit jitter is allocated to the reference clock, typically 20% or lower. Therefore, the allowable reference clock jitter, for a 20% clock jitter budget, is 5.43-ps, pp.

As can be seen in Figure 1, the bandwidth of TX and RX is the frequency range in which clock jitter adds without any attenuation to the jitter budget of the link. Outside of these frequencies, the SERDES link will attenuate clock jitter with a 20 dB/dec or even steeper roll-off. Modern ASIC or FPGA designs have some flexibility on deciding the optimal RX CDR bandwidth and TX PLL bandwidth. These bandwidths are typically set based on what is achievable in the ASIC or FPGA process node, without increasing design complexity, and on any jitter tolerance or wander specification that needs to be met, as related to the RX CDR bandwidth

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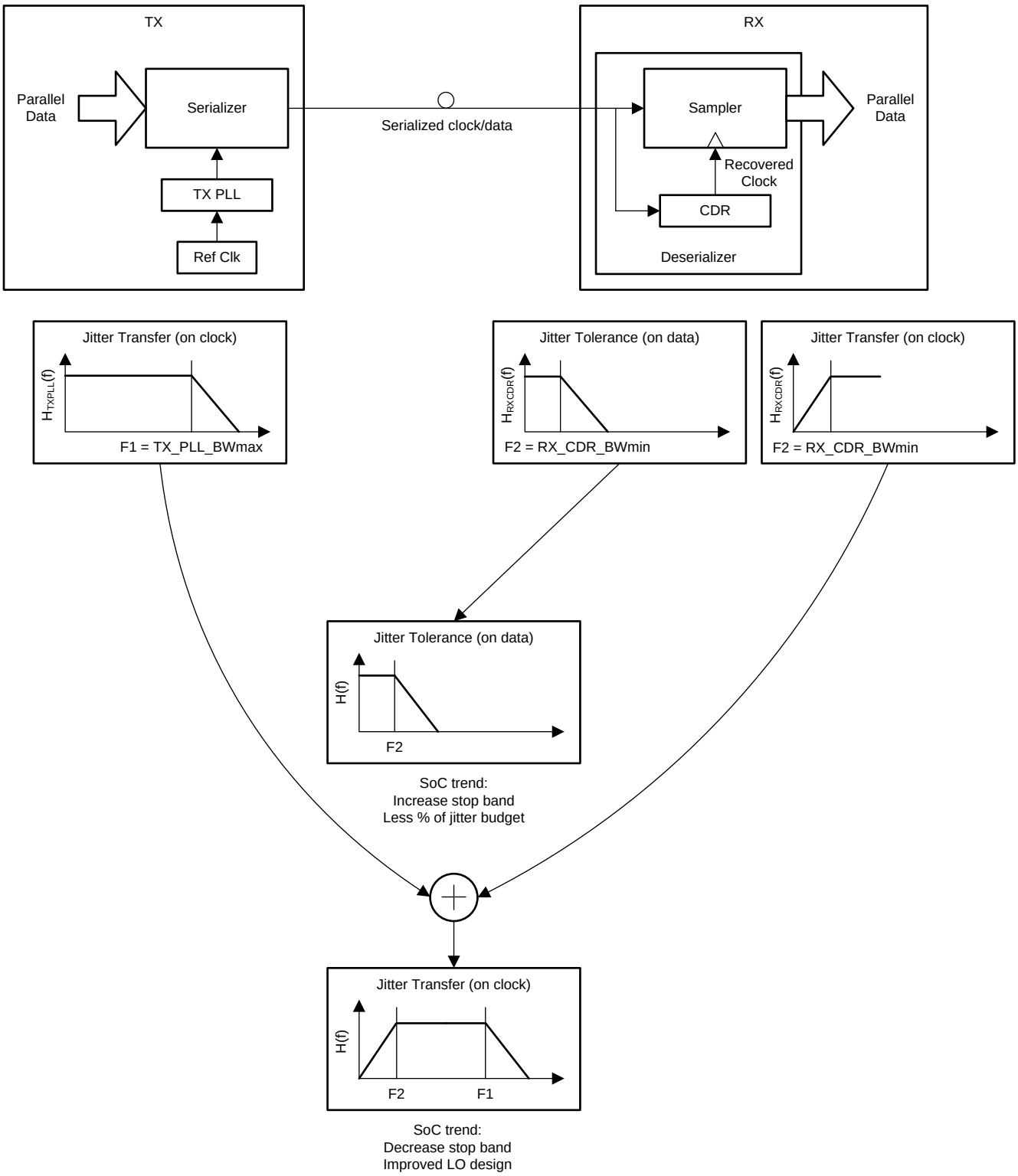

Figure 1. Dependence of Clock Jitter in Serial Links

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Jitter in a reference clock is made up of deterministic jitter (arising from spurious signals like supply noise or output crosstalk) and random jitter (arising from phase noise). A typical clock tree in a serial link system consists of clock generators and fan out buffers. The allowable reference clock jitter of 5.43 ps, pp is needed at the output of the fan out buffer. Modern fan out buffers have low additive random jitter (less than 100 fs, rms) with no substantial contribution to the deterministic jitter. Therefore, the contribution of random jitter is the collection of that from the clock generator and the fan out buffer and the contribution of deterministic jitter is solely from the clock generator. A rule of thumb, for modern clock generators, is to allocate 25% of allowable reference clock jitter to the deterministic jitter and 75% to the random jitter. This amounts to an allowable determistic jitter of 1.36 ps, pp and an allowable random jitter of 4.07 ps, pp. For serial link systems that need to meet a BER of 10^{-12}, the allowable random jitter in root-mean-square is 0.29 ps, rms. This is calculated by dividing the p-p jitter by 14 for a BER of 10^{-12}. Accounting for random jitter from the fan out buffer, the random jitter needed from the clock generator is 0.27 ps, rms. This is calculated by the root-mean-square subtraction from the desired jitter at the fan out buffer's output assuming 100 fs, rms of additive jitter from the fan out buffer.

With careful frequency planning and PLL optimization using clock design tools, such as TI's WEBENCH® Clock Architect Tool, and on-chip LDOs to suppress supply noise, LMK03328 is able to generate clock outputs with deterministic jitter <1 ps, pp and random jitter <0.2 ps, rms. This level of clock performance enables the serial link system to operate with fewer bit errors by providing more margin on the allowable transmit jitter. Figure 2 and Figure 3 show the comparison in transmit and receive eye diagrams of a 10.3125 Gbps system with a PRBS pattern when clocked at 156.25 MHz from either an LMK03328 or a high-performance crystal oscillator that is rated for a maximum random jitter of 1 ps, rms in the band of 12 kHz to 20 MHz. The data-path transmit medium is a 30 inch copper backplane with loss characteristics that are suitable for XAUI data rates. Figure 4 shows a comparison of the output clock phase noise of LMK03328 and the oscillator. Most serial link systems care about the total integrated jitter between the SerDes' CDR bandwidth and its TX PLL bandwidth and since LMK03328 shows superior jitter in the band of interest, it is able to achieve 3x improvement in BER as calculated by the number of bit errors in the link over a period of 5 minutes. The SerDes settings were kept the same (CDR bandwidth of around 1 MHz, TX PLL bandwidth of around 16 MHz) when its reference clock was provided by either LMK03328 or the oscillator.

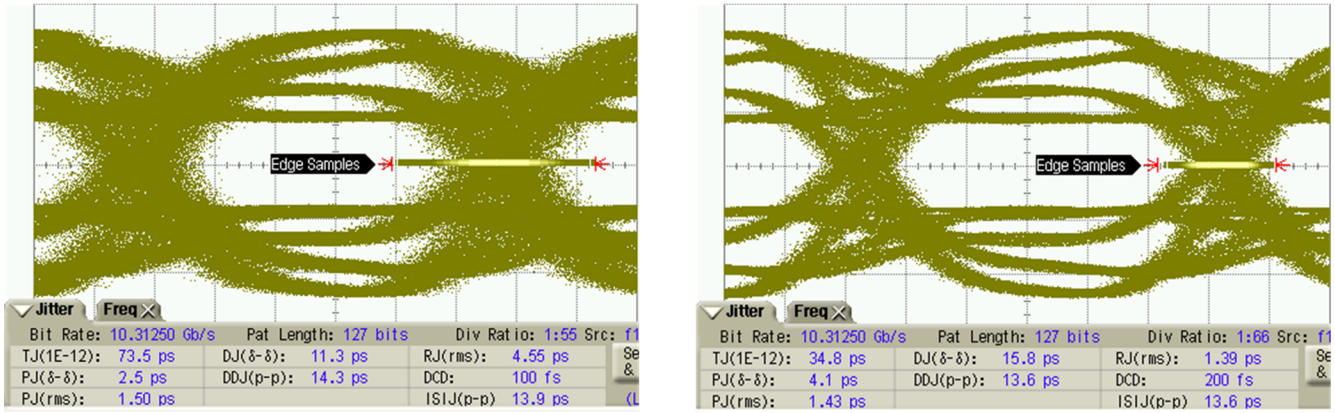

Figure 2. Transmit Eye of 10.3125-Gbps Serialized Data with Oscillator (Left) and LMK03328 (Right)

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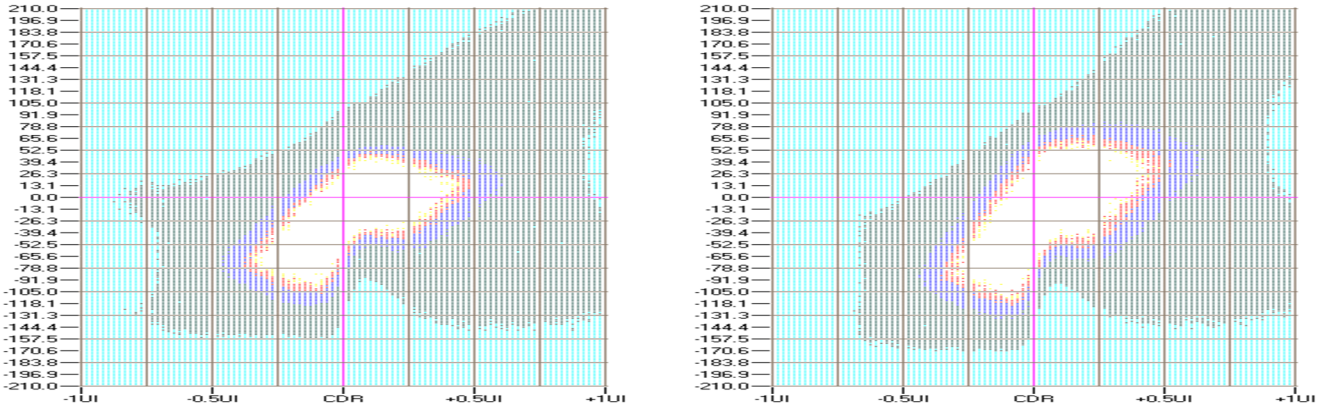

Figure 3. Receive Eye of 10.3125-Gbps Serialized Data with Oscillator (Left) and LMK03328 (Right)

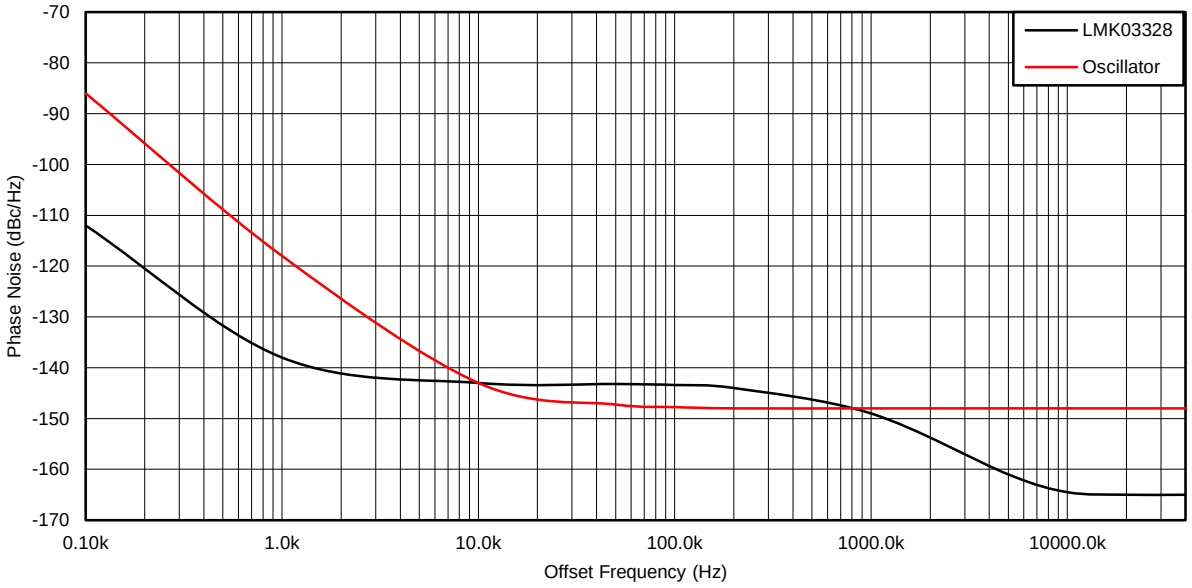

Figure 4. 156.25MHz LVPECL Phase Noise of LMK03328 (Foreground) and Oscillator (Background)

3 Summary

Ultra-high performance clock generators from TI, like LMK03328 and LMK03318, can outperform discrete crystal oscillator solutions, which suffer from various drawbacks that affect the overall performance of high-speed serial link systems as outlined in this report. The ultra-low-jitter of LMK03328 and LMK03318, combined with the plethora of features like frequency margining, simplify the overall system development, including design, prototyping and standards compliance. TI also offers WEBENCH Clock Architect Tool that helps hardware engineers to select the appropriate settings for LMK03328 and LMK03318 that meet their requirements.

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Revision History

Changes from Original (August 2015) to A Revision	Page
• Added LMK03318 throughout document	1

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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