Application Report
SNLA109A–September 2008–Revised April 2013

AN-1887 Expanding the Payload With TI's FPGA-Link DS32ELX0421 and DS32ELX0124 Serializer and Deserializer

ABSTRACT

High data payload, reaching across 10's of meters of low cost media, is stretching the current boundaries of high speed transceiver solutions. Whether the data is packetized for fiber channel at 4.25 Gbps or two streams of HD video content are multiplexed in a single link, more markets are emerging to push the limits of current high speed data solutions.

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1 Introduction

TI's family of FPGA-Link (DS32ELX0421 and DS32ELX0124) serializers and deserializers operate at serial data rates up to 3.125 Gbps. They interface to a FPGA or an ASIC over a LVDS bus containing five data bits and a clock. By combining two serializers and two deserializers the line rate is doubled to 6.25 Gbps and the payload is increased to 5 Gbps. This mode of operation is called link-aggregation. This application report offers implementation details of link-aggregation.

2 System Overview

The link segment uses two high-speed differential pairs to transmit the equivalent of 5 Gbps payload across 30 meters of low cost cable media. Figure 1 shows the basic connection diagram of link-aggregation. Link-aggregation requires a DC-balance feature where a spare data line, data[4], is used for channel delay synchronization. In this mode, data[4] is called data valid. Remote sense enables a back channel that ensures the link between the serializer and deserializer, reducing some of the FPGA/ASIC channel initialization. Remote sense is recommended if there is no active device in the serial channel.

During initialization, the data valid line to the serializer is set high. This sends IDLE characters from the serializer to the deserializer over each link. In response, the deserializer sets the data valid line high and data[3:0] is set low. When the data valid line to the serializer is pulled low, the IDLE characters stop and the deserializer sets the data valid line low. At this point, valid data is sent and received on data[3:0]. Any delay difference between the links will be seen as an offset between the data valid lines on Link A and Link B. This offset is used to compensate for the channel delays and is the key to link-aggregation.

3 Single Link Interface

We need to first understand how to setup a single serial link. Figure 2 shows the timing diagram of the FPGA/ASIC to serializer interface using DC-balance and remote sense. With remote sense on, the deserializer has a low speed back channel to the serializer that allows the serializer and deserializer to communicate and establish a link. When the serializer's lock_n signal goes low, both the serializer and deserializer are locked. At this point, the FPGA needs to hold the data valid (data[4]) line high for at least 110 clock cycles, which causes the serializer to send IDLE characters to the deserializer. Transitions of the clock and data to the serializer need to be aligned to reduce clock resources in the FPGA. There is an LVDS clock delay in the serializer that can be adjusted to ensure setup and hold times at the serializer interface. For more information on adjusting the clock delay, see Section 5.

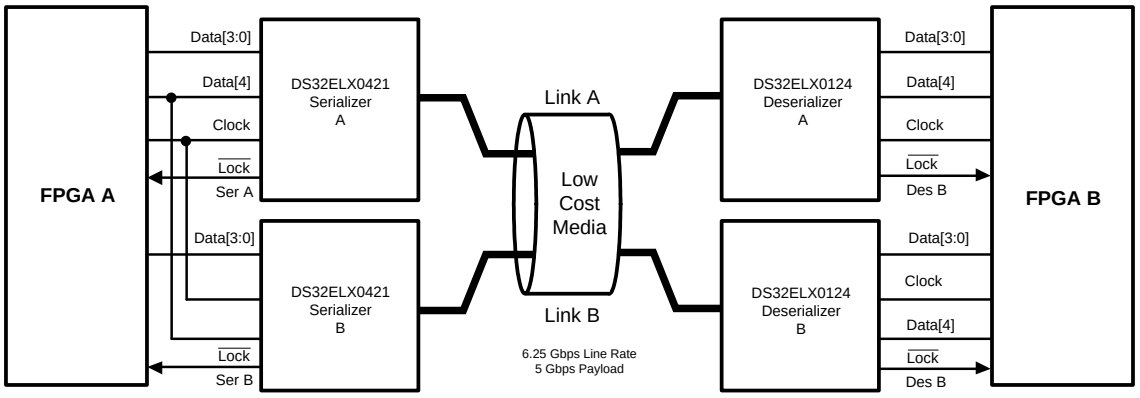

Figure 1. Link-Aggregation System Block Diagram

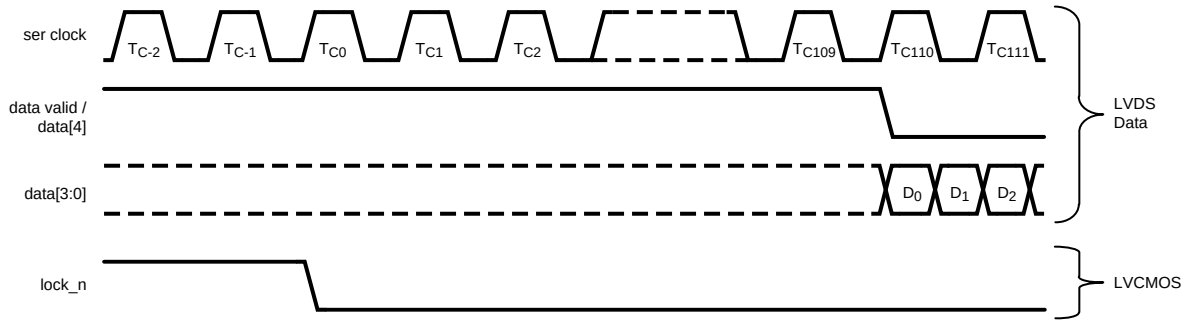

Figure 2. FPGA to Serializer Interface Single Link

Figure 3 shows the timing diagram of the deserializer to FPGA/ASIC interface using DC-balance and remote sense. On the deserializer side, the lock_n signal will go low once the serializer and deserializer establish a link. When the serializer sends IDLE characters to the deserializer the data valid (data[4]) line will go high and the data bus will go low. Once the data valid line goes low, the data bus will be aligned and valid data from the serial link will show up on the deserializer data bus. Transitions of the clock and data from the deserializer will be offset by 90°. This is close to optimum for setup and hold times in the FPGA. There is a LVDS clock delay in the deserializer that can be adjusted to ensure setup and hold times at the FPGA interface. For more information on adjusting the clock delay, see Section 5.

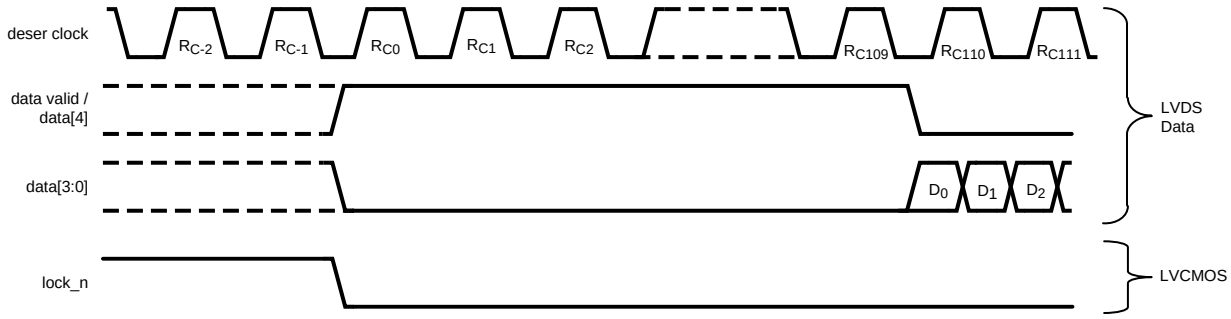

Figure 3. Deserializer to FPGA Interface Single Link

When remote sense is off, there is no back channel to ensure the link between the serializer and deserializer. In this case, the lock_n signal only means the serializer is sending serial data and the deserializer is recovering serial data. Alignment of the data has not necessarily been achieved. The startup sequence is the same as with remote sense on, except now the serializer needs to periodically send IDLE characters by setting the data valid high for 110 clock cycles. When the deserializer sees IDLE characters, the data valid line will go high and the data bus will go low. Doing this every 500 µS should give good initial data alignment and not cause excessive overhead.

4 Link-Aggregation Interface

Link-aggregation requires the use of the DC-balance encoding to align the two links of serial data. There are two keys to aggregate two links of serial data: the first is to compensate for the delay difference between each link and the second is to align the two 4-bit interfaces into a single 8-bit interface.

The startup sequence is similar to the single link interface. The FPGA/ASIC needs to drive both serializers with the same clock and data valid signal. This is shown in Figure 4.

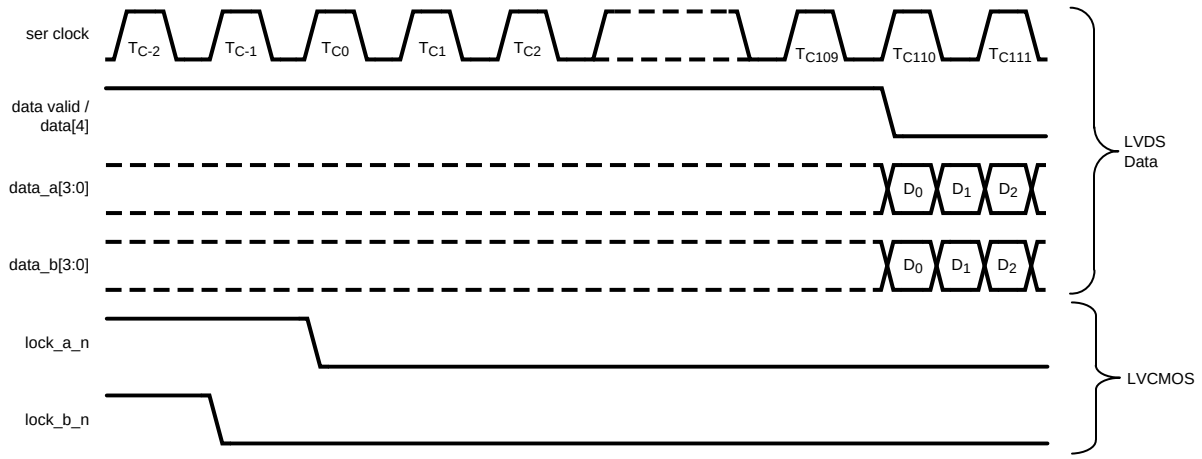

Figure 4. FPGA to Serializer Interface Two Links

After both links are acquired, the data at the deserializer outputs is frequency and phase locked but there is a delay difference due to power on reset delays and cable length mismatch. The data valid signals from the deserializers are used to determine the delay difference. Adjustable input FIFOs in the FPGA/ASIC are used to compensate for this delay difference. Each deserializer needs an input FIFO driven by its own clock to properly cross clock domains in the FPGA and compensate for the jitter differences between the two deserializers.

Figure 5 shows how the deserializer interfaces might be seen at the FPGA/ASIC. In this case, the FPGA/ASIC needs to delay the data from deserializer B by one clock cycle.

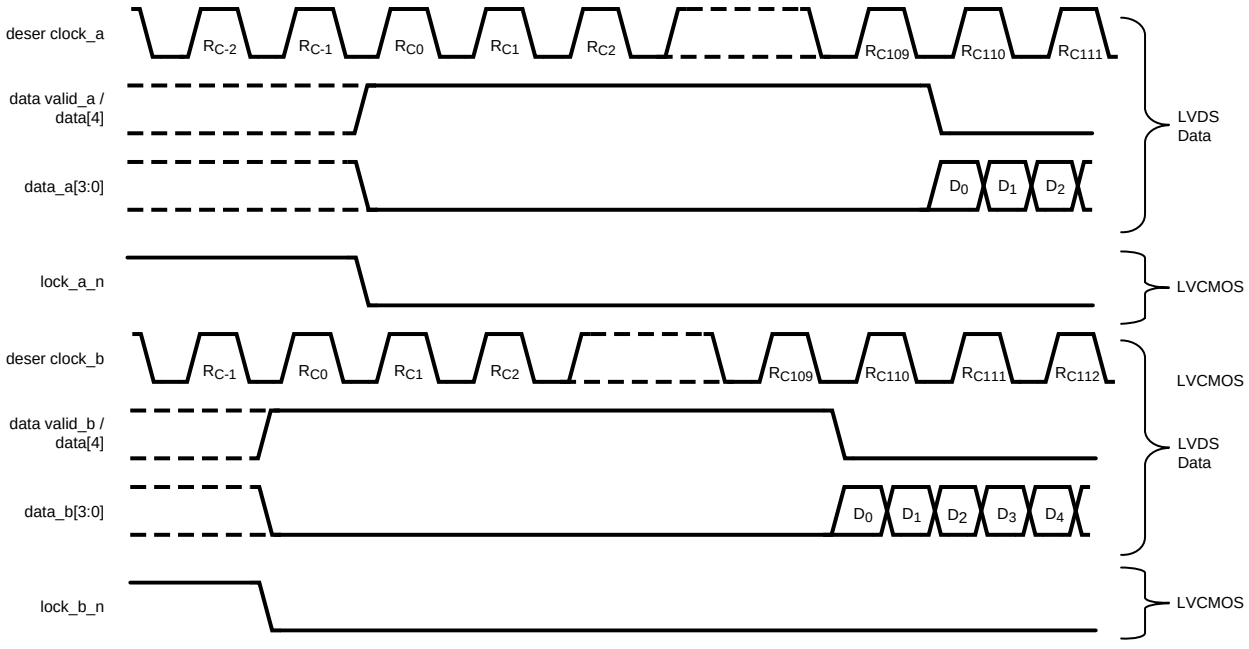

Figure 5. FPGA to Deserializer Interfaces Two Links

Alignment of the data is not required across a single deserializer data bus. This is done when the IDLE characters are received from the serializer. However, alignment needs to be done between the data bus of both deserializers. There are only two solutions at the 8-bit interface. Either data_b[3:0] is the most significant nibble and data_a[3:0] is the least significant nibble or data_a[3:0] is the most significant nibble and data_b[3:0] is the least significant nibble. This is done by comparing a known generated sequence with the received sequence and shifting the 8-bit data to match. The most common method would be to frame the data with a known header and use the header to align the 8-bit interface.

5 Register and Pin Descriptions

Both Table 1 and Table 2 list registers of interest for link-aggregation and the serializer and deserializer interface. Table 3 lists pin settings of interest for link-aggregation. More details can be found in the DS32ELX0421 and DS32ELX0124 data sheets. For link-aggregation, DC-balance must be enabled. Your can enable these by registers or by pin settings. The registers default to 0x0, which enable DC-balance and remote sense.

Table 1. Serializer Registers

Name	Address	Bit/s	R/W	Default	Description
Remote Sense	0 x 21	1	R/W	0	Remote sense active low, enables the back-channel communication between the deserializer and the serializer
DC-balance	0 x 21	0	R/W	0	DC-balance active low, enables the DC-Balance encoder
Device Configuration Override	0 x 22	0	R/W	0	0: Remote sense and DC-balance set by pins 1: Reg 0x21 bits 1:0 overrides external pins
LVDS Clock Delay	0 x 30	7:5	R/W	3	LVDS clock input delay in 125 pS increments

Table 2. Deserializer Registers

Name	Address	Bit/s	R/W	Default	Description
Remote Sense	0 x 21	1	R/W	0	Remote sense active low, enables the back-channel communication between the deserializer and the serializer
DC-balance	0 x 21	0	R/W	0	DC-balance active low, enables the DC-Balance decoder
Device Configuration Override	0 x 22	0	R/W	0	0: Remote sense and DC-balance set by pins 1: Reg 0x21 bits 1:0 overrides external pins
LVDS Clock Delay	0 x 28	3:2	R/W	2	LVDS clock output delay in 125 pS increments

Table 3. Pin Settings

Name	Pin	Description
$\overline{RS}$	6	Remote sense active low
$\overline{DC-B}$	5	DC-balance active low

6 Low Cost Media

Whether the application is Channel-Link or HDMI, the cost of the media is a significant portion of the overall system bill of materials (BOM). The DS32ELX0124 and DS32ELX0421 are designed with transmit de-emphasis and precise receive equalization targeted at Category 6 cable. Use the de-emphasis to combat cable reach up to 15 meters. At 20 meters, the deserializer needs to receive equalization to achieve link. Table 4 shows recommended media with de-emphasis and equalizer settings.

Table 4. Low Cost Media and Device Settings

Media Type	Length	Transmit De-Emphasis	Receive Equalization	Notes
Category 5	8 meters	High	None	24 awg
Category 6	20 meters	High	Setting 2	23 awg
Category 7	25 meters	High	Setting 1	24 awg
DVI	30 meters	High	Setting 2	24 awg

Crosstalk limits the performance of multi-links within a single cable. Category 6, Category 7 and DVI cables each have individually shielded pairs. The shielding limits the radiation from coupling into the different pairs, which allows the use of a single cable for multiple links.

For more information, see TI's *LVDS Owners Manual - 4th Edition* at:
http://www.ti.com/ww/en/analog/interface/lvds.shtml

7 Conclusion

Data payload can be expanded up to 5 Gbps on Texas Instruments DS32ELX0421 and DS32ELX0124 serializer and deserializer by using link-aggregation. High-speed applications, such as multiplexing two HDMI data streams, can make use of low cost media by taking advantage of the signal conditioning features and link-aggregation on Ti's serializers and deserializers.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265