

***System Design Considerations for TFT-LCD Panels Using Sample and Hold  
Based Column Drivers***



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## P-35: System Design Considerations for TFT-LCD Panels Using Sample and Hold Based Column Drivers

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### Abstract

In this paper, we outline the unique system requirements of a flat panel display that uses sample and hold based column drivers. The basic operation and system considerations of the sample and hold architecture are compared to the traditional R-DAC architecture, specifically in terms of output performance and accuracy.

### 1. Introduction

Column drivers using a sample and hold based architecture have advantages for both IC manufacturers as well as TFT-LCD panel manufacturers when compared to the traditional resistor DAC (R-DAC) based column drivers. For the IC manufacturer, the sample and hold architecture allows for smaller die size due to the elimination of many space consuming R-DAC cells. This allows for lower cost, higher yield rates, and larger column driver capacity at the wafer level. For the TFT-LCD panel manufacturer, the sample and hold architecture allows true 8-bit panels to be built at similar cost and power consumption to the dithered 8-bit panels. The smaller die size also allows for advanced packaging technologies such as Chip-On-Glass without expanding the bezel size of the overall panel.

Because the sample and hold architecture samples output voltages throughout the line time and not just at the end of the line, there are several system design considerations that need to be taken into account when designing with sample and hold based column drivers. This paper will outline the important operation characteristics of the traditional R-DAC and sample and hold architectures and the different system requirements.

### 2. Traditional R-DAC Architecture

The traditional R-DAC architecture uses one R-DAC per output to convert the digital data into analog voltage levels. Digital data is loaded and stored in data latches until the conversion takes place. Because each output has an independent DAC, the data conversion only needs to occur once per line, typically at the end of the line.

Figure 1 shows the typical R-DAC architecture. RSDS™ data is loaded into the column driver and is stored in the data latches based on the control inputs. The D to A Converters simultaneously convert all outputs of data from their digital level to their analog level based on the voltages applied across the internal resistor string.

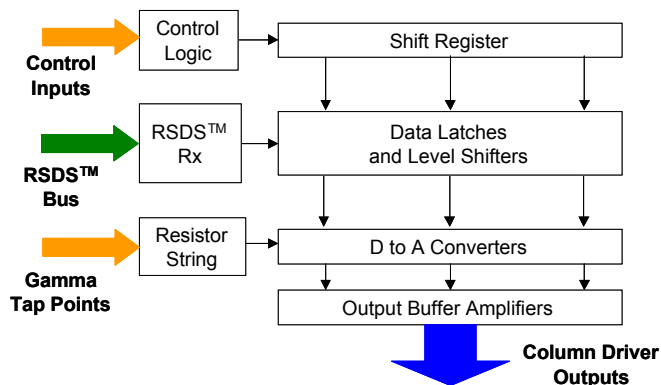


Figure 1. Traditional R-DAC Column Driver Architecture

Figure 2 shows the location of the data latch and conversion in the R-DAC architecture. Because there is a DAC dedicated to each output, the data latching and conversion only needs to occur once per line.

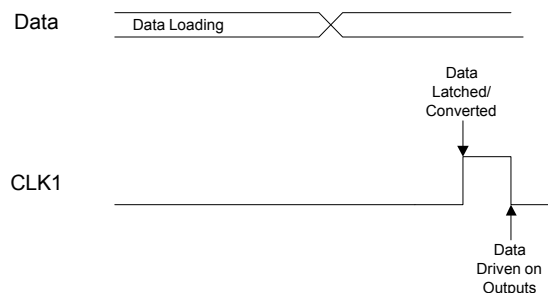
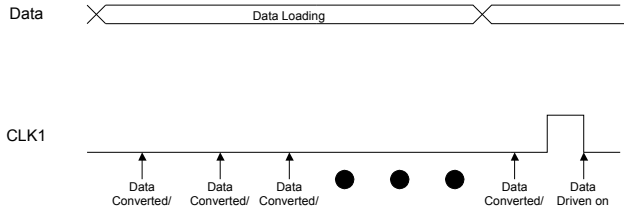


Figure 2. Data Conversion and Output Driving in an R-DAC Architecture

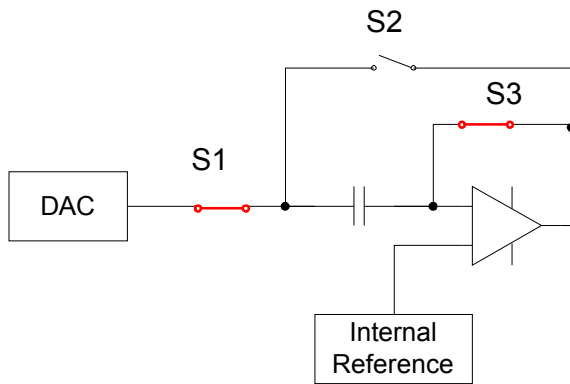
### 3. Sample and Hold Architecture

The sample and hold architecture uses shared DACs for the outputs. Data is latched and converted many times throughout the line. Each time data is latched and converted, the resulting output voltage is sampled onto a capacitor until it is time for the outputs to drive to the new level. For example, a sample and hold column driver with 384 outputs and 12 shared DACs will need to convert and sample voltages 32 times every line. This is shown in Figure 3.

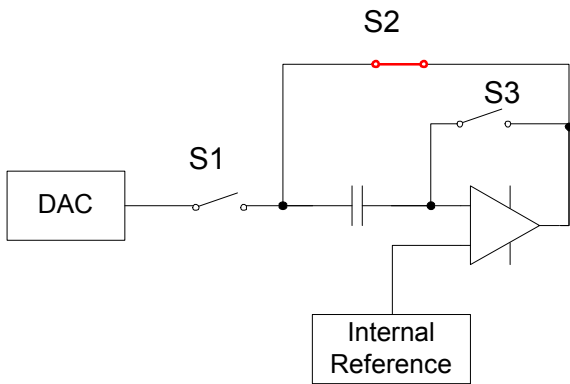


**Figure 3. Sample and Hold Data Conversion and Sampling**

The sample and hold circuitry operates in two stages, the sampling stage and the driving stage. As shown in Figure 4, during the sampling stage switches S1 and S3 are closed, allowing the DAC voltage to charge up the capacitor. The voltage developed across the capacitor is equal to the gamma voltage minus the internal reference voltage. The voltage is then held on the capacitor until the outputs need to start driving. As shown in Figure 5, during the driving phase, switch S2 is closed and the output drives the sampled voltage.



**Figure 4. Sample and Hold Sampling**



**Figure 5. Sample and Hold Driving**

#### 4. System Considerations for Sample and Hold Architectures

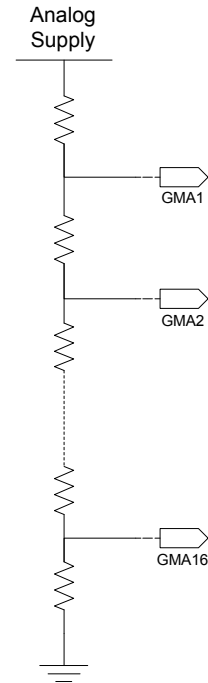
Because the R-DAC architecture only samples the output voltage once per line, it is critical that the gamma input voltages be accurate and stable at that point. For the rest of the line, the stability and accuracy of the gamma voltages are not as critical.

For a Sample and Hold architecture, it is critical that the difference between the gamma voltage and the internal reference voltage (which is developed from the analog supply) needs to be consistent across the entire line time. Note that this does not necessarily mean that both voltages need to be independently stable across the line, but the delta between them must be stable.

#### 4.1 Generating Gamma Voltages

Because the internal reference voltages are developed from the analog supply, in order to maintain good correlation between the gamma voltages and the references, the gamma voltages should be developed from the analog supply. The analog supply will droop (20-80mV typically) when the outputs begin to drive. If the gamma references are developed from a separate reference that is stable relative to the analog supply, then there will be a difference between the gamma voltages and the internal reference.

A second important consideration is the driving of the gamma voltages. In many systems it is common to use external operational amplifiers to drive at least some of the gamma voltages. This provides additional stability and precision to the gamma voltages. In the Sample and Hold architecture, these op amps can artificially stabilize the gamma references in relation to the analog supply. The recommended method for generating the gamma voltages is to use a simple resistor divider as shown in Figure 6.



**Figure 6. Recommended Gamma Voltage Generation**

The error in the sampled voltage can be estimated. The internal reference is  $\frac{3}{4}$  of the analog supply for the voltages in the upper range and  $\frac{1}{4}$  of the analog supply for voltages in the lower range. If the analog supply droops X mV, then the internal references will droop  $\frac{3}{4}$  X and  $\frac{1}{4}$  X mV. The gamma voltage will droop a fraction of the overall droop based on its relationship to the analog rail (i.e. if the target gamma voltage is 82% of the analog rail, the droop on that voltage will be 82% X mV). The output voltage

error can be reduced to zero near the center of the gamma curve (when the target gamma voltages are  $\frac{3}{4}$  and  $\frac{1}{4}$  of the analog rail) and will be a worst case 25% of the droop at the ends of the gamma curve. Having a higher output error at the ends of the gamma curve is normally acceptable because adjacent gray levels can be 100mV or more apart. At the center of the curve, where the output error approaches zero, the gray levels are sometimes separated by 30mV or less.

## 4.2 Gamma and Power Supply Decoupling

In addition to using the most efficient circuitry to generate the gamma reference voltages, the overall decoupling scheme needs to be considered. For the analog supply, large decoupling capacitors (10-22 $\mu$ F) can be used at the output of the DC-DC converter for energy storage. At the input to the column driver, 0.1-0.47 $\mu$ F capacitors are recommended. On the gamma reference voltages, only small decoupling capacitors (0.1 $\mu$ F or less) should be used. These capacitor values will typically provide good high frequency decoupling without stabilizing either the analog supply or the gamma reference voltages independent of the other.

The ideal scenario is to generate a perfect analog supply, but experimental results have shown that the instantaneous current draw of the column drivers when the outputs begin driving is so large that it would take several hundred  $\mu$ F in order to completely stabilize the supply. The best alternative is to provide some

energy storage on the analog supply, but to try and match the decoupling of the gamma references and analog supply.

## 5. Conclusions

The idea of column drivers that use a sample and hold architecture is not new. The practical implementation has been somewhat elusive. We have demonstrated that a sample and hold column driver can have very good output performance if the differences between the sample and hold and the traditional R-DAC are understood and accounted for.

In our experience, the system changes needed to improve the performance of a sample and hold column driver not only improve the column driver performance, but they also tend to reduce the total number of components in the system and can reduce the overall system power. The success of the sample and hold architecture will lead to more cost effective true 8-bit column drivers and higher performance displays for all large scale applications.

## 6. Acknowledgements

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