# TPA6211A1-Q1 3.1W Mono Fully Differential Audio Power Amplifier

## 1 Features

- Qualified for automotive applications
  - Temperature Grade 2: –40°C to 105°C $T_A$
  - Device HBM ESD classification level 2
  - Device CDM ESD classification level C6
- 3.1W into 3Ω from a 5V supply at THD = 10% (typical)
- Low supply current: 4mA (typical) at 5V
- Shutdown current: 0.01µA (typical)
- Fast startup with minimal pop
- Only three external components
  - Improved PSRR (–80dB) and wide supply voltage (2.5V to 5.5V) for direct battery operation
  - Fully differential design reduces RF rectification
  - –63dB CMRR Eliminates two input coupling capacitors

## 2 Applications

- Automotive audio
- Emergency calls
- Driver notifications
- Cluster chimes

## 3 Description

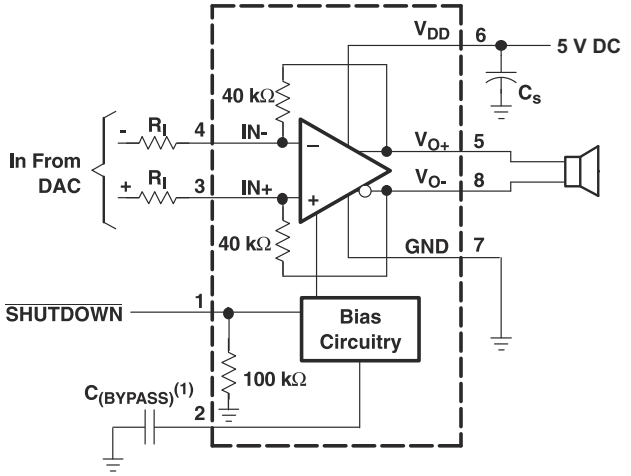
The TPA6211A1-Q1 device is a 3.1W mono fully-differential amplifier designed to drive a speaker with at least 3Ω impedance while consuming only 20mm$^2$ total printed-circuit board (PCB) area in most applications. The device operates from 2.5V to 5.5V, drawing only 4mA of quiescent supply current. The TPA6211A1-Q1 device is available in the space-saving 8-pin HVSSOP package.

The device includes features such as a –80dB supply voltage rejection from 20Hz to 2kHz, improved RF-rectification immunity, small PCB area, and a fast start-up with minimal pop makes the TPA6211A1-Q1 device an excellent choice for emergency call applications. Additionally, the device supports low-power needs in infotainment and cluster applications, such as cluster chimes or driver notification.

**Device Information**

| PART NUMBER | PACKAGE(1) | PACKAGE SIZE(2) | BODY SIZE (NOM) |
|---|---|---|---|
| TPA6211A1-Q1 | HVSSOP (8) | 3.00mm × 4.90mm | 3.00mm × 3.00mm |

(1) For more information, see Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.




A. $C_{(BYPASS)}$ is optional

**Application Circuit**

# Table of Contents

# 4 Pin Configuration and Functions

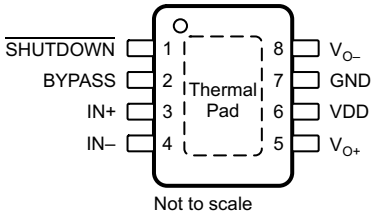



**Figure 4-1. DGN Package 8-Pin HVSSOP Top View**

## Pin Functions

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| BYPASS | 2 | I | Mid-supply voltage, adding a bypass capacitor improves PSRR |
| GND | 7 | I | High-current ground |
| IN– | 4 | I | Negative differential input |
| IN+ | 3 | I | Positive differential input |
| $\overline{\text{SHUTDOWN}}$ | 1 | I | Shutdown pin (active low logic) |
| Thermal Pad | — | — | Connect to ground. Thermal pad must be soldered down in all applications to properly secure device on the PCB. |
| $V_{DD}$ | 6 | I | Power supply |
| $V_{O+}$ | 5 | O | Positive BTL output |
| $V_{O-}$ | 8 | O | Negative BTL output |

## 4.1 DAPPER

| NAME | NO. | TYPE | DESCRIPTION |
|---|---|---|---|
| BYPASS | 2 | I | Mid-supply voltage, adding a bypass capacitor improves PSRR |
| GND | 7 | I | High-current ground |
| IN– | 4 | I | Negative differential input |
| IN+ | 3 | I | Positive differential input |
| $\overline{\text{SHUTDOWN}}$ | 1 | I | Shutdown pin (active low logic) |
| $V_{DD}$ | 6 | I | Power supply |
| $V_{O+}$ | 5 | O | Positive BTL output |
| $V_{O-}$ | 8 | O | Negative BTL output |
| Thermal Pad | — | — | Connect to ground. Thermal pad must be soldered down in all applications to properly secure device on the PCB. |

# 5 Specifications

## 5.1 Absolute Maximum Ratings

over operating free-air temperature range unless otherwise noted(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage, $V_{DD}$ | | –0.3 | 6 | V |
| Input voltage, $V_I$ | | –0.3 | $V_{DD}$ + 0.3 V | V |
| Continuous total power dissipation | | See *Section 5.7* | | |
| Lead temperature 1.6 mm (1/16 Inch) from case for 10 s | DGN | | 260 | °C |
| Operating free-air temperature, $T_A$ | | –40 | 105 | °C |
| Junction temperature, $T_J$ | | –40 | 150 | °C |
| Storage temperature, $T_{stg}$ | | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Section 5.3*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 5.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per AEC Q100-002(1) | ±2000 | V |
| | | Charged-device model (CDM), per AEC Q100-011 | ±1000 | |

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

## 5.3 Recommended Operating Conditions

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | | 2.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | $\overline{SHUTDOWN}$ | 1.55 | | V |
| $V_{IL}$ | Low-level input voltage | $\overline{SHUTDOWN}$ | | 0.5 | V |
| $T_A$ | Operating free-air temperature | | –40 | 105 | °C |

## 5.4 Thermal Information

| THERMAL METRIC(1) | | TPA6211A1-Q1 DGN (HVSSOP) 8 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 71.7 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 55.9 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 44.9 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 3.7 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 44.7 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 19.6 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 5.5 Electrical Characteristics

$T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{OS}$ | Output offset voltage (measured differentially) | $V_I$ = 0-V differential, Gain = 1 V/V, $V_{DD}$ = 5.5 V | –9 | 0.3 | 9 | mV |
| PSRR | Power supply rejection ratio | $V_{DD}$ = 2.5 V to 5.5 V | | –85 | –60 | dB |
| $V_{IC}$ | Common mode input range | $V_{DD}$ = 2.5 V to 5.5 V | 0.5 | | $V_{DD}$ – 0.8 | V |

$T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| CMRR | Common mode rejection ratio | $V_{DD}$ = 5.5 V, $V_{IC}$ = 0.5 V to 4.7 V | | | –63 | –40 | dB |
| | | $V_{DD}$ = 2.5 V, $V_{IC}$ = 0.5 V to 1.7 V | | | –63 | –40 | |
| | Low-output swing | $R_L$ = 4 Ω, $V_{IN+}$ = $V_{DD}$, $V_{IN+}$ = 0 V, Gain = 1 V/V, $V_{IN–}$ = 0 V or $V_{IN–}$ = $V_{DD}$ | $V_{DD}$ = 5.5 V | | 0.45 | | V |
| | | | $V_{DD}$ = 3.6 V | | 0.37 | | |
| | | | $V_{DD}$ = 2.5 V | | 0.26 | 0.4 | |
| | High-output swing | $R_L$ = 4 Ω, $V_{IN+}$ = $V_{DD}$, $V_{IN–}$ = $V_{DD}$, Gain = 1 V/V, $V_{IN–}$ = 0 V or $V_{IN+}$ = 0 V | $V_{DD}$ = 5.5 V | | 4.95 | | V |
| | | | $V_{DD}$ = 3.6 V | | 3.18 | | |
| | | | $V_{DD}$ = 2.5 V | 2 | 2.13 | | |
| $\lvert I_{IH} \rvert$ | High-level input current, shutdown | $V_{DD}$ = 5.5 V, $V_I$ = 5.8 V | | | 58 | 100 | µA |
| $\lvert I_{IL} \rvert$ | Low-level input current, shutdown | $V_{DD}$ = 5.5 V, $V_I$ = –0.3 V | | | 3 | 100 | µA |
| $I_Q$ | Quiescent current | $V_{DD}$ = 2.5 V to 5.5 V, no load | | | 4 | 5 | mA |
| $I_{(SD)}$ | Supply current | $V_{\overline{SHUTDOWN}}$ ≤ 0.5 V, $V_{DD}$ = 2.5 V to 5.5 V, $R_L$ = 4 Ω | | | 0.01 | 1 | µA |
| | Gain | $R_L$ = 4 Ω | | $\frac{38\ k\Omega}{R_I}$ | $\frac{40\ k\Omega}{R_I}$ | $\frac{42\ k\Omega}{R_I}$ | V/V |
| | Resistance from shutdown to GND | | | | 100 | | kΩ |

## 5.6 Operating Characteristics

$T_A$ = 25°C, Gain = 1 V/V

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $P_O$ | Output power | THD + N = 1%, f = 1 kHz, $R_L$ = 3 Ω | $V_{DD}$ = 5 V | | 2.45 | | W |
| | | | $V_{DD}$ = 3.6 V | | 1.22 | | |
| | | | $V_{DD}$ = 2.5 V | | 0.49 | | |
| | | THD + N = 1%, f = 1 kHz, $R_L$ = 4 Ω | $V_{DD}$ = 5 V | | 2.22 | | |
| | | | $V_{DD}$ = 3.6 V | | 1.1 | | |
| | | | $V_{DD}$ = 2.5 V | | 0.47 | | |
| | | THD + N = 1%, f = 1 kHz, $R_L$ = 8 Ω | $V_{DD}$ = 5 V | | 1.36 | | |
| | | | $V_{DD}$ = 3.6 V | | 0.72 | | |
| | | | $V_{DD}$ = 2.5 V | | 0.33 | | |
| THD+N | Total harmonic distortion plus noise | f = 1 kHz, $R_L$ = 3 Ω | $P_O$ = 2 W, $V_{DD}$ = 5 V | | 0.045% | | |
| | | | $P_O$ = 1 W, $V_{DD}$ = 3.6 V | | 0.05% | | |
| | | | $P_O$ = 300 mW, $V_{DD}$ = 2.5 V | | 0.06% | | |
| | | f = 1 kHz, $R_L$ = 4 Ω | $P_O$ = 1.8 W, $V_{DD}$ = 5 V | | 0.03% | | |
| | | | $P_O$ = 0.7 W, $V_{DD}$ = 3.6 V | | 0.03% | | |
| | | | $P_O$ = 300 mW, $V_{DD}$ = 2.5 V | | 0.04% | | |
| | | f = 1 kHz, $R_L$ = 8 Ω | $P_O$ = 1 W, $V_{DD}$ = 5 V | | 0.02% | | |
| | | | $P_O$ = 0.5 W, $V_{DD}$ = 3.6 V | | 0.02% | | |
| | | | $P_O$ = 200 mW, $V_{DD}$ = 2.5 V | | 0.03% | | |
| $k_{SVR}$ | Supply ripple rejection ratio | $V_{DD}$ = 3.6 V, Inputs AC-grounded with $C_I$ = 2 µF, $V_{RIPPLE}$ = 200 $mV_{pp}$ | f = 217 Hz | | –80 | | dB |
| | | | f = 20 Hz to 20 kHz | | –70 | | |
| SNR | Signal-to-noise ratio | $V_{DD}$ = 5 V, $P_O$ = 2 W, $R_L$ = 4 Ω | | | 105 | | dB |
| $V_n$ | Output voltage noise | $V_{DD}$ = 3.6 V, f = 20 Hz to 20 kHz, Inputs AC-grounded with $C_I$ = 2 µF | No weighting | | 15 | | $µV_{RMS}$ |
| | | | A weighting | | 12 | | |
| CMRR | Common mode rejection ratio | $V_{DD}$ = 3.6 V, $V_{IC}$ = 1 $V_{pp}$ | f = 217 Hz | | –65 | | dB |
| $Z_I$ | Input impedance | | | 38 | 40 | 44 | kΩ |
| | Start-up time from shutdown | $V_{DD}$ = 3.6 V, No $C_{BYPASS}$ | | | 4 | | µs |
| | | $V_{DD}$ = 3.6 V, $C_{BYPASS}$ = 0.1 µF | | | 27 | | ms |

## 5.7 Dissipation Ratings

| PACKAGE | $T_A \leq 25°C$ POWER RATING | DERATING FACTOR(1) | $T_A$ = 70°C POWER RATING | $T_A$ = 85°C POWER RATING |
|---|---|---|---|---|
| DGN | 2.13 W | 17.1 mW/°C | 1.36 W | 1.11 W |

(1) Derating factor based on High-k board layout.

## Typical Characteristics

**Table 5-1. Table of Graphs**

| | | FIGURE |
|---|---|---|
| Output power | vs Supply voltage | Figure 5-1 |
| | vs Load resistance | Figure 5-2 |
| Power dissipation | vs Output power | Figure 5-3, Figure 5-4 |
| Total harmonic distortion + noise | vs Output power | Figure 5-5, Figure 5-6, Figure 5-7 |
| | vs Frequency | Figure 5-8, Figure 5-9, Figure 5-10, Figure 5-11, Figure 5-12 |
| | vs Common-mode input voltage | Figure 5-13 |
| Supply voltage rejection ratio | vs Frequency | Figure 5-14, Figure 5-15, Figure 5-16, Figure 5-17 |
| Supply voltage rejection ratio | vs Common-mode input voltage | Figure 5-18 |
| GSM Power supply rejection | vs Time | Figure 5-19 |
| GSM Power supply rejection | vs Frequency | Figure 5-20 |
| Common-mode rejection ratio | vs Frequency | Figure 5-21 |
| | vs Common-mode input voltage | Figure 5-22 |
| Closed loop gain/phase | vs Frequency | Figure 5-23 |
| Open loop gain/phase | vs Frequency | Figure 5-24 |
| Supply current | vs Supply voltage | Figure 5-25 |
| | vs Shutdown voltage | Figure 5-26 |
| Start-up time | vs Bypass capacitor | Figure 5-27 |

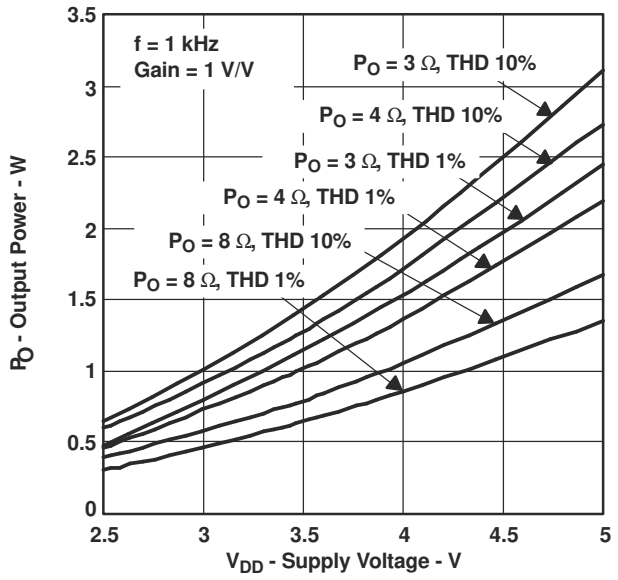



**Figure 5-1. Output Power vs Supply Voltage**

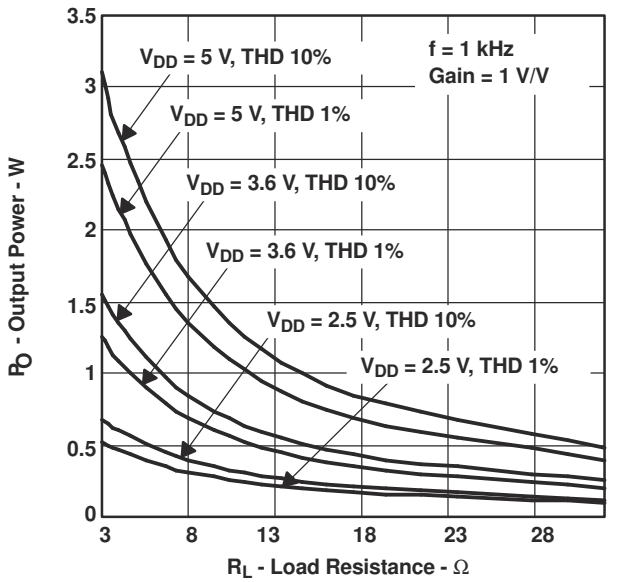



**Figure 5-2. Output Power vs Load Resistance**

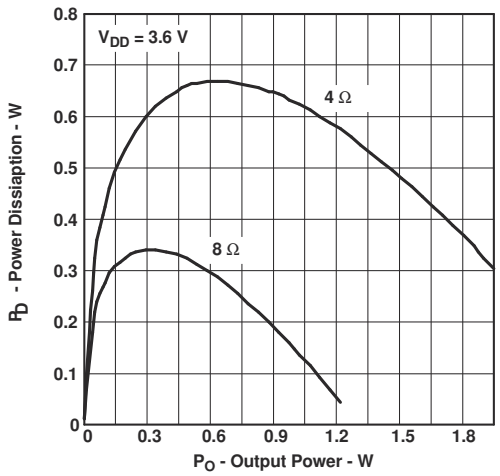



**Figure 5-3. Power Dissipation vs Output Power**

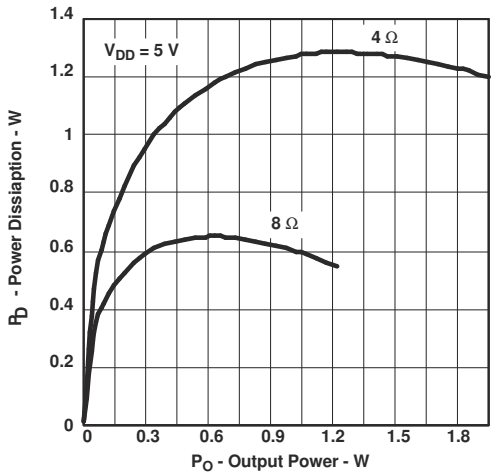



**Figure 5-4. Power Dissipation vs Output Power**

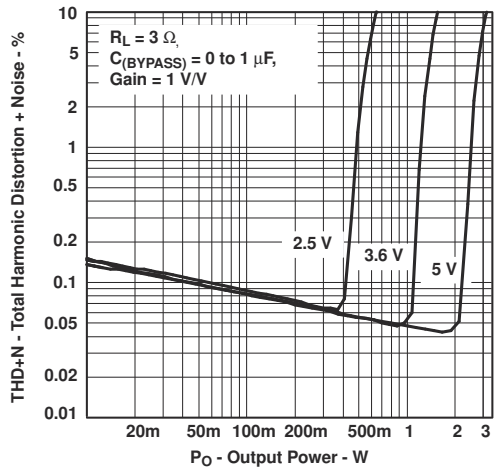



**Figure 5-5. Total Harmonic Distortion + Noise vs Output Power**

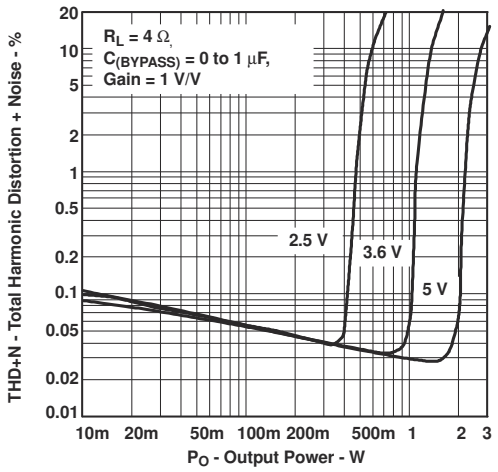



**Figure 5-6. Total Harmonic Distortion + Noise vs Output Power**

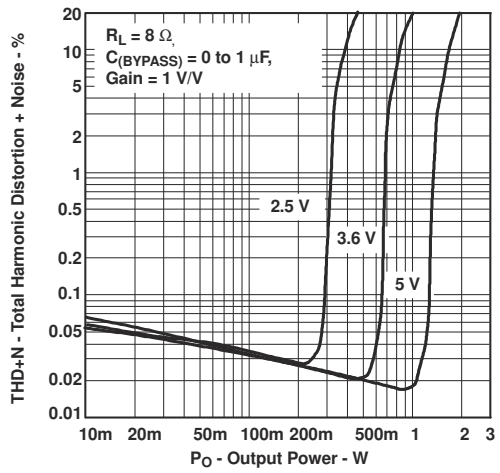



**Figure 5-7. Total Harmonic Distortion + Noise vs Output Power**

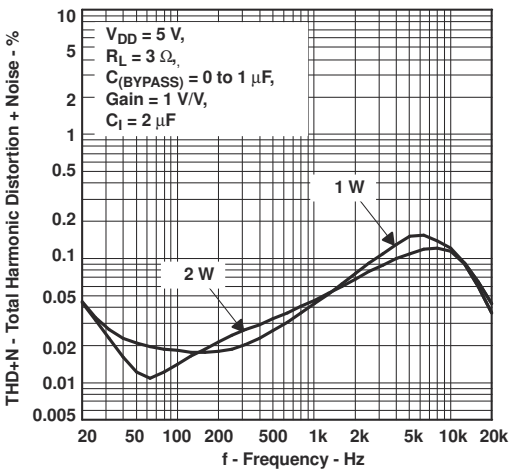



**Figure 5-8. Total Harmonic Distortion + Noise vs Frequency**

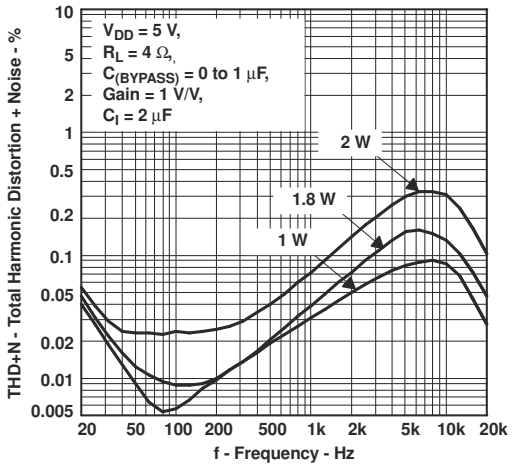



**Figure 5-9. Total Harmonic Distortion + Noise vs Frequency**

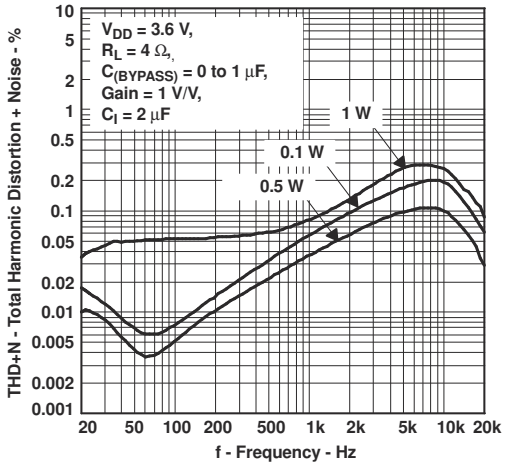



**Figure 5-10. Total Harmonic Distortion + Noise vs Frequency**

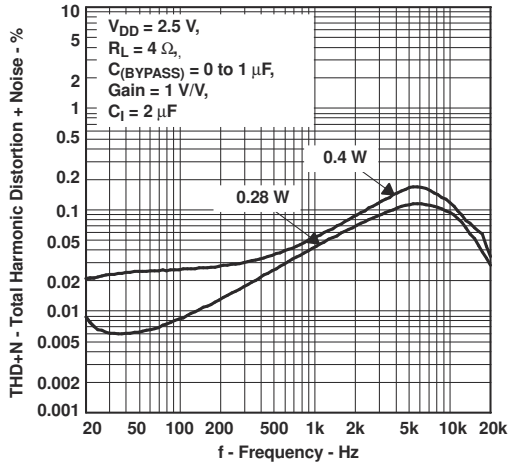



**Figure 5-11. Total Harmonic Distortion + Noise vs Frequency**

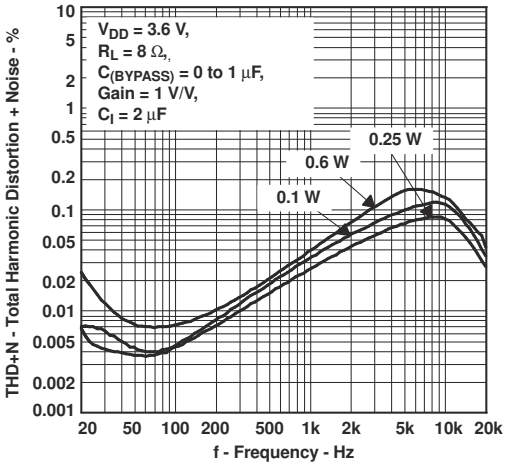



**Figure 5-12. Total Harmonic Distortion + Noise vs Frequency**

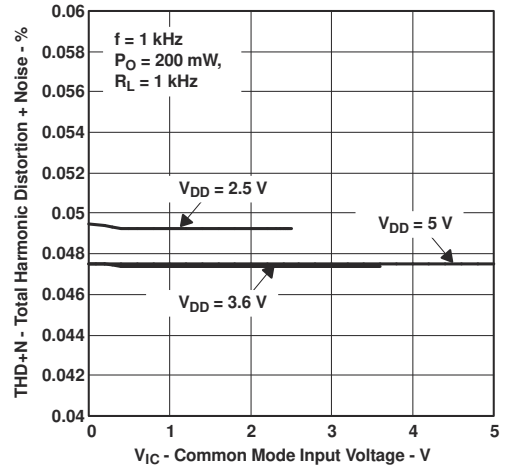



**Figure 5-13. Total Harmonic Distortion + Noise vs Common-Mode Input Voltage**

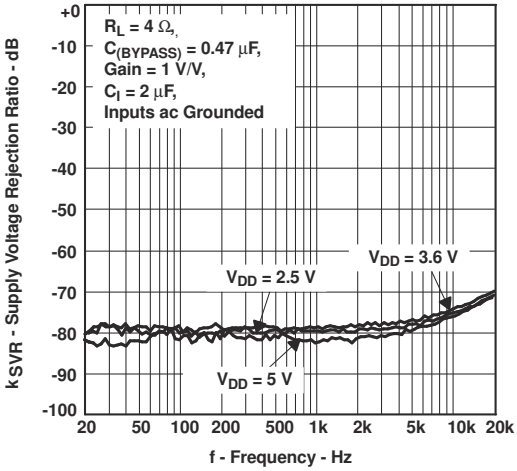



**Figure 5-14. Supply Voltage Rejection Ratio vs Frequency**

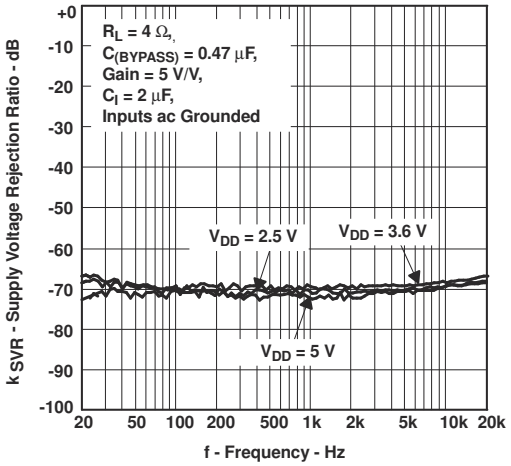



**Figure 5-15. Supply Voltage Rejection Ratio vs Frequency**

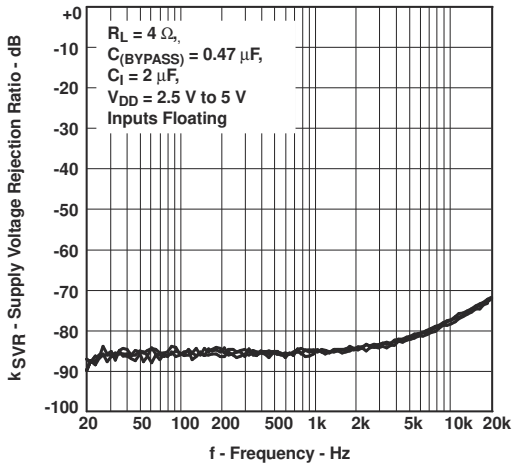



**Figure 5-16. Supply Ripple Rejection Ratio vs Frequency**

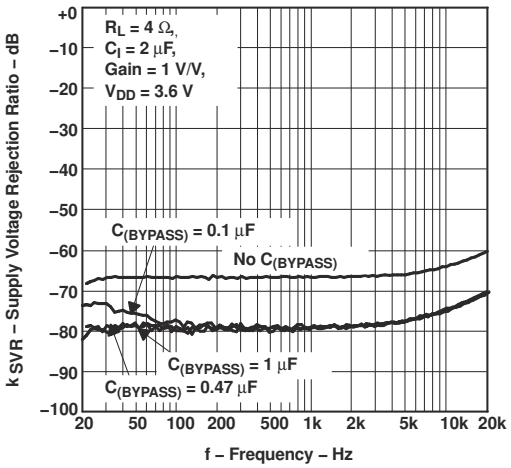



**Figure 5-17. Supply Voltage Rejection Ratio vs Frequency**

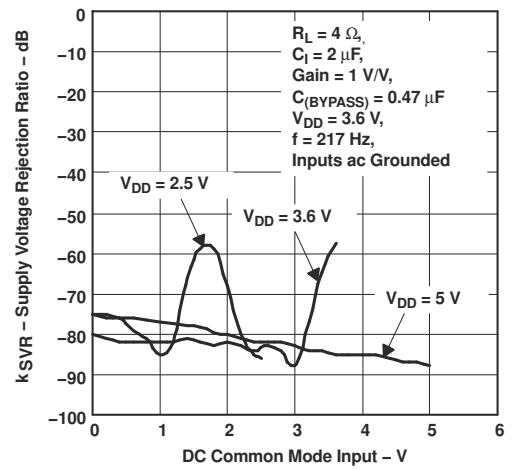



**Figure 5-18. Supply Voltage Rejection Ratio vs DC Common-Mode Input**

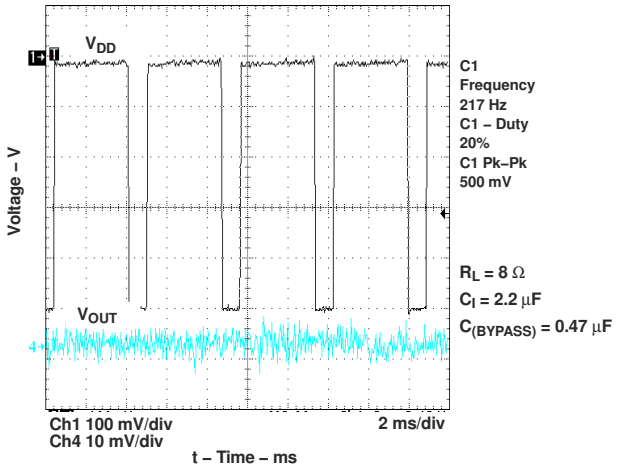



**Figure 5-19. GSM Power Supply Rejection vs Time**

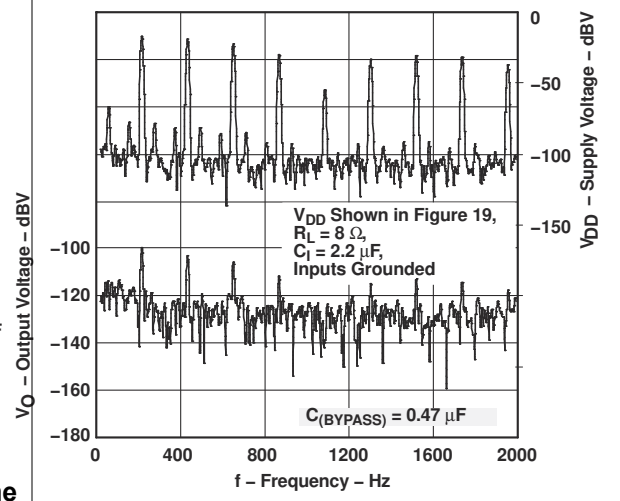



**Figure 5-20. GSM Power Supply Rejection vs Frequency**

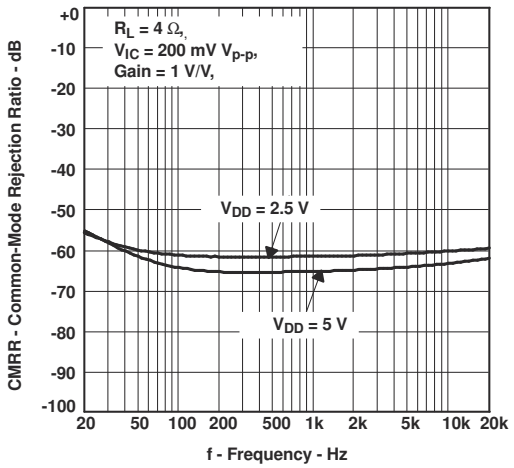



**Figure 5-21. Common-Mode Rejection Ratio vs Frequency**

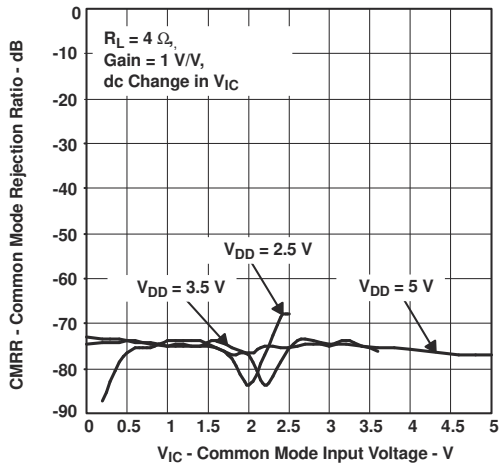



**Figure 5-22. Common-Mode Rejection Ratio vs Common-Mode Input Voltage**

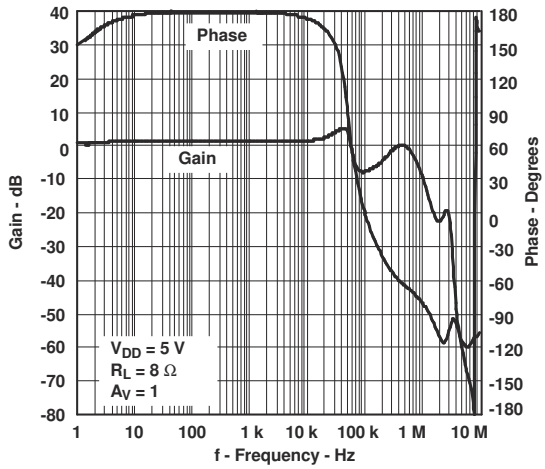



**Figure 5-23. Closed Loop Gain/Phase vs Frequency**

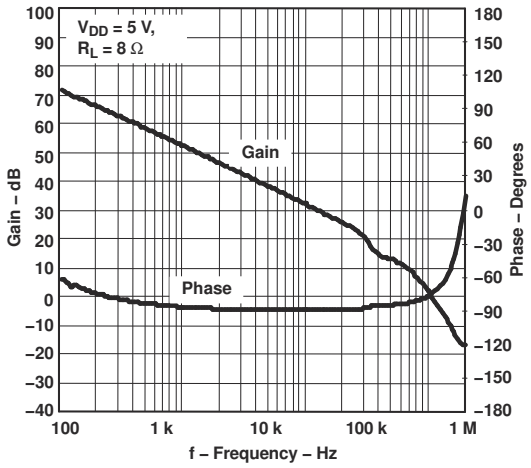



**Figure 5-24. Open Loop Gain/Phase vs Frequency**

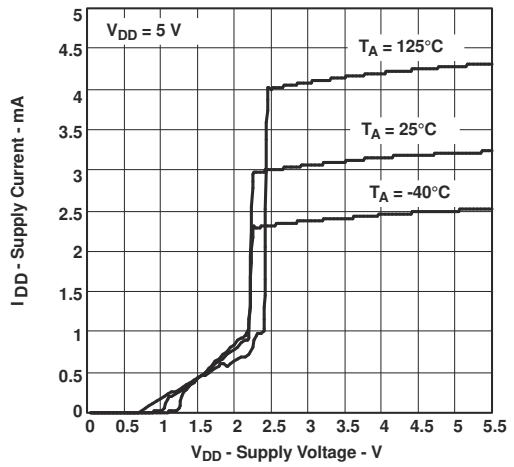



**Figure 5-25. Supply Current vs Supply Voltage**

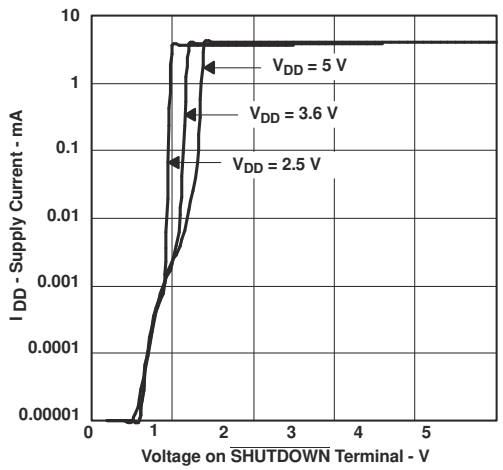



**Figure 5-26. Supply Current vs Shutdown Voltage**

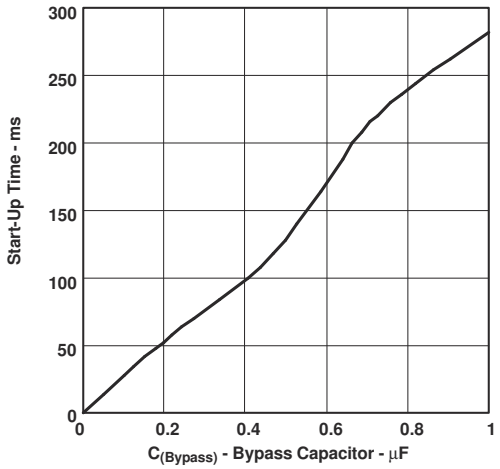


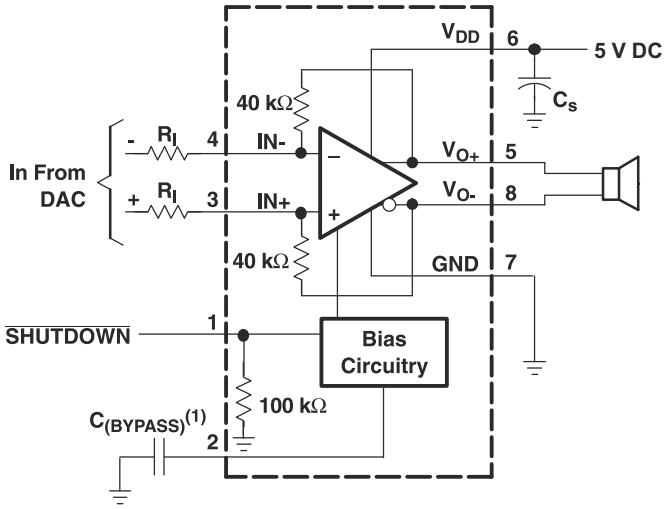

**Figure 5-27. Start-up Time vs Bypass Capacitor**

# 6 Detailed Description

## 6.1 Overview

The TPA6211A1-Q1 device is a fully differential amplifier with differential inputs and outputs. The fully differential amplifier consists of a differential amplifier and a common-mode amplifier. The differential amplifier ensures that the amplifier outputs a differential voltage that is equal to the differential input times the gain. The common-mode feedback ensures that the common-mode voltage at the output is biased around $V_{DD}$ / 2 regardless of the common-mode voltage at the input.

## 6.2 Functional Block Diagram




A. $C_{(BYPASS)}$ is optional

## 6.3 Feature Description

### 6.3.1 Advantages of Fully Differential Amplifiers

Input coupling capacitors are not required. A fully differential amplifier with good CMRR, such as the TPA6211A1-Q1 device, allows the inputs to be biased at voltage other than mid-supply. For example, if a DAC has a lower mid-supply voltage than that of the TPA6211A1-Q1 device, the common-mode feedback circuit compensates, and the outputs are still biased at the mid-supply point of the TPA6211A1-Q1 device. The inputs of the TPA6211A1-Q1 device can be biased from 0.5 V to $V_{DD}$ – 0.8 V. If the inputs are biased outside of that range, input coupling capacitors are required.

A Mid-supply bypass capacitor, $C_{BYPASS}$, is not required. The fully differential amplifier does not require a bypass capacitor. Any shift in the mid-supply voltage affects both positive and negative channels equally, thus canceling at the differential output. Removing the bypass capacitor slightly worsens power supply rejection ratio ($k_{SVR}$), but a slight decrease of $k_{SVR}$ can be acceptable when an additional component can be eliminated (see Figure 5-17).

The RF-immunity is improved. A fully differential amplifier cancels the noise from RF disturbances much better than the typical audio amplifier.

### 6.3.2 Fully Differential Amplifier Efficiency and Thermal Information

Class-AB amplifiers are inefficient, primarily because of voltage drop across the output-stage transistors. The two components of this internal voltage drop are the headroom or DC voltage drop that varies inversely to output power, and the sinewave nature of the output. The total voltage drop can be calculated by subtracting the RMS value of the output voltage from $V_{DD}$. The internal voltage drop multiplied by the average value of the supply current, $I_{DD}$(avg), determines the internal power dissipation of the amplifier.

An easy-to-use equation to calculate efficiency starts out as being equal to the ratio of power from the power supply to the power delivered to the load. To accurately calculate the RMS and average values of power in the load and in the amplifier, the current and voltage waveform shapes must first be understood (see Figure 6-1).

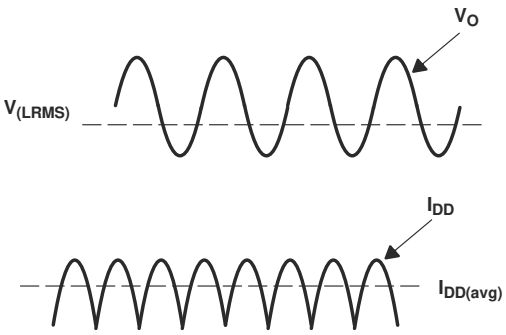



**Figure 6-1. Voltage and Current Waveforms for BTL Amplifiers**

Although the voltages and currents for SE and BTL are sinusoidal in the load, currents from the supply are different between SE and BTL configurations. In an SE application the current waveform is a half-wave rectified shape, whereas in BTL the current waveform is a full-wave rectified waveform. This means RMS conversion factors are different. Keep in mind that for most of the waveform both the push and pull transistors are not on at the same time, which supports the fact that each amplifier in the BTL device only draws current from the supply for half the waveform. Equation 2 to Equation 11 are the basis for calculating amplifier efficiency.

$$\text{Efficiency of a BTL amplifier} = \frac{P_L}{P_{SUP}}$$

Where:

$$P_L = \frac{V_L rms^2}{R_L}, \text{ and } V_{LRMS} = \frac{V_P}{\sqrt{2}}, \text{ therefore, } P_L = \frac{V_P{}^2}{2R_L}$$

$$\text{and } P_{SUP} = V_{DD}\, I_{DD}avg \quad \text{and} \quad I_{DD}avg = \frac{1}{\pi}\int_0^{\pi} \frac{V_P}{R_L} \sin(t)\, dt = -\frac{1}{\pi} \times \frac{V_P}{R_L} [\cos(t)]_0^{\pi} = \frac{2V_P}{\pi R_L}$$

Therefore,

$$P_{SUP} = \frac{2\, V_{DD}\, V_P}{\pi\, R_L}$$

substituting $P_L$ and $P_{SUP}$ into equation 6,

$$\text{Efficiency of a BTL amplifier} = \frac{\frac{V_P{}^2}{2\, R_L}}{\frac{2\, V_{DD}\, V_P}{\pi\, R_L}} = \frac{\pi\, V_P}{4\, V_{DD}}$$

Where:

$$V_P = \sqrt{2\, P_L\, R_L}$$

$P_L$ = Power delivered to load
$P_{SUP}$ = Power drawn from power supply
$V_{LRMS}$ = RMS voltage on BTL load
$R_L$ = Load resistance
$V_P$ = Peak voltage on BTL load
$I_{DD}avg$ = Average current drawn from the power supply
$V_{DD}$ = Power supply voltage
$\eta_{BTL}$ = Efficiency of a BTL amplifier

(1)

$$\eta_{BTL} = \frac{P_L}{P_{SUP}} \tag{2}$$

where

- $\eta_{BTL}$ is the efficiency of a BTL amplifier
- $P_L$ is the power delivered to load
- $P_{SUP}$ is the power drawn from power supply

$P_L$ is calculated with Equation 3, and $V_{LRMS}$ is calculated with Equation 4.

$$P_L = \frac{V_{LRMS}^2}{R_L} \quad (3)$$

where

- $V_{LRMS}$ = RMS voltage on BTL load
- $R_L$ is load resistance

$$V_{LRMS} = \frac{V_P}{\sqrt{2}} \quad (4)$$

where

- $V_P$ is peak voltage on BTL load

Therefore, $P_L$ can be given as Equation 5.

$$P_L = \frac{V_P^2}{2 \times R_L} \quad (5)$$

$P_{SUP}$ is calculated with Equation 6.

$$P_{SUP} = V_{DD} \times I_{DD}avg \quad (6)$$

where

- $V_{DD}$ is power supply voltge
- $I_{DD}avg$ is average current drawn from the power supply

$I_{DD}avg$ is calculated with Equation 7.

$$I_{DD}avg = \frac{1}{\pi}\int_0^{\pi} \frac{V_P}{R_L} \times \sin(t) \times dt = -\frac{1}{\pi} \times \frac{V_P}{R_L} \times \cos(t)_0^{\pi} = \frac{2 \times V_P}{\pi \times R_L} \quad (7)$$

Therefore, $P_{SUP}$ can be given as Equation 8.

$$P_{SUP} = \frac{2 \times V_{DD} \times V_P}{\pi \times R_L} \quad (8)$$

Substituting for $P_L$ and $P_{SUP}$, Equation 2 becomes Equation 9

$$\eta_{BTL} = \frac{\frac{V_P^2}{2 \times R_L}}{\frac{2 \times V_{DD} \times V_P}{\pi \times R_L}} = \frac{\pi \times V_P}{4 \times V_{DD}} \quad (9)$$

$V_P$ is calculated with Equation 10.

$$V_P = \sqrt{2 \times P_L \times R_L} \quad (10)$$

And substituting for $V_P$, $\eta_{BTL}$ can be calculated with Equation 11

$$\eta_{BTL} = \frac{\pi\sqrt{2 \times P_L \times R_L}}{4 \times V_{DD}} \quad (11)$$

A simple formula for calculating the maximum power dissipated ($P_{Dmax}$) can be used for a differential output application:

$$P_{Dmax} = \frac{2V_{DD}^2}{\pi^2 R_L} \quad (12)$$

**Table 6-1. Efficiency and Maximum Ambient Temperature vs Output Power**

| OUTPUT POWER | EFFICIENCY | INTERNAL DISSIPATION | POWER FROM SUPPLY | MAX AMBIENT TEMPERATURE |
|---|---|---|---|---|
| 5-V, 3-Ω SYSTEMS | | | | |
| 0.5 W | 27.2% | 1.34 W | 1.84 W | 54°C |
| 1 W | 38.4% | 1.6 W | 2.6 W | 35°C |
| 2.45 W | 60.2% | 1.62 W | 4.07 W | 34°C |
| 3.1 W | 67.7% | 1.48 W | 4.58 W | 44°C |
| **5-V, 4-Ω BTL SYSTEMS** | | | | |
| 0.5 W | 31.4% | 1.09 W | 1.59 W | 72°C |
| 1 W | 44.4% | 1.25 W | 2.25 W | 60°C |
| 2 W | 62.8% | 1.18 W | 3.18 W | 65°C |
| 2.8 W | 74.3% | 0.97 W | 3.77 W | 80°C |
| **5-V, 8-Ω SYSTEMS** | | | | |
| 0.5 W | 44.4% | 0.625 W | 1.13 W | 105°C (limited by maximum ambient temperature specification) |
| 1 W | 62.8% | 0.592 W | 1.6 W | 105°C (limited by maximum ambient temperature specification) |
| 1.36 W | 73.3% | 0.496 W | 1.86 W | 105°C (limited by maximum ambient temperature specification) |
| 1.7 W | 81.9% | 0.375 W | 2.08 W | 105°C (limited by maximum ambient temperature specification) |

Equation 11 is used to calculate efficiencies for four different output power levels, see Table 6-1. The efficiency of the amplifier is quite low for lower power levels and rises sharply as power to the load is increased resulting in a nearly flat internal power dissipation over the normal operating range. The internal dissipation at full output power is less than in the half power range. Calculating the efficiency for a specific system is the key to proper power supply design. For a 2.8-W audio system with 4-Ω loads and a 5-V supply, the maximum draw on the power supply is almost 3.8 W.

A final point to remember about Class-AB amplifiers is how to manipulate the terms in the efficiency equation to the utmost advantage when possible. In Equation 11, $V_{DD}$ is in the denominator. This indicates that as $V_{DD}$ goes down, efficiency goes up.

The maximum ambient temperature depends on the heat sinking ability of the PCB system. Given $R_{\theta JA}$ (junction-to-ambient thermal resistance), the maximum allowable junction temperature, and the internal dissipation at 1-W output power with a 4-Ohm load, the maximum ambient temperature can be calculated with Equation 13. The maximum recommended junction temperature for the TPA6211A1-Q1 device is 150°C.

$$T_A(\text{Max}) = T_J(\text{Max}) - R_{\theta JA} \times P_D = 150 - 71.7 \times 1.25 = 60°C \quad (13)$$

Equation 13 shows that the maximum ambient temperature is 60°C at 1-W output power and 4-Ohm load with a 5-V supply.

Table 6-1 shows that the thermal performance must be considered when using a Class-AB amplifier to keep junction temperatures in the specified range. The TPA6211A1-Q1 device is designed with thermal protection that turns the device off when the junction temperature surpasses 150°C to prevent damage to the IC. In addition,

using speakers with an impedance higher than 4 Ω dramatically increases the thermal performance by reducing the output current.

### 6.3.3 Differential Output Versus Single-Ended Output

Figure 6-2 shows a Class-AB audio power amplifier (APA) in a fully differential configuration. The TPA6211A1-Q1 amplifier has differential outputs driving both ends of the load. One of several potential benefits to this configuration is power to the load. The differential drive to the speaker means that as one side is slewing up, the other side is slewing down, and vice versa. This in effect doubles the voltage swing on the load as compared to a ground-referenced load. Plugging 2 × $V_{O(PP)}$ into the power equation (Equation 14) yields four-times the output power (as the voltage is squared) from the same supply rail and load impedance (see Equation 16 and Equation 17).

$$V_{(rms)} = \frac{V_{O(PP)}}{2\sqrt{2}}$$

$$\text{Power} = \frac{V_{(rms)}^2}{R_L} \tag{14}$$

$$\text{Power}_{(S-E)} = \frac{V_{(rms)}^2}{R_L} = \frac{\left(\frac{V_{O(PP)}}{2\sqrt{2}}\right)^2}{R_L} = \frac{V_{O(PP)}^2}{8R_L} \tag{15}$$

$$\text{Power}_{(Diff)} = \frac{V_{(rms)}^2}{R_L} = \frac{\left(\frac{2 \times V_{O(PP)}}{2\sqrt{2}}\right)^2}{R_L} = \frac{V_{O(PP)}^2}{2R_L} \tag{16}$$

$$\text{Power}_{(Diff)} = 4 \times \text{Power}_{(S-E)} \tag{17}$$

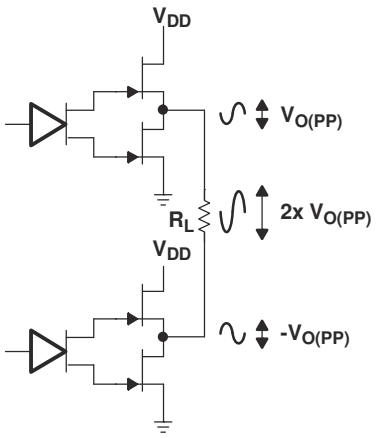



**Figure 6-2. Differential Output Configuration**

In a typical automotive application operating at 5 V, bridging raises the power into an 8-Ω speaker from a singled-ended (SE, ground reference) limit of 390 mW to 1.56 W. This is a 6-dB improvement in sound power, or loudness of the sound. In addition to increased power, there are frequency-response concerns. Consider the single-supply SE configuration shown in Figure 6-3. A coupling capacitor ($C_C$) is required to block the DC-offset voltage from the load. This capacitor can be quite large (approximately 33 µF to 1000 µF) so it tends to be expensive, heavy, occupy valuable PCB area, and have the additional drawback of limiting low-frequency performance. This frequency-limiting effect is due to the high-pass filter network created with the speaker impedance and the coupling capacitance. This is calculated with Equation 18.

$$f_c = \frac{1}{2\pi R_L C_C} \quad (18)$$

For example, a 68-µF capacitor with an 8-Ω speaker would attenuate low frequencies below 293 Hz. The BTL configuration cancels the DC offsets, which eliminates the need for the blocking capacitors. Low-frequency performance is then limited only by the input network and speaker response. Cost and PCB space are also minimized by eliminating the bulky coupling capacitor.

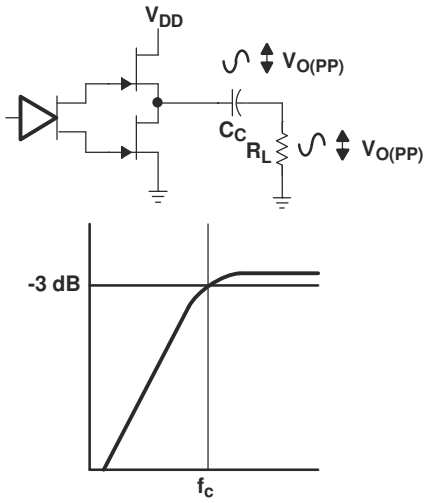



**Figure 6-3. Single-Ended Output and Frequency Response**

Increasing power to the load does carry a penalty of increased internal power dissipation. The increased dissipation is understandable considering that the BTL configuration produces four-times the output power of the SE configuration.

## 6.4 Device Functional Modes

The TPA6211A1-Q1 device can be put in shutdown mode when asserting $\overline{\text{SHUTDOWN}}$ pin to a logic LOW. While in shutdown mode, the device output stage is turned off and set into high impedance, making the current consumption very low. The device exits shutdown mode when a HIGH logic level is applied to $\overline{\text{SHUTDOWN}}$ pin.

# 7 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

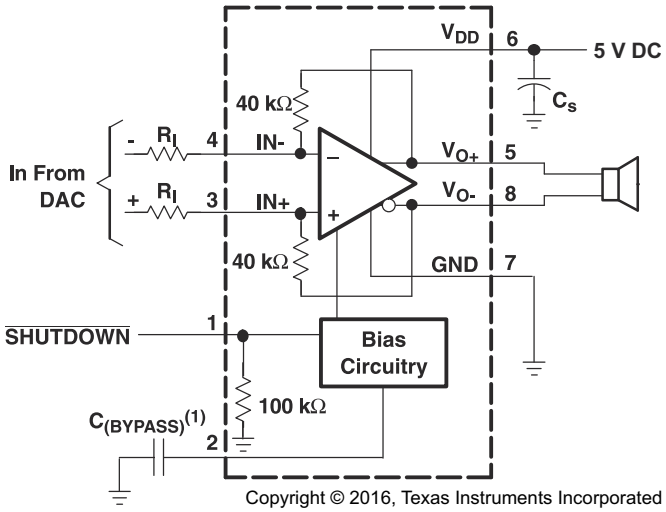
## 7.1 Application Information

The TPA6211A1-Q1 is a fully-differential amplifier designed to drive a speaker with at least 3-Ω impedance while consuming only 20-mm$^2$ total printed-circuit board (PCB) area in most applications.

## 7.2 Typical Applications

Figure 7-1 shows a typical application circuit for the TPA6211A1-Q1 with a speaker, input resistors, and supporting power supply decoupling capacitors.

### *7.2.1 Typical Differential Input Application*




A. $C_{(BYPASS)}$ is optional

**Figure 7-1. Typical Differential Input Application Schematic**

Typical values are shown in Table 7-1.

**Table 7-1. Typical Component Values**

| COMPONENT | VALUE |
|---|---|
| $R_I$ | 40 kΩ |
| $C_{BYPASS}$ (1) | 0.22 µF |
| $C_S$ | 1 µF |
| $C_I$ | 0.22 µF |

(1) $C_{BYPASS}$ is optional.

#### 7.2.1.1 Design Requirements

For this design example, use the parameters listed in Table 7-2 as the input parameters.

**Table 7-2. Design Parameters**

| PARAMETER | EXAMPLE VALUE |
|---|---|
| Power supply voltage | 2.5 V to 5.5 V |

**Table 7-2. Design Parameters (continued)**

| PARAMETER | EXAMPLE VALUE |
|---|---|
| Current | 4 mA to 5 mA |
| Shutdown | High > 1.55 V |
| | Low < 0.5 V |
| Speaker | 3 Ω, 4 Ω, or 8 Ω |

#### 7.2.1.2 Detailed Design Procedure

##### *7.2.1.2.1 Resistors ($R_I$)*

The input resistor ($R_I$) can be selected to set the gain of the amplifier according to Equation 19.

$$\text{Gain} = \frac{R_F}{R_I} \tag{19}$$

The internal feedback resistors ($R_F$) are trimmed to 40 kΩ.

Resistor matching is very important in fully differential amplifiers. The balance of the output on the reference voltage depends on matched ratios of the resistors. CMRR, PSRR, and the cancellation of the second harmonic distortion diminishes if resistor mismatch occurs. Therefore, TI recommends 1%-tolerance resistors or better to optimize performance.

##### *7.2.1.2.2 Bypass Capacitor ($C_{BYPASS}$) and Start-Up Time*

The internal voltage divider at the BYPASS pin of this device sets a mid-supply voltage for internal references and sets the output common mode voltage to $V_{DD}$ / 2. Adding a capacitor filters any noise into this pin, increasing $k_{SVR}$. $C_{BYPASS}$ also determines the rise time of $V_{O+}$ and $V_{O–}$ when the device exits shutdown. The larger the capacitor, the slower the rise time.

##### *7.2.1.2.3 Input Capacitor ($C_I$)*

The TPA6211A1-Q1 device does not require input coupling capacitors when driven by a differential input source biased from 0.5 V to $V_{DD}$ – 0.8 V. Use 1% tolerance or better gain-setting resistors if not using input coupling capacitors.

In the single-ended input application, an input capacitor ($C_I$) is required to allow the amplifier to bias the input signal to the proper DC level. In this case, $C_I$ and $R_I$ form a high-pass filter with the corner frequency defined in Equation 20.

$$f_c = \frac{1}{2\pi R_I C_I} \tag{20}$$

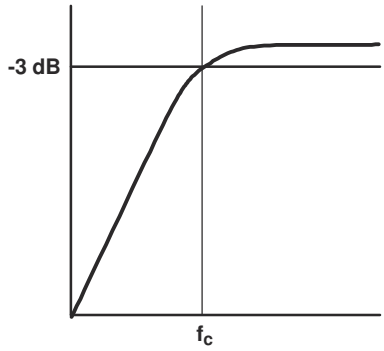



**Figure 7-2. Input Filter Cutoff Frequency**

The value of $C_I$ is an important consideration, as it directly affects the bass (low frequency) performance of the circuit. Consider the example where $R_I$ is 10 kΩ and the specification calls for a flat bass response down to 100 Hz. Equation 20 is reconfigured as Equation 21.

$$C_I = \frac{1}{2\pi R_I f_c} \tag{21}$$

In this example, $C_I$ is 0.16 µF, so the likely choice ranges from 0.22 µF to 0.47 µF. TI recommends the use of ceramic capacitors because they are the best choice in preventing leakage current. When polarized capacitors are used, the positive side of the capacitor faces the amplifier input in most applications. The input DC level is held at $V_{DD}$ / 2, typically higher than the source DC level. Confirming the capacitor polarity in the application is important.

#### *7.2.1.2.4 Band-Pass Filter ($R_I$, $C_I$, and $C_F$)*

Having signal filtering beyond the one-pole high-pass filter formed by the combination of $C_I$ and $R_I$ can be desirable. A low-pass filter can be added by placing a capacitor ($C_F$) between the inputs and outputs, forming a band-pass filter.

An example of when this technique might be used would be in an application where the desirable pass-band range is between 100 Hz and 10 kHz, with a gain of 4 V/V. Equation 22 to Equation 29 allow the proper values of $C_F$ and $C_I$ to be determined.

##### *7.2.1.2.4.1 Step 1: Low-Pass Filter*

$$f_{c(LPF)} = \frac{1}{2\pi R_F C_F} \tag{22}$$

$$f_{c(LPF)} = \frac{1}{2\pi\, 40\,\text{k}\Omega\, C_F} \tag{23}$$

Therefore,

$$C_F = \frac{1}{2\pi 40\ \text{k}\Omega\ f_{c(LPF)}} \tag{24}$$

Substituting 10 kHz for $f_{c(LPF)}$ and solving for $C_F$:

$$C_F = 398\ \text{pF} \tag{25}$$

##### *7.2.1.2.4.2 Step 2: High-Pass Filter*

$$f_{c(HPF)} = \frac{1}{2\pi R_I C_I} \tag{26}$$

Because the application in this case requires a gain of 4 V/V, $R_I$ must be set to 10 kΩ.

Substituting $R_I$ into Equation 26.

$$f_{c(HPF)} = \frac{1}{2\pi 10\ \text{k}\Omega\ C_I} \tag{27}$$

Therefore,

$$C_I = \frac{1}{2\pi 10\ k\Omega\ f_{c(HPF)}} \quad (28)$$

Substituting 100 Hz for $f_{c(HPF)}$ and solving for $C_I$:

$$C_I = 0.16\ \mu F \quad (29)$$

At this point, a first-order band-pass filter has been created with the low-frequency cutoff set to 100 Hz and the high-frequency cutoff set to 10 kHz.

The process can be taken a step further by creating a second-order high-pass filter. This is accomplished by placing a resistor ($R_a$) and capacitor ($C_a$) in the input path. $R_a$ must be at least 10 times smaller than $R_I$; otherwise its value has a noticeable effect on the gain, as $R_a$ and $R_I$ are in series.

#### *7.2.1.2.4.3 Step 3: Additional Low-Pass Filter*

$R_a$ must be at least ten-times smaller than $R_I$. Set $R_a$ = 1 kΩ

$$f_{c(LPF)} = \frac{1}{2\pi R_a C_a} \quad (30)$$

Therefore,

$$C_a = \frac{1}{2\pi\ 1k\Omega\ f_{c(LPF)}} \quad (31)$$

Substituting 10 kHz for $f_{c(LPF)}$ and solving for $C_a$:

$$C_a = 160\ pF \quad (32)$$

Figure 7-3 is a bode plot for the band-pass filter in the previous example. Figure 7-8 shows how to configure the TPA6211A1-Q1 device as a band-pass filter.

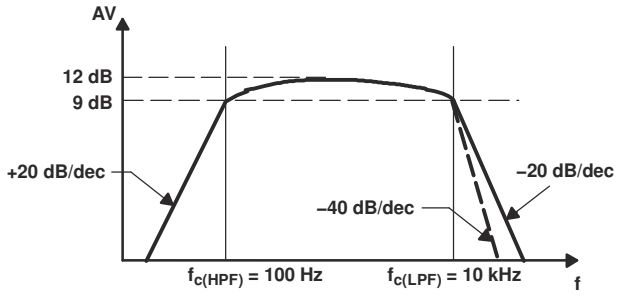



**Figure 7-3. Bode Plot**

#### *7.2.1.2.5 Decoupling Capacitor ($C_S$)*

The TPA6211A1-Q1 device is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power-supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 µF to 1 µF, placed as close as possible to the device $V_{DD}$ lead works best. For filtering lower frequency noise signals, a 10-µF or greater capacitor placed near the audio power amplifier also helps, but is not required in most applications because of the high PSRR of this device.

#### 7.2.1.2.6 Using Low-ESR Capacitors

Low-ESR capacitors are recommended throughout this applications section. A real (as opposed to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance the more the real capacitor behaves like an ideal capacitor.

### 7.2.1.3 Application Curves

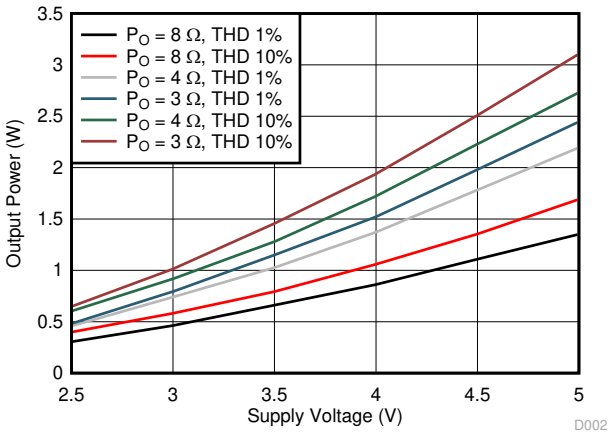



**Figure 7-4. Output Power vs Supply Voltage**

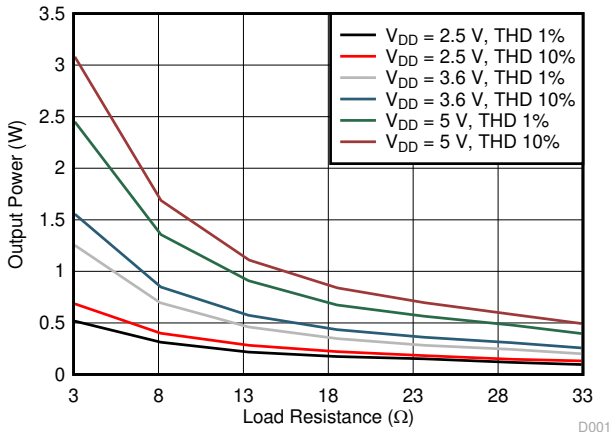
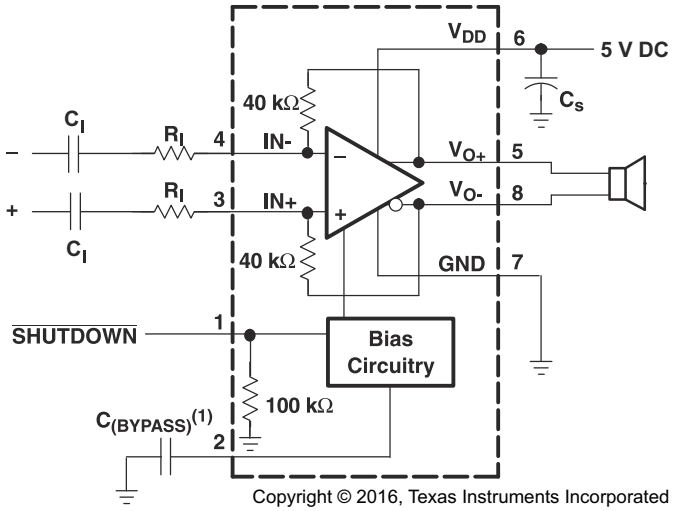



**Figure 7-5. Output Power vs Load Resistance**

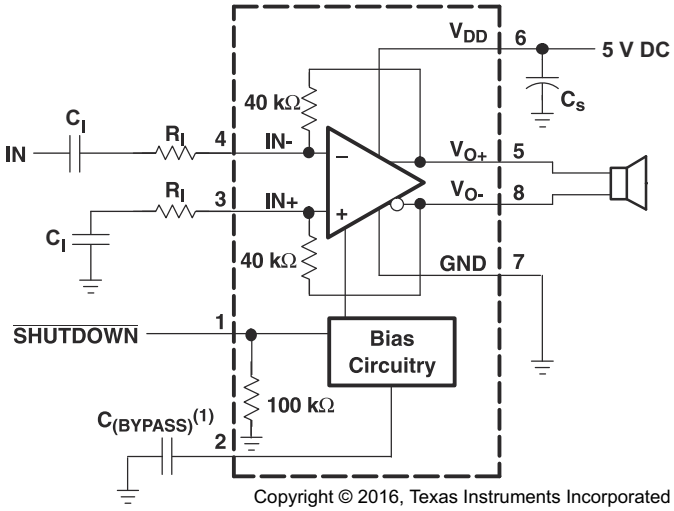
### 7.2.2 Other Application Circuits

Figure 7-6, Figure 7-7, and Figure 7-8 show example circuits using the TPA6211A1-Q1 device.



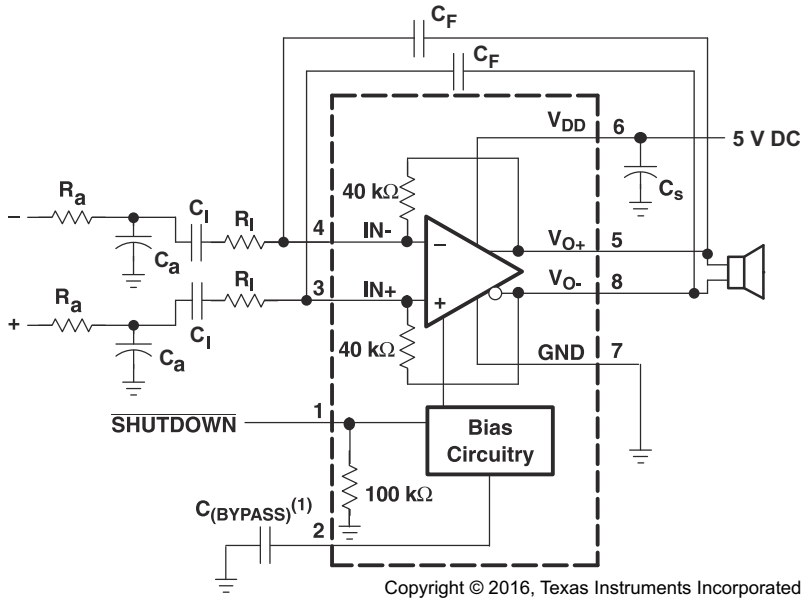

A. $C_{(BYPASS)}$ is optional

**Figure 7-6. Differential Input Application Schematic Optimized With Input Capacitors**




A. $C_{(BYPASS)}$ is optional

**Figure 7-7. Single-Ended Input Application Schematic**




A. $C_{(BYPASS)}$ is optional

**Figure 7-8. Differential Input Application Schematic With Input Bandpass Filter**

## 7.3 Power Supply Recommendations

The TPA6211A1-Q1 device is designed to operate from an input voltage supply range between 2.5 V and 5.5 V. Therefore, the output voltage range of power supply must be within this range and well regulated. The current capability of upper power should not exceed the maximum current limit of the power switch.

### *7.3.1 Power Supply Decoupling Capacitor*

The TPA6211A1-Q1 device requires adequate power supply decoupling to ensure a high efficiency operation with low total harmonic distortion (THD). Place a low equivalent series resistance (ESR) ceramic capacitor, typically 0.1 µF, as close as possible of the $V_{DD}$ pin. This choice of capacitor and placement helps with higher frequency transients, spikes, or digital hash on the line. TI recommends placing a 2.2-µF to 10-µF capacitor on the $V_{DD}$ supply trace. This larger capacitor acts as a charge reservoir, providing energy faster than the board supply, thus helping to prevent any droop in the supply voltage.

## 7.4 Layout

### 7.4.1 Layout Guidelines

Place all the external components close to the TPA6211A1-Q1 device. The input resistors need to be close to the device input pins so noise does not couple on the high impedance nodes between the input resistors and the input amplifier of the device. Placing the decoupling capacitors, $C_S$ and $C_{BYPASS}$, close to the TPA6211A1-Q1 device is important for the efficiency of the amplifier. Any resistance or inductance in the trace between the device and the capacitor can cause a loss in efficiency.

### 7.4.2 Layout Example

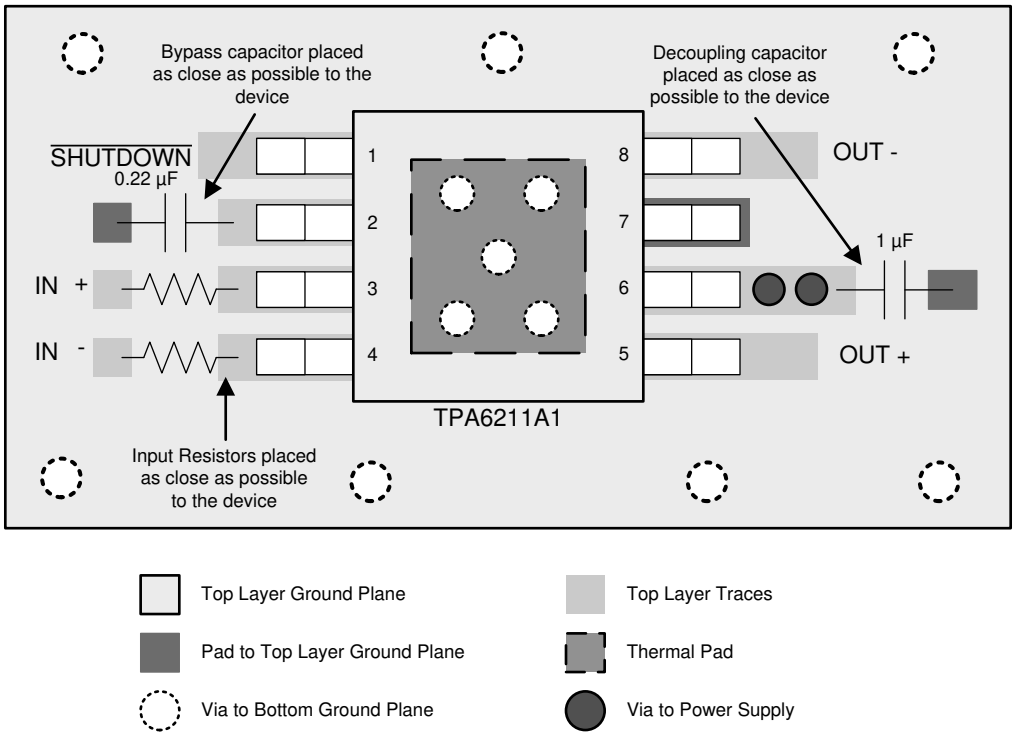



**Figure 7-9. TPA6211A1-Q1 8-Pin HVSSOP (DGN) Board Layout**

# 8 Device and Documentation Support

## 8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 8.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 8.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

## 8.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 8.5 Glossary

| | |
|---|---|
| TI Glossary | This glossary lists and explains terms, acronyms, and definitions. |

# 9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision F (February 2024) to Revision G (May 2024) | Page |
|---|---|
| • Changed the *ESD Ratings* for CDM to ±1000V | 4 |

| Changes from Revision E (August 2019) to Revision F (February 2024) | Page |
|---|---|
| • Changed *Device HBM ESD classification level* in the Feature: Qualified for automotive applications | 1 |
| • Changed the *ESD Ratings* for HBM to ±2000V | 4 |

| Changes from Revision D (August 2019) to Revision E (August 2019) | Page |
|---|---|
| • Changed packaging to HVSSOP | 1 |
| • Changed packaging to HVSSOP | 4 |
| • Changed packaging to HVSSOP | 25 |

| Changes from Revision C (August 2016) to Revision D (August 2019) | Page |
|---|---|
| • Deleted *AEC-Q100* from the Feature: Qualified for automotive applications | 1 |
| • Deleted Feature: Temperature Grade 2 | 1 |
| • Changed the *ESD Ratings* table | 4 |

**Changes from Revision B (January 2014) to Revision C (August 2016)** **Page**

- Added *Device Information* table, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes* section, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ..... 1
- Added missing Max Ambient Temperature values to Table 6-1 ..... 13
- Changed 45.9 to 71.7, 1.27 to 1.25, and 91.7 to 60 in Equation 13 ..... 13

**Changes from Revision A (November 2013) to Revision B (January 2014)** **Page**

- Added three new equations to the *DIFFERENTIAL OUTPUT VERSUS SINGLE-ENDED OUTPUT* section in order to show difference between single-ended and differential output..... 17

**Changes from Revision * (June 2011) to Revision A (November 2013)** **Page**

- Deleted *Designed for Wireless or Cellular Handsets and PDAs* from *Features* list..... 1
- Deleted *Ordering Information* table..... 3
- Changed reference from "equation 6" to Equation 26 in the *High-Pass Filter* section..... 21

## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TPA6211A1TDGNRQ1 | ACTIVE | HVSSOP | DGN | 8 | 2500 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 105 | 6211Q | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.



**OTHER QUALIFIED VERSIONS OF TPA6211A1-Q1 :**

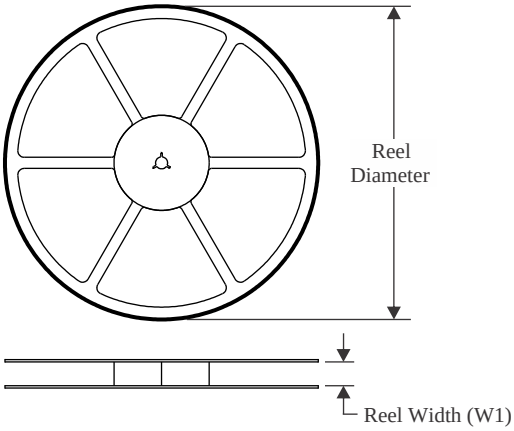
- Catalog : TPA6211A1

NOTE: Qualified Version Definitions:

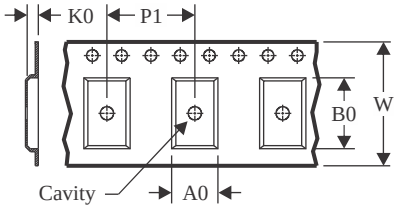
- Catalog - TI's standard catalog product

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

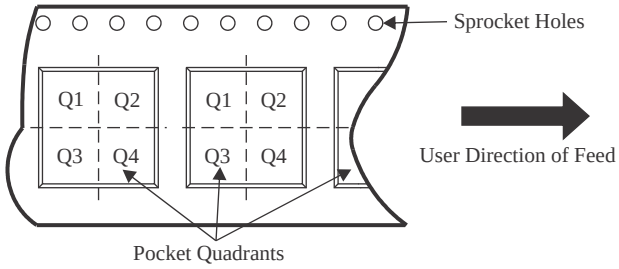



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

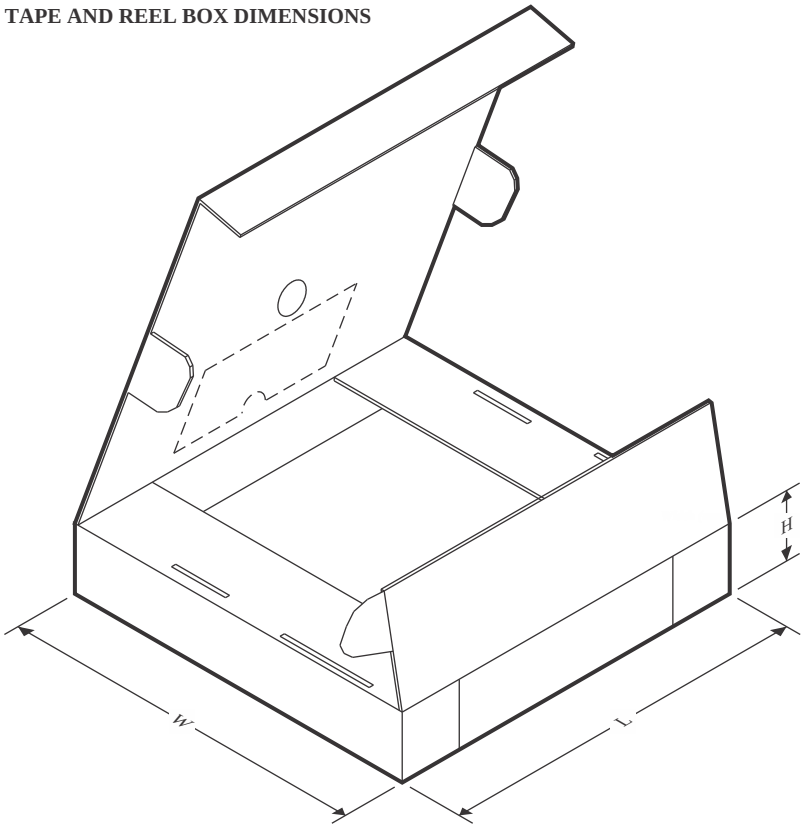
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPA6211A1TDGNRQ1 | HVSSOP | DGN | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPA6211A1TDGNRQ1 | HVSSOP | DGN | 8 | 2500 | 346.0 | 346.0 | 29.0 |

# GENERIC PACKAGE VIEW

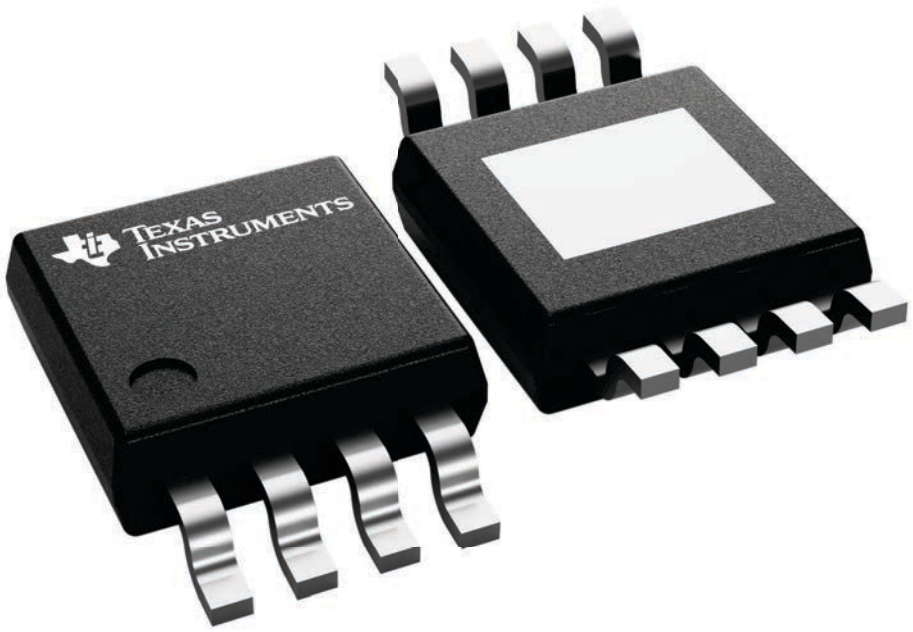
## DGN 8

## PowerPAD™ HVSSOP - 1.1 mm max height

**3 x 3, 0.65 mm pitch**

SMALL OUTLINE PACKAGE

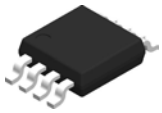
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.




4225482/B

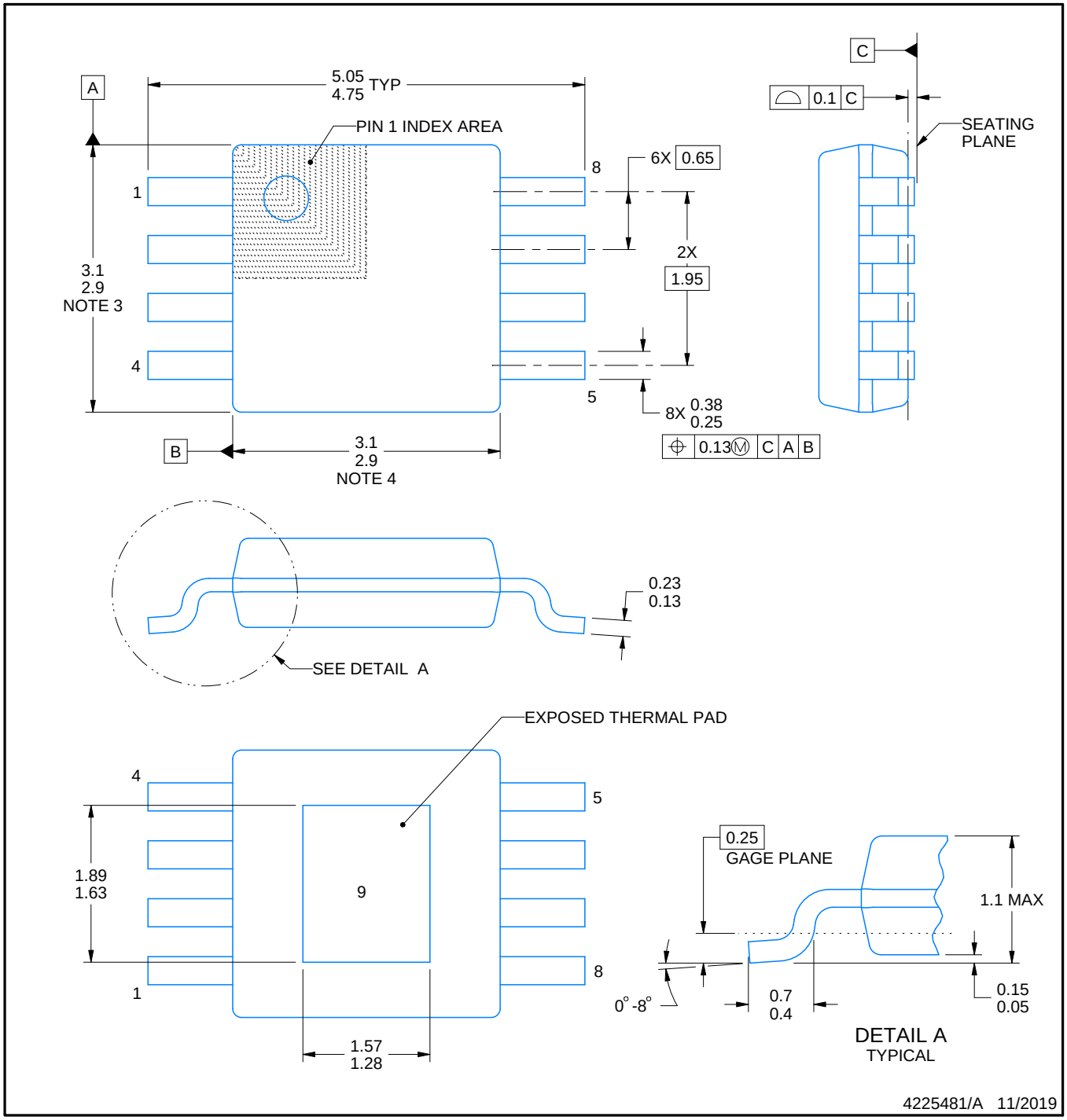
# PACKAGE OUTLINE

## DGN0008D



## PowerPAD™ VSSOP - 1.1 mm max height

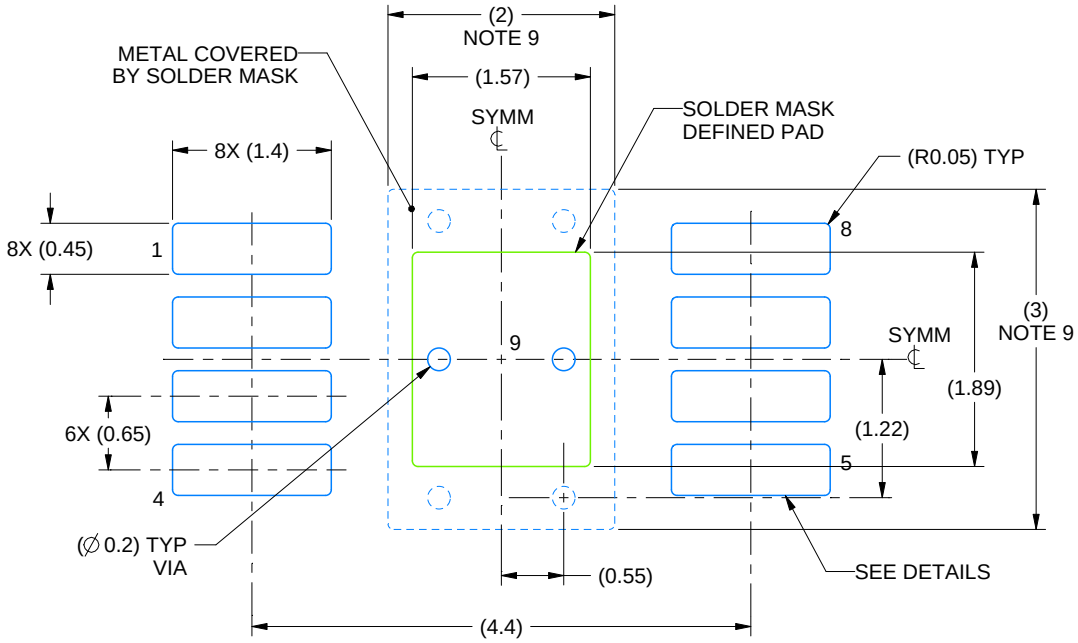
SMALL OUTLINE PACKAGE



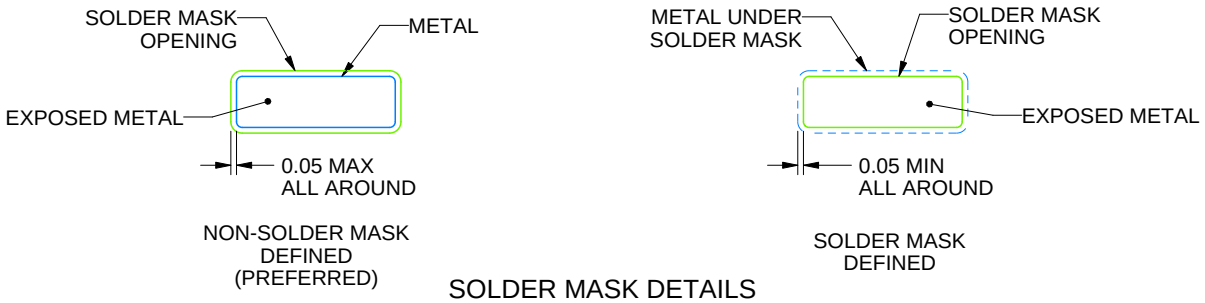

PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

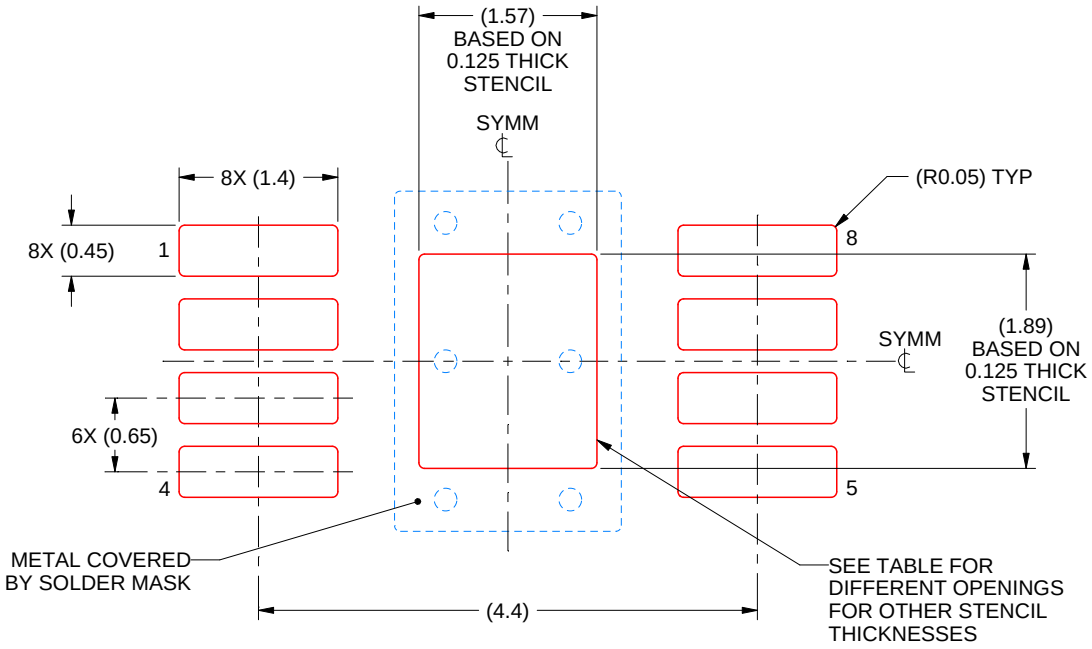



SOLDER MASK DETAILS

4225481/A 11/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.




SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

| STENCIL THICKNESS | SOLDER STENCIL OPENING |
|---|---|
| 0.1 | 1.76 X 2.11 |
| 0.125 | 1.57 X 1.89 (SHOWN) |
| 0.15 | 1.43 X 1.73 |
| 0.175 | 1.33 X 1.60 |

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NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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