Very Low Input, Very Low Dropout, 2-Amp Regulator With Enable

FEATURES

- **Input Voltage as low as 1.425 V**
- **380 mV Dropout Maximum at 2 A**
- **Adjustable Output from 0.5 V**
- **Protections: Current Limit and Thermal Shutdown**
- **Enable Pin**
- **1-µA Quiescent Current in Shutdown Mode**
- **Full Industrial Temperature Range**
- **Available in SOIC-8, Fully RoHS-Compliant Package**

APPLICATIONS

- **Telecom/Networking Cards**
- **Motherboards/Peripheral Cards**
- **Industrial**
- **Wireless Infrastructure**
- **Set-Top Boxes**
- **Medical Equipment**
- **Notebook Computers**
- **Battery-Powered Systems**

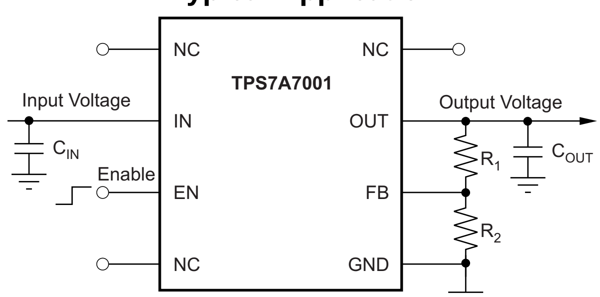
DESCRIPTION

The TPS7A7001 is a high-performance, positive-voltage, low-dropout (LDO) regulator designed for use in applications requiring very low input voltage and very low dropout voltage at up to 2 A. The device operates with a single input voltage as low as 1.425 V, and with an output voltage programmable to as low as 0.5 V. The output voltage can be set using an external divider.

The TPS7A7001 features ultralow dropout, ideal for applications where V_{OUT} is very close to V_{IN}. Additionally, the TPS7A7001 has an enable pin for further reduced power dissipation while in Shutdown mode. The TPS7A7001 provides excellent regulation over variations in line, load, and temperature.

The TPS7A7001 is available in an SOIC-8 PowerPAD™ package.

Typical Application



$$V_{OUT} = 0.5 \times \left(1 + \frac{R_1}{R_2}\right)$$

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION[1]

PRODUCT	V_{OUT}
TPS7A7001***yyyz***	**YYY** is package designator. **Z** is package quantity.

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS[1]

Over operating free-air temperature range (unless otherwise noted).

		VALUE		UNIT
		MIN	MAX	
Voltage	IN, OUT	–0.3	+7.0	V
	EN, FB	–0.3	V_{IN} + 0.3[2]	V
Current	OUT	Internally limited		A
Temperature	Operating virtual junction, T_J	–55	+150	°C
	Storage, T_{stg}	–55	+150	°C
Electrostatic discharge rating[3]	Human body model (HBM, JESD22-A114A)		2	kV
	Charged device model (CDM, JESD22-C101B.01)		500	V

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The absolute maximum rating is V_{IN} + 0.3 V or +7.0 V, whichever is smaller.
(3) ESD testing is performed according to the respective JESD22 JEDEC standard.

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Input voltage	1.425		6.5	V
Ambient temperature range	–40		+105	°C
Junction temperature range	–40		+125	°C
Maximum output current			2	A

THERMAL INFORMATION

THERMAL METRIC[1][2]		TPS7A7001[3] DDA (SOIC) 8 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance[4]	46.4	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance[5]	54.2	
θ_{JB}	Junction-to-board thermal resistance[6]	29.9	
ψ_{JT}	Junction-to-top characterization parameter[7]	10.2	
ψ_{JB}	Junction-to-board characterization parameter[8]	29.8	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance[9]	6.8	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953A.
(2) For thermal estimates of this device based on PCB copper area, see the TI PCB Thermal Calculator.
(3) Thermal data for the DDA package is derived by thermal simulations based on JEDEC-standard methodology as specified in the JESD51 series. The following assumptions are used in the simulations:
(a) DDA: The exposed pad is connected to the PCB ground layer through a 3x2 thermal via array.
(b) DDA: The top and bottom copper layers are assumed to have a 5% thermal conductivity of copper representing a 5% copper coverage.
(c) These data were generated with only a single device at the center of a JEDEC high-K (2s2p) board with 3in × 3in copper area.
(4) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(5) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the top of the package. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(6) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(7) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data to obtain θ_{JA} using a procedure described in JESD51-2a (sections 6 and 7).
(8) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data to obtain θ_{JA} using a procedure described in JESD51-2a (sections 6 and 7).
(9) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

ELECTRICAL CHARACTERISTICS

Over the full operating temperature range (see Recommended Operating Conditions), V_{EN} = 1.1 V, V_{FB} = V_{OUT} [(1)], 1.425 V ≤ V_{IN} ≤ 6.5 V, 10 µA ≤ I_{OUT} ≤ 2 A, C_{OUT} = 10 µF, unless otherwise noted. Typical values are at T_J = +25°C

PARAMETER		TEST CONDITIONS	TPS7A7001 MIN	TPS7A7001 TYP	TPS7A7001 MAX	UNIT
INPUT VOLTAGE						
I_{GND}	GND pin current (small)	V_{IN} = 3.3 V, 50-Ω load resistor between OUT and GND			3	mA
I_{GND}	GND pin current (shutdown)	V_{IN} = 6.5 V, V_{EN} = 0 V			5	µA
OUTPUT VOLTAGE						
V_{OUT}	Output voltage accuracy [(2)(3)]	V_{IN} = V_{OUT} + 0.5 V [(4)], I_{OUT} = 10 mA	–2.0		+2.0	%
		V_{IN} = 1.8 V, I_{OUT} = 0.8 A, 0°C ≤ T_J = T_A ≤ +85°C				
		I_{OUT} = 10 mA	–3.0		+3.0	
$ΔV_{O(ΔVI)}$	Line regulation	I_{OUT} = 10 mA		0.2	0.4	%/V
$ΔV_{O(ΔIO)}$	Load regulation [(3)]	10 mA ≤ I_{OUT} ≤ 2 A		0.25	0.75	%/A
V_{DO}	Dropout voltage [(5)]	I_{OUT} = 1.0 A, 0.5 V ≤ V_{OUT} ≤ 5.0 V			200	mV
		I_{OUT} = 1.5 A, 0.5 V ≤ V_{OUT} ≤ 5.0 V			300	
		I_{OUT} = 2.0 A, 0.5 V ≤ V_{OUT} ≤ 5.0 V			380	
I_{LIM}	Output current limit	V_{IN} = 1.425 V, V_{OUT} = 0.9 × $V_{OUT(NOM)}$	2.1		4.4	A
FEEDBACK						
V_{REF}	Reference voltage accuracy	V_{IN} = 3.3 V, V_{FB} = V_{OUT}, I_{OUT} = 10 mA	0.490	0.500	0.510	V
I_{FB}	FB pin current	V_{FB} = 0.5 V			1	µA
ENABLE						
I_{EN}	EN pin current	V_{EN} = 0 V, V_{IN} = 3.3 V			0.2	µA
VIL_{EN}	EN pin input low (disable)	V_{IN} = 3.3 V	0		0.5	V
VIH_{EN}	EN pin input high (enable)	V_{IN} = 3.3 V	1.1		V_{IN}	V
TEMPERATURE						
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing		+160		°C
		Reset, temperature decreasing		+140		°C

(1) When setting V_{OUT} to a value other than 0.5 V, connect R_1 and R_2 to the FB pin using 10 kΩ ≤ R_2 ≤ 50 kΩ resistors. See Figure 1 for details of R_1 and R_2.
(2) Accuracy does not include error on feedback resistors R_1 and R_2.
(3) TPS7A7001 is not tested at V_{OUT} = 0.5 V, 2.3 V ≤ V_{IN} ≤ 6.5 V, and 500 mA ≤ I_{OUT} ≤ 2 A because the power dissipation is higher than the maximum rating of the package. Also, this accuracy specification does not apply to any application condition that exceeds the power dissipation limit of the package.
(4) V_{IN} = V_{OUT} + 0.5 V or 1.425 V, whichever is greater.
(5) V_{DO} = V_{IN} - V_{OUT} with V_{FB} = GND configuration.

FUNCTIONAL BLOCK DIAGRAM

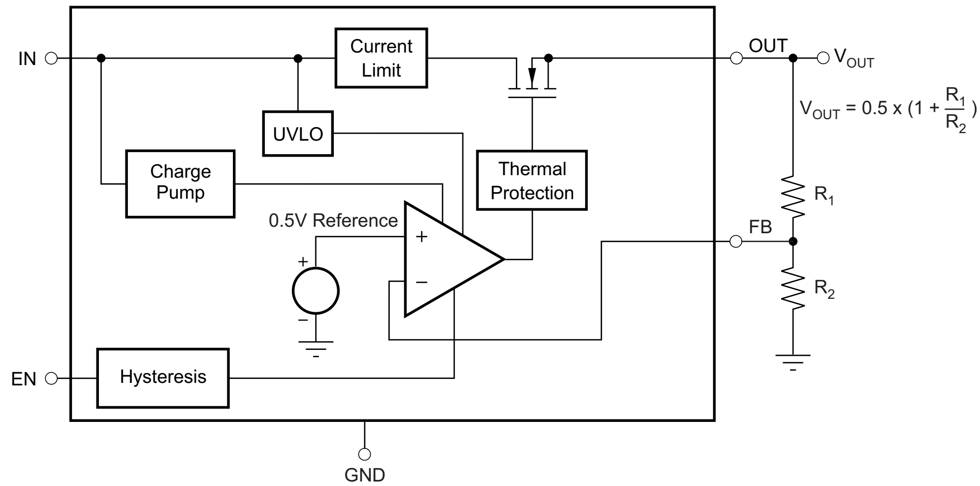
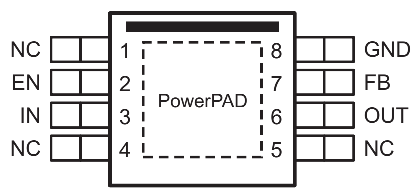


Figure 1. Adjustable Output Voltage Version

PIN CONFIGURATIONS

DDA PACKAGE
SOIC-8
(TOP VIEW)



Pin Descriptions

NAME	PIN #	DESCRIPTION
EN	2	Enable input. Pulling this pin below 0.5 V turns the regulator off. Connect to V_{IN} if not being used.
FB	7	This pin is the output voltage feedback input through voltage dividers. See the recommended feedback resistor table for more details.
GND	8	Ground pin
IN	3	Unregulated supply voltage pin. It is recommended to connect an input capacitor to this pin.
NC	1, 4, 5	Not internally connected. The NC pins are not connected to any electrical node. It is recommended to connect the NC pins to large-area planes.
OUT	6	Regulated output pin. A 4.7-μF or larger capacitor of any type is required for stability.
PowerPAD		It is strongly recommended to connect the thermal pad to a large-area ground plane. If an electrically floating, dedicated thermal plane is available, the thermal pad can also be connected to it.

TYPICAL CHARACTERISTICS

For all fixed voltage versions and an adjustable version at T_J = +25°C, V_{EN} = V_{IN}, C_{IN} = 10 μF, C_{OUT} = 10 μF, and using the component values in Table 1, unless otherwise noted.

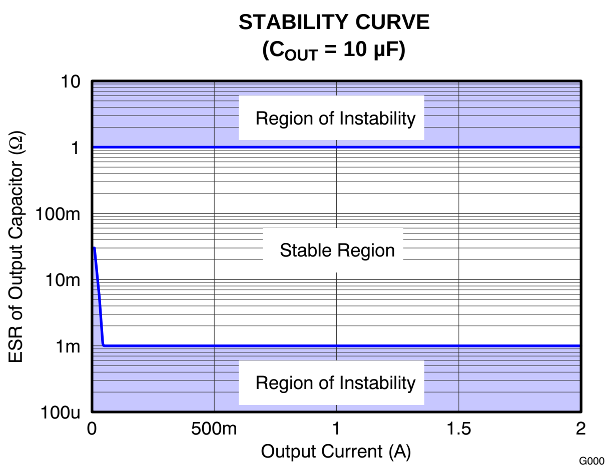


Figure 2.

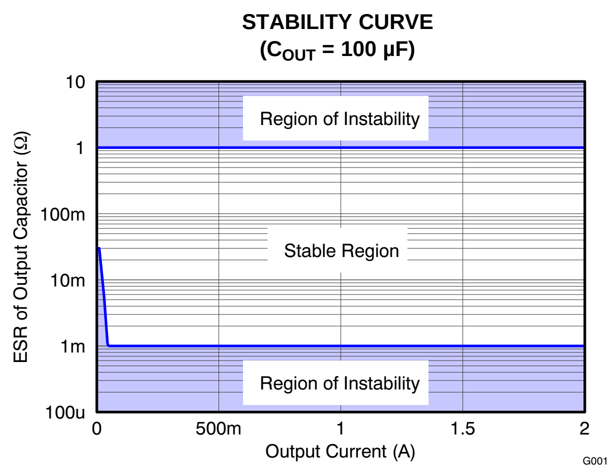


Figure 3.

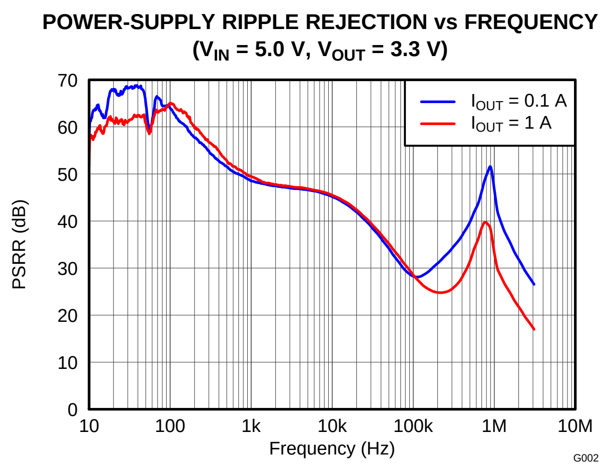


Figure 4.

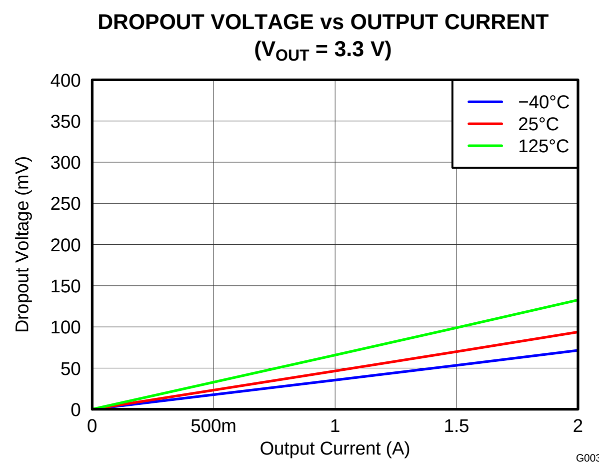


Figure 5.

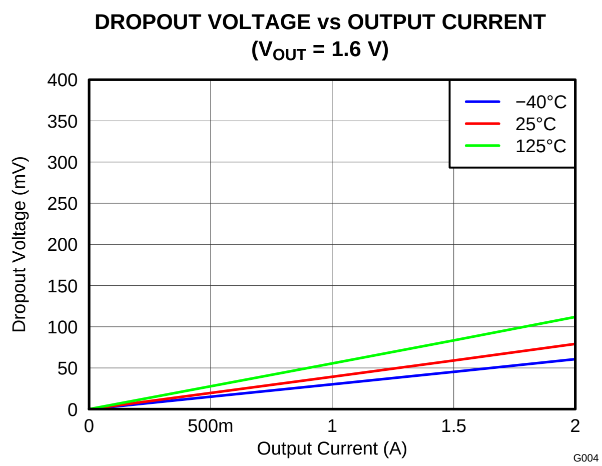


Figure 6.

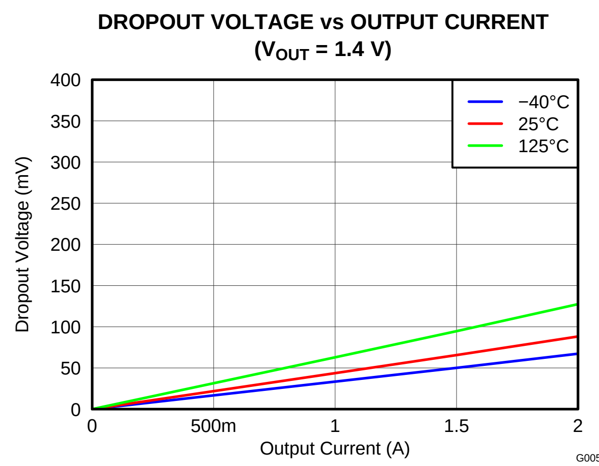


Figure 7.

APPLICATION INFORMATION

OVERVIEW

The TPS7A7001 offers a high current supply with very low dropout voltage. The TPS7A7001 is designed to minimize the required component count for a simple, small-size, and low-cost solution.

INPUT CAPACITOR (IN)

Although an input capacitor is not required for stability, it is recommended to connect a 1-µF to 10-µF low equivalent series resistance (ESR) capacitor across IN and GND near the device.

OUTPUT CAPACITOR (OUT)

The device is designed to be stable with output capacitance 4.7 µF or larger. For a good load transient response, a 10-µF or larger ceramic capacitor is recommended. Connect the output capacitor across OUT and GND near the device.

FEEDBACK RESISTORS (FB)

The voltage on the FB pin sets the output voltage and is determined by the values of R_1 and R_2. The values of R_1 and R_2 can be calculated for any voltage using the formula given in Equation 1:

$$V_{OUT} = \frac{(R_1 + R_2)}{R_2} \times 0.500 \quad (1)$$

Table 1 shows the recommended resistor values for the best performance of the TPS7A7001. In Table 1, E96 series resistors are used. For the actual design, pay attention to any resistor error factors.

Table 1. Sample Resistor Values for Common Output Voltages

V_{OUT}	R_1	R_2
1.0 V	30.1 kΩ	30.1 kΩ
1.2 V	42.2 kΩ	30.1 kΩ
1.5 V	60.4 kΩ	30.1 kΩ
1.8 V	78.7 kΩ	30.1 kΩ
2.5 V	121 kΩ	30.1 kΩ
3.0 V	150 kΩ	30.1 kΩ
3.3 V	169 kΩ	30.1 kΩ
5.0 V	274 kΩ	30.1 kΩ

ENABLE (EN)

The enable pin (EN) is an active high logic input. When it is logic low, the device turns off and its consumption current is less than 1 µA. When it is logic high, the device turns on. The EN pin is required to be connected to a logic high or logic low level.

When the enable function is not required, connect EN to VIN.

INTERNAL CURRENT LIMIT

The TPS7A7001 internal current limit helps protect the regulator during fault conditions. During current limit, the output sources a fixed amount of current that is largely independent of output voltage. For reliable operation, the device should not be operated in a current limit state for extended periods of time.

THERMAL INFORMATION

Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately +160°C, allowing the device to cool. When the junction temperature cools to approximately +140°C, the output circuitry is enabled again.

The internal protection circuitry of the TPS7A7001 is designed to protect against overload conditions. It is not intended to replace proper heatsinking. Continuously running the TPS7A7001 into thermal shutdown degrades device reliability.

Power Dissipation

Power dissipation of the device depends on the input voltage and load conditions and can be calculated using Equation 2:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (2)$$

Power dissipation can be minimized and greater efficiency can be achieved by using the lowest possible input voltage necessary to achieve the required output voltage regulation.

On the SOIC (DDA) package, the primary conduction path for heat is through the exposed pad to the printed circuit board (PCB). The pad can be connected to ground or left floating; however, it should be attached to an appropriate amount of copper PCB area to ensure the device does not overheat. The maximum junction-to-ambient thermal resistance depends on the maximum ambient temperature, maximum device junction temperature, and power dissipation of the device and can be calculated using Equation 3:

$$R_{\theta JA} = \left(\frac{+125°C - T_A}{P_D} \right) \quad (3)$$

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (June 2012) to Revision B **Page**

Changes from Original (January 2012) to Revision A **Page**

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TPS7A7001DDA	ACTIVE	SO PowerPAD	DDA	8	75	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	QVH	Samples
TPS7A7001DDAR	ACTIVE	SO PowerPAD	DDA	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	QVH	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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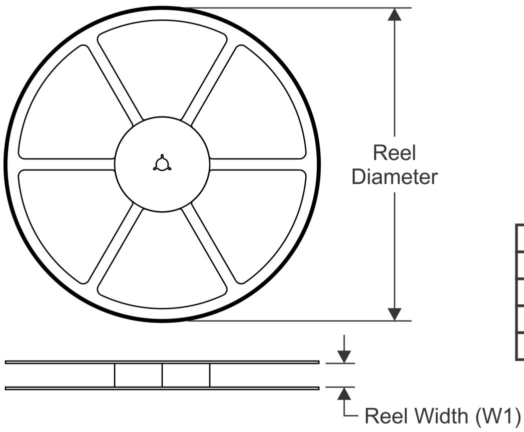
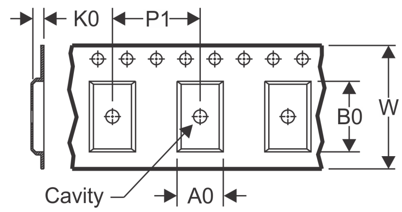
TAPE AND REEL INFORMATION

REEL DIMENSIONS

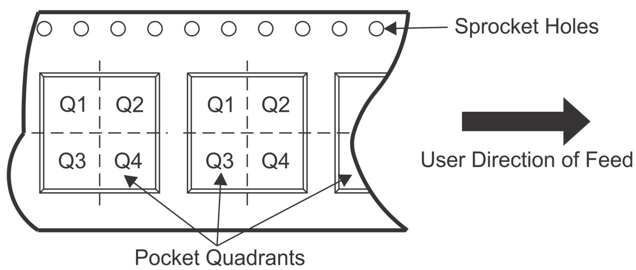


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

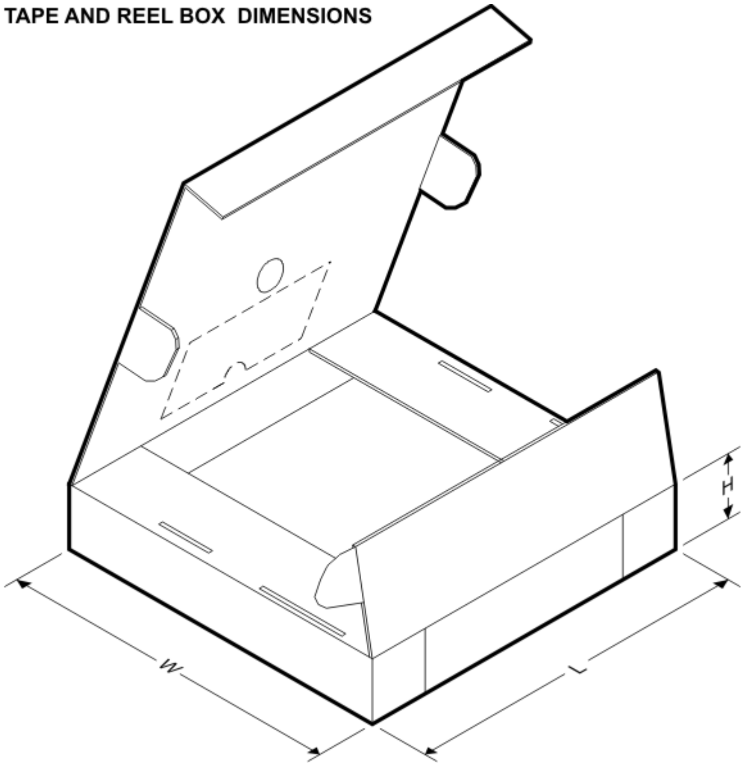
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7A7001DDAR	SO Power PAD	DDA	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1

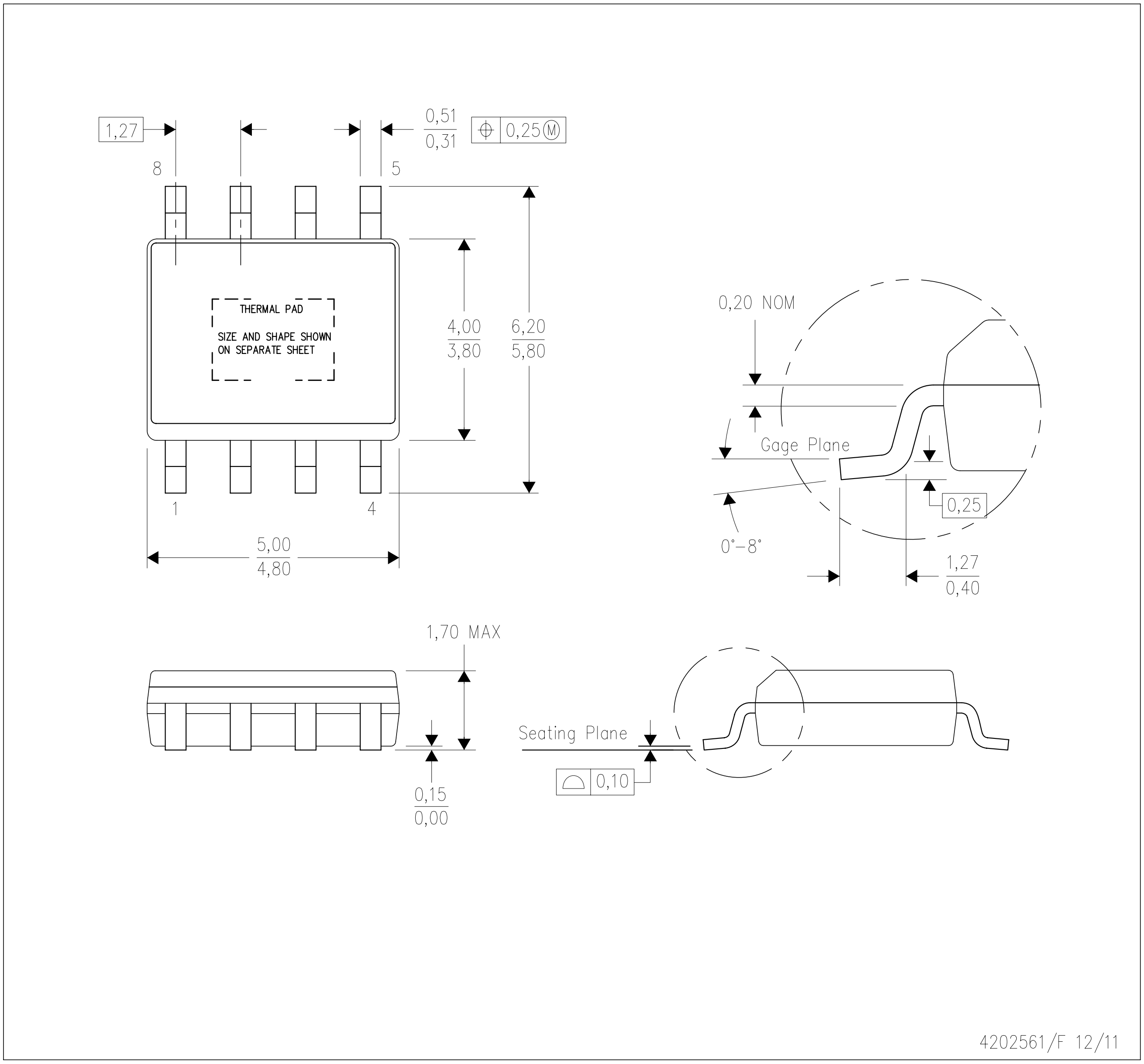
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7A7001DDAR	SO PowerPAD	DDA	8	2500	366.0	364.0	50.0

DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL–OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http: //www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. This package complies to JEDEC MS–012 variation BA

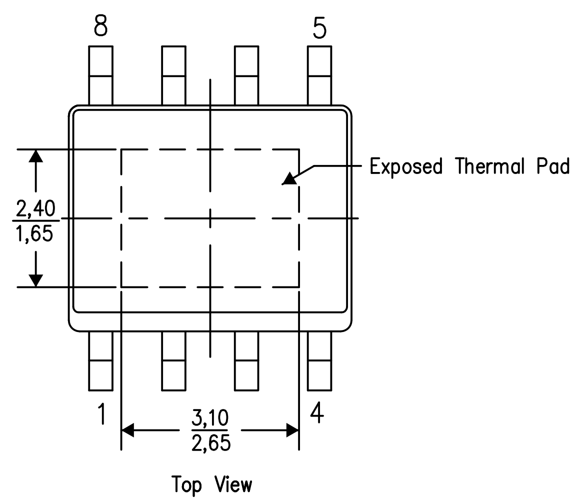
DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

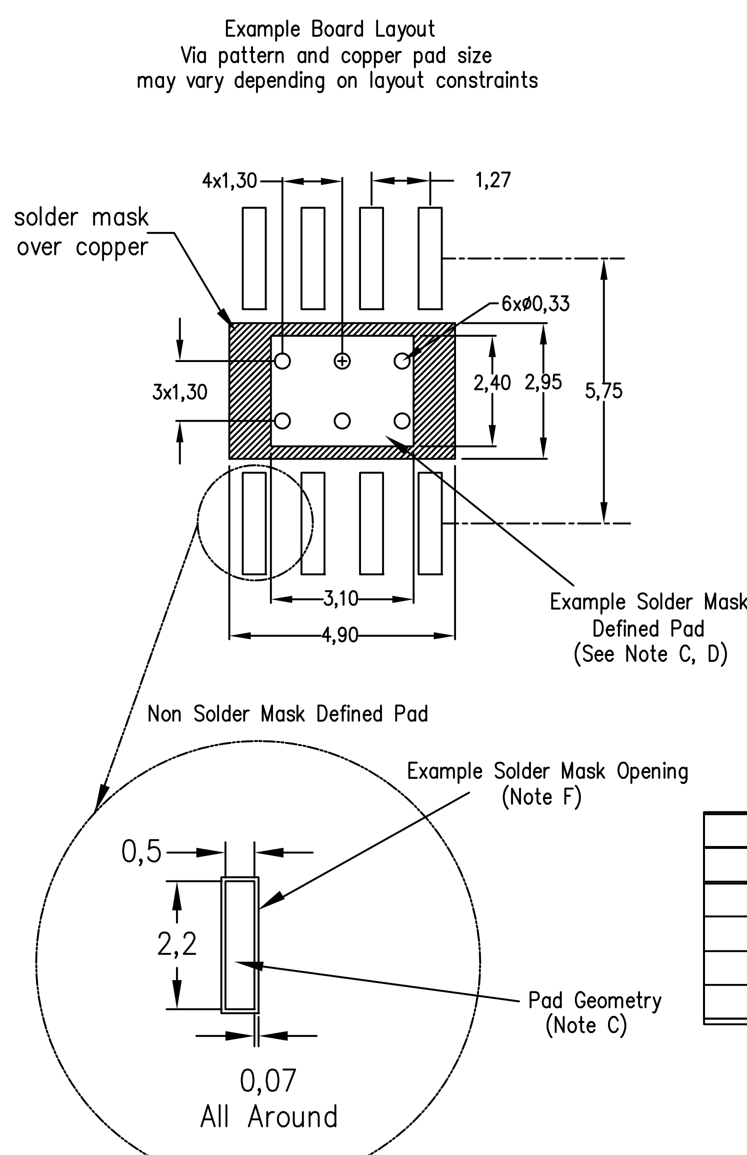


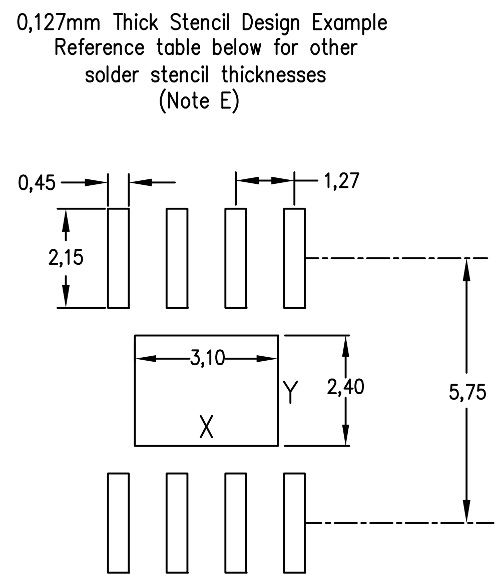
Exposed Thermal Pad Dimensions

4206322-6/L 05/12

NOTE: A. All linear dimensions are in millimeters

DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE





Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.3	2.6
0.127mm	3.1	2.4
0.152mm	2.9	2.2
0.178mm	2.8	2.1

4208951–6/D 04/12

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
- F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265