28-BIT TO 56-BIT REGISTERED BUFFER WITH ADDRESS-PARITY TEST

FEATURES

- Member of the Texas Instruments Widebus+ ™Family
- Pinout Optimizes DDR2 DIMM PCB Layout
- 1-to-2 Outputs Supports Stacked DDR2 DIMMs
- One Device Per DIMM Required
- Chip-Select Inputs Gate the Data Outputs from Changing State and Minimizes System Power Consumption
- Output Edge-Control Circuitry Minimizes Switching Noise in an Unterminated Line
- Supports SSTL_18 Data Inputs
- Differential Clock (CLK and $\overline{\text{CLK}}$) Inputs
- Supports LVCMOS Switching Levels on the Chip-Select Gate-Enable, Control, and $\overline{\text{RESET}}$ Inputs
- Checks Parity on DIMM-Independent Data Inputs
- Supports Industrial Temperature Range (-40°C to 85°C)
- $\overline{\text{RESET}}$ Input Disables Differential Input Receivers, Resets All Registers, and Forces All Outputs Low, Except $\overline{\text{QERR}}$

APPLICATIONS

- DDR2 registered DIMM

DESCRIPTION

This 28-bit 1:2 configurable registered buffer is designed for 1.7-V to 1.9-V V_{CC} operation. One device per DIMM is required to drive up to 18 SDRAM loads or two devices per DIMM are required to drive up to 36 SDRAM loads.

All inputs are SSTL_18, except the chip-select gate-enable (CSGEN), control (C), and reset ($\overline{\text{RESET}}$) inputs, which are LVCMOS. All outputs are edge-controlled circuits optimized for unterminated DIMM loads, and meet SSTL_18 specifications, except the open-drain error ($\overline{\text{QERR}}$) output.

The 74SSTUB32868 operates from a differential clock (CLK and CLK). Data are registered at the crossing of CLK going high and CLK going low.

The 74SSTUB32868 accepts a parity bit from the memory controller on the parity bit (PAR_IN) input, compares it with the data received on the DIMM-independent D-inputs (D1−D5, D7, D9−D12, D17−D28 when C = 0; or D1−D12, D17−D20, D22, D24−D28 when C = 1) and indicates whether a parity error has occurred on the open-drain $\overline{\text{QERR}}$ pin (active low). The convention is even parity, i.e., valid parity is defined as an even number of ones across the DIMM-independent data inputs combined with the parity input bit. To calculate parity, all DIMM-independent D-inputs must be tied to a known logic state.

The 74SSTUB32868 includes a parity checking function. Parity, which arrives one cycle after the data input to which it applies, is checked on the PAR_IN input of the device. Two clock cycles after the data are registered, the corresponding QERR signal is generated.

ORDERING INFORMATION

T_A	PACKAGE(1)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	TFBGA-ZRH	Tape and Reel	74SSTUB32868ZRHR	SB868

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION (CONTINUED)

If an error occurs and the QERR output is driven low, it stays latched low for a minimum of two clock cycles or until RESET is driven low. If two or more consecutive parity errors occur, the QERR output is driven low and latched low for a clock duration equal to the parity error duration or until RESET is driven low. If a parity error occurs on the clock cycle before the device enters the low−power mode (LPM) and the QERR output is driven low, it stays latched low for the LPM duration plus two clock cycles or until RESET is driven low. The DIMM-dependent signals (DCKE0, DCKE1, DODT0, DODT1, DCS0 and DCS1) are not included in the parity check computation.

The C input controls the pinout configuration from register-A configuration (when low) to register-B configuration (when high). The C input should not be switched during normal operation. It should be hard-wired to a valid low or high level to configure the register in the desired mode.

In the DDR2 RDIMM application, RESET is specified to be completely asynchronous with respect to CLK and CLK. Therefore, no timing relationship can be ensured between the two. When entering reset, the register is cleared and the data outputs is driven low quickly, relative to the time to disable the differential input receivers. However, when coming out of reset, the register becomes active quickly, relative to the time to enable the differential input receivers. As long as the data inputs are low, and the clock is stable during the time from the low-to-high transition of RESET until the input receivers are fully enabled, the design of the 74SSTUB32868 must ensure that the outputs remain low, thus ensuring no glitches on the output.

To ensure defined outputs from the register before a stable clock has been supplied, RESET must be held in the low state during power up.

The device supports low-power standby operation. When RESET is low, the differential input receivers are disabled, and undriven (floating) data, clock, and reference voltage (V_{REF}) inputs are allowed. In addition, when RESET is low, all registers are reset and all outputs are forced low except QERR. The LVCMOS RESET and C inputs always must be held at a valid logic high or low level.

The device also supports low-power active operation by monitoring both system chip select (DCS0 and DCS1) and CSGEN inputs and will gate the Qn outputs from changing states when CSGEN, DCS0, and DCS1 inputs are high. If CSGEN, DCS0 or DCS1 input is low, the Qn outputs function normally. Also, if both DCS0 and DCS1 inputs are high, the device will gate the QERR output from changing states. If either DCS0 or DCS1 is low, the QERR output functions normally. The RESET input has priority over the DCS0 and DCS1 control and when driven low forces the Qn outputs low, and the QERR output high. If the chip-select control functionality is not desired, then the CSGEN input can be hard-wired to ground, in which case, the setup-time requirement for DCS0 and DCS1 would be the same as for the other D data inputs. To control the low-power mode with DCS0 and DCS1 only, then the CSGEN input should be pulled up to V_{CC} through a pullup resistor.

The two V_{REF} pins (A5 and AB5) are connected together internally by approximately 150 Ω. However, it is necessary to connect only one of the two V_{REF} pins to the external V_{REF} power supply. An unused V_{REF} pin should be terminated with a V_{REF} coupling capacitor.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)[1]

			VALUE	UNIT
V_{CC}	Supply voltage range		–0.5 to 2.5	V
V_I	Input voltage range (see notes [2] and [3])		–0.5 to V_{CC} + 0.5	V
V_O	Output voltage range (see notes [2] and [3])		–0.5 to V_{CC} + 0.5	V
I_{IK}	Input clamp current (V_I < 0, V_I > V_{CC})		±50	mA
I_{OK}	Output clamp current (V_I < 0, V_O > V_{CC})		±50	mA
I_O	Continuous output current (V_O = 0 to V_{CC})		±50	mA
I_{CC}	Continuous current through each V_{CC} or GND		±100	mA
$R_{\theta JA}$	Thermal resistance, junction−to−ambient (see note [4])	No airflow	46.8	k/W
		Airflow 200 ft/min	42.9	
$R_{\theta JC}$	Thermal resistance, junction−to−case (see note [4])	No airflow	17.9	
T_{stg}	Storage temperature range		-65 to 150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(3) This value is limited to 2.5 V maximum.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted) [1]

			MIN	NOM	MAX	UNIT
SUPPLY VOLTAGES, CURRENTS AND TEMPERATURE RANGE						
V_{CC}	Supply voltage		1.7		1.9	V
V_{REF}	Reference voltage		0.49 x V_{CC}	0.5 x V_{CC}	0.51 x V_{CC}	V
V_{TT}	Termination voltage		V_{REF} - 40 mV	V_{REF}	V_{REF} + 40 mV	V
V_I	Input voltage		0		V_{CC}	V
V_{IH}	AC high-level input voltage	Data inputs, $\overline{DCSn}$, PAR_IN	V_{REF} + 250 mV			V
V_{IL}	AC low-level input voltage	Data inputs, $\overline{DCSn}$, PAR_IN			V_{REF} - 250 mV	V
V_{IH}	DC high-level input voltage	Data inputs, $\overline{DCSn}$, PAR_IN	V_{REF} + 125 mV			V
V_{IL}	DC low-level input voltage	Data inputs, $\overline{DCSn}$, PAR_IN			V_{REF} - 125 mV	V
V_{IH}	High-level input voltage	$\overline{RESET}$, CSGEN, C	0.65 x V_{CC}			V
V_{IL}	Low-level input voltage	$\overline{RESET}$, CSGEN, C			0.35 x V_{CC}	V
V_{ICR}	Common-mode input voltage range	CLK, $\overline{CLK}$	0.675		1.125	V
$V_{I(PP)}$	Peak-to-peak input voltage	CLK, $\overline{CLK}$	0.6			V
I_{OH}	High-level output current	Q outputs			-8	mA
I_{OL}	Low-level output current	Q outputs			8	mA
		$\overline{QERR}$ output	30			
T_A	Operating free-air temperature		-40		85	°C

(1) The $\overline{RESET}$ and Cn inputs of the device must be held at valid logic voltage levels (not floating) to ensure proper device operation. The differential inputs must not be floating unless $\overline{RESET}$ is low. See the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

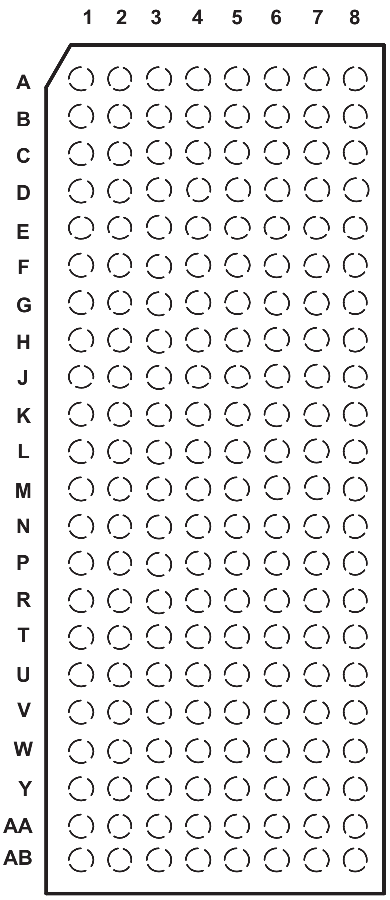
ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITION		V_{CC}	MIN	TYP[1]	MAX	UNIT
V_{OH}	Q outputs	I_{OH} = -100 µA		1.7 V to 1.9 V	V_{CC} - 0.2			V
		I_{OH} = -6 mA		1.7 V	1.2			
V_{OL}	Q outputs	I_{OL} = 100 µA		1.7 V to 1.9 V			0.2	V
		I_{OL} = 6 mA		1.7 V			0.5	
	$\overline{\text{QERR}}$	I_{OL} = 25 mA		1.7 V			0.5	
I_I	PAR_IN	V_I = GND		1.9 V			-5	µA
		$V_I = V_{CC}$					25	
	All other inputs[2]	$V_I = V_{CC}$ or GND					±5	
I_{OZ}	$\overline{\text{QERR}}$ outputs	$V_O = V_{CC}$ or GND		1.9 V			±10	µA
I_{CC}	Static standby[3]	$\overline{\text{RESET}}$ = GND	$I_O = 0$	1.9 V			200 [3]	µA
	Static operating	$\overline{\text{RESET}} = V_{CC}$, VI = $V_{IH(AC)}$ or $V_{IL(AC)}$					80	mA
$I_{CC(D)}$	Dynamic operating – clock only	$\overline{\text{RESET}} = V_{CC}$, $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$, CLK and $\overline{\text{CLK}}$ switching 50% duty cycle	$I_O = 0$	1.8 V		64		µA/MHz
	Dynamic operating – per each data input	$\overline{\text{RESET}} = V_{CC}$, $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$, CLK and $\overline{\text{CLK}}$ switching 50% duty cycle, One data input switching at one half clock frequency, 50% duty cycle				37		µA/clock MHz/ D inputs
$I_{CC(DLP)}$	Chip-select-enabled low-power active mode – clock only	$\overline{\text{RESET}} = V_{CC}$, $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$, CLK and $\overline{\text{CLK}}$ switching 50% duty cycle	$I_O = 0$	1.8 V		68		µA/MHz
	Chip-select-enabled low-power active mode	$\overline{\text{RESET}} = V_{CC}$, $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$, CLK and $\overline{\text{CLK}}$ switching 50% duty cycle, One data input switching at one half clock frequency, 50% duty cycle				2.7		µA/clock MHz/ D inputs
C_I	Data inputs, DCSn, PAR_IN, CSGEN	$V_I = V_{REF}$ ±250 mV		1.8 V	2	2.5	3	pF
	CLK, $\overline{\text{CLK}}$	V_{ICR} = 0.9 V, $V_{I(PP)}$ = 600 mV			2		3	
	$\overline{\text{RESET}}$	$V_I = V_{CC}$ or GND				4		

(1) All typical values are at V_{CC} = 1.8 V, T_A = 25°C.
(2) Each V_{REF} pin (A5 or AB5) should be tested independently, with the other (untested) pin open.
(3) The maximum static standby current I_{CC} is 100 µA if the device is exposed to commercial temperature range (0°C to 70°C) only. For industrial temperature range (-40°C to 85°C), the static I_{CC} is 200 µA.

PACKAGE
(TOP VIEW)



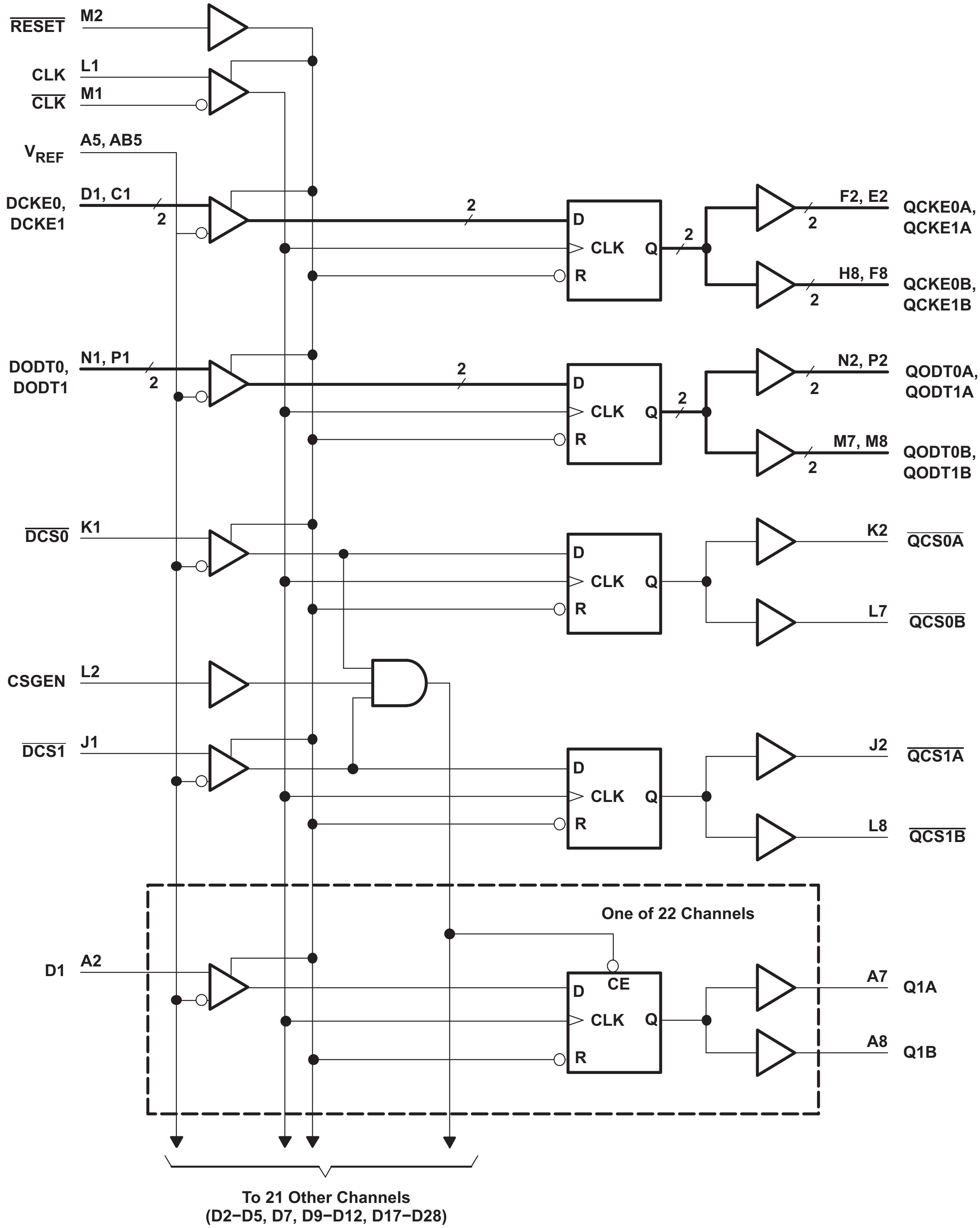
Terminal Assignment for Register-A (C = 0)

	1	2	3	4	5	6	7	8
A	D2	D1	C	GND	V_{REF}	GND	Q1A	Q1B
B	D4	D3	V_{CC}	V_{CC}	V_{CC}	V_{CC}	Q2A	Q2B
C	D6 (DCKE1)	D5	GND	GND	GND	GND	Q3A	Q3B
D	D8 (DCKE0)	D7	V_{CC}	V_{CC}	V_{CC}	V_{CC}	Q4A	Q4B
E	D9	Q6A (QCKE1A)	GND	GND	GND	GND	Q5A	Q5B
F	D10	Q8A (QCKE0A)	V_{CC}	V_{CC}	V_{CC}	V_{CC}	Q7A	Q6B (QCKE1B)
G	D11	Q10A	GND	GND	GND	GND	Q9A	Q7B
H	D12	Q12A	V_{CC}	V_{CC}	V_{CC}	V_{CC}	Q11A	Q8B (QCKE0B)
J	D13 ($\overline{\text{DCS1}}$)	Q13A ($\overline{\text{QCS1A}}$)	GND	GND	GND	GND	Q10B	Q9B
K	D14 ($\overline{\text{DCS0}}$)	Q14A ($\overline{\text{QCS0A}}$)	V_{CC}	V_{CC}	V_{CC}	V_{CC}	Q12B	Q11B
L	CLK	CSGEN	PAR_IN	GND	GND	GND	Q14B ($\overline{\text{QCS0B}}$)	Q13B ($\overline{\text{QCS1B}}$)
M	$\overline{\text{CLK}}$	$\overline{\text{RESET}}$	$\overline{\text{QERR}}$	V_{CC}	V_{CC}	V_{CC}	Q15B (QODT0B)	Q16B (QODT1B)
N	D15 (DODT0)	Q15A (QODT0A)	GND	GND	GND	GND	Q17B	Q18B
P	D16 (DODT1)	Q16A (QODT1A)	V_{CC}	V_{CC}	V_{CC}	V_{CC}	Q19B	Q20B
R	D17	Q17A	GND	GND	GND	GND	Q18A	Q21B
T	D18	Q19A	V_{CC}	V_{CC}	V_{CC}	V_{CC}	Q20A	Q22B
U	D19	Q21A	GND	GND	GND	GND	Q22A	Q23B
V	D20	Q23A	V_{CC}	V_{CC}	V_{CC}	V_{CC}	Q24A	Q24B
W	D21	D22	GND	GND	GND	GND	Q25A	Q25B
Y	D23	D24	V_{CC}	V_{CC}	V_{CC}	V_{CC}	Q26A	Q26B
AA	D25	D26	GND	GND	GND	GND	Q27A	Q27B
AB	D27	D28	NC	V_{CC}	V_{REF}	V_{CC}	Q28A	Q28B

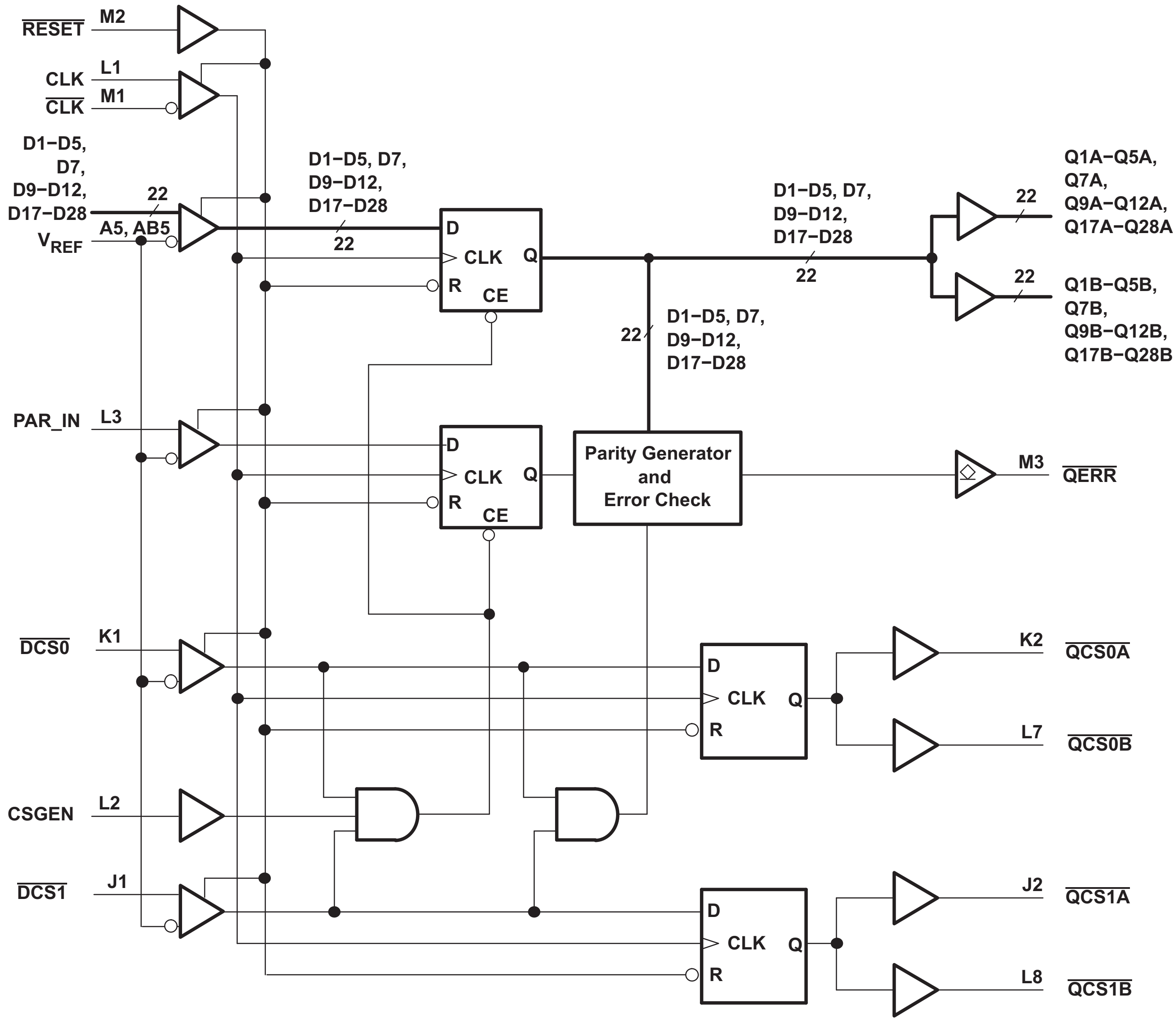
A. Each pin name in parentheses indicates the DDR2 DIMM signal name.

B. NC - No internal connection.

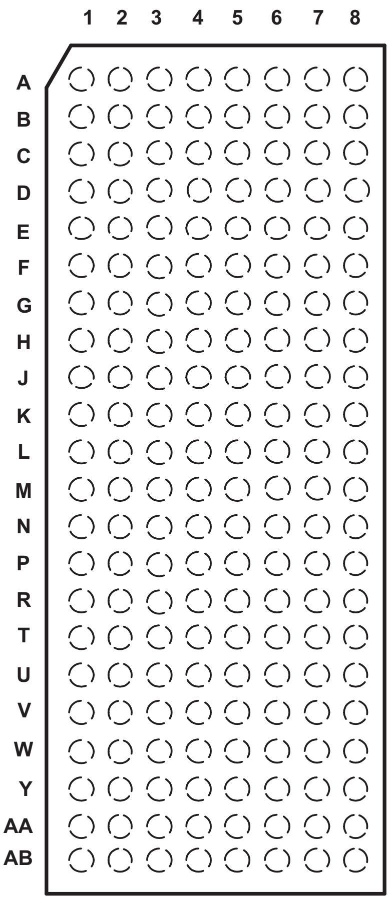
Logic Diagram for Register-A Configuration (Positive Logic); C = 0



Parity Logic Diagram for Register-A Configuration (Positive Logic); C = 0



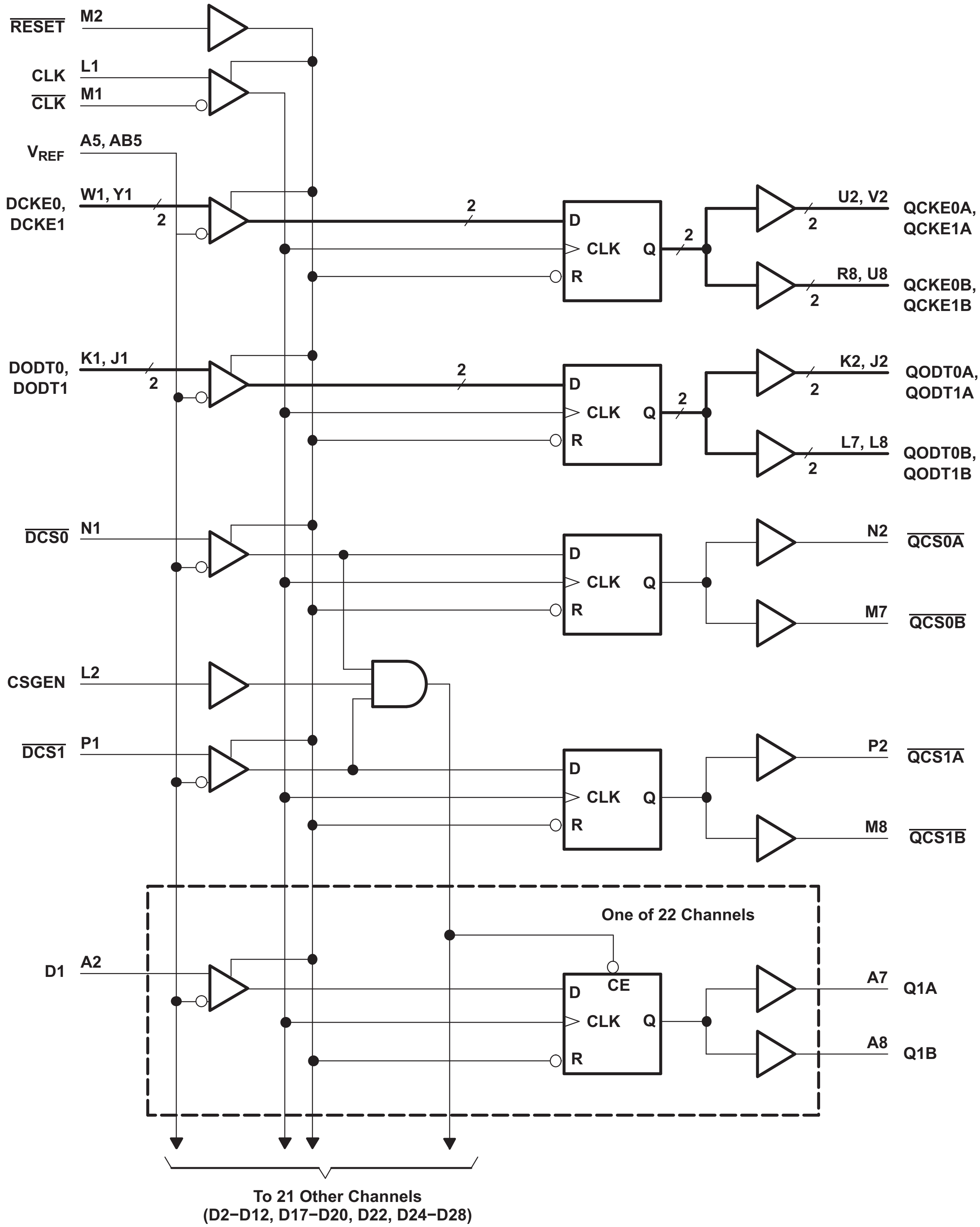
PACKAGE
(TOP VIEW)



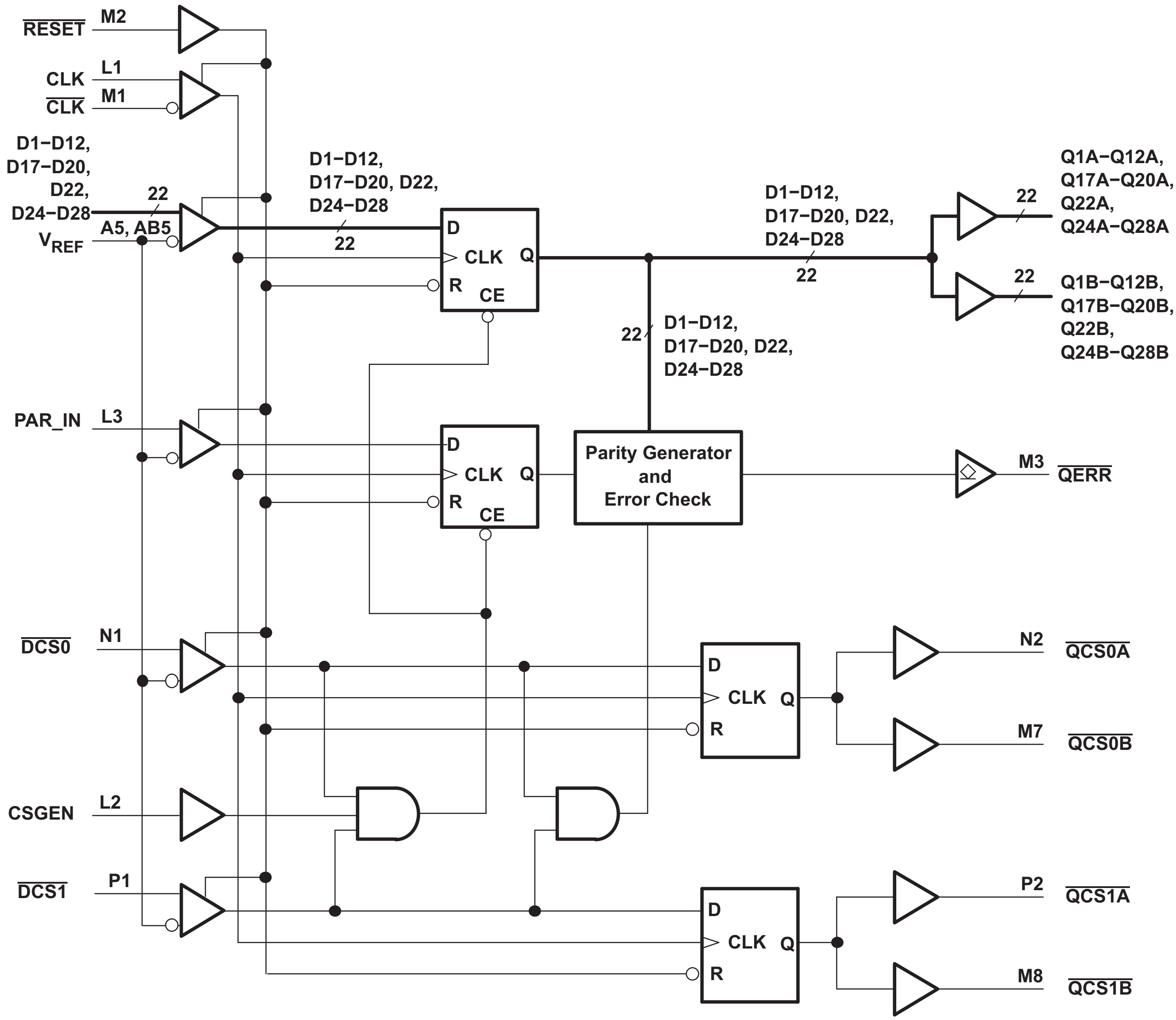
Terminal Assignment for Register-B (C = 1)

	1	2	3	4	5	6	7	8
A	D2	D1	C	GND	V_{REF}	GND	Q1A	Q1B
B	D4	D3	V_{CC}	V_{CC}	V_{CC}	V_{CC}	Q2A	Q2B
C	D6	D5	GND	GND	GND	GND	Q3A	Q3B
D	D8	D7	V_{CC}	V_{CC}	V_{CC}	V_{CC}	Q4A	Q4B
E	D9	Q6A	GND	GND	GND	GND	Q5A	Q5B
F	D10	Q8A	V_{CC}	V_{CC}	V_{CC}	V_{CC}	Q7A	Q6B
G	D11	Q10A	GND	GND	GND	GND	Q9A	Q7B
H	D12	Q12A	V_{CC}	V_{CC}	V_{CC}	V_{CC}	Q11A	Q8B
J	D13 ($\overline{\text{DODT1}}$)	Q13A (DODT1A)	GND	GND	GND	GND	Q10B	Q9B
K	D14 ($\overline{\text{DODT0}}$)	Q14A (QODT0A)	V_{CC}	V_{CC}	V_{CC}	V_{CC}	Q12B	Q11B
L	CLK	CSGEN	PAR_IN	GND	GND	GND	Q14B (QODT0B)	Q13B (QODT1B)
M	$\overline{\text{CLK}}$	$\overline{\text{RESET}}$	$\overline{\text{QERR}}$	V_{CC}	V_{CC}	V_{CC}	Q15B ($\overline{\text{QCS0B}}$)	Q16B ($\overline{\text{QCS1B}}$)
N	D15 ($\overline{\text{DCS0}}$)	Q15A ($\overline{\text{QCS0A}}$)	GND	GND	GND	GND	Q17B	Q18B
P	D16 ($\overline{\text{DCS1}}$)	Q16A ($\overline{\text{QCS1A}}$)	V_{CC}	V_{CC}	V_{CC}	V_{CC}	Q19B	Q20B
R	D17	Q17A	GND	GND	GND	GND	Q18A	Q21B (QCKE0B)
T	D18	Q19A	V_{CC}	V_{CC}	V_{CC}	V_{CC}	Q20A	Q22B
U	D19	Q21A (QCKE0A)	GND	GND	GND	GND	Q22A	Q23B (QCKE1B)
V	D20	Q23A (QCKE1A)	V_{CC}	V_{CC}	V_{CC}	V_{CC}	Q24A	Q24B
W	D21 (DCKE0)	D22	GND	GND	GND	GND	Q25A	Q25B
Y	D23 (DCKE1)	D24	V_{CC}	V_{CC}	V_{CC}	V_{CC}	Q26A	Q26B
AA	D25	D26	GND	GND	GND	GND	Q27A	Q27B
AB	D27	D28	NC	V_{CC}	V_{REF}	V_{CC}	Q28A	Q28B

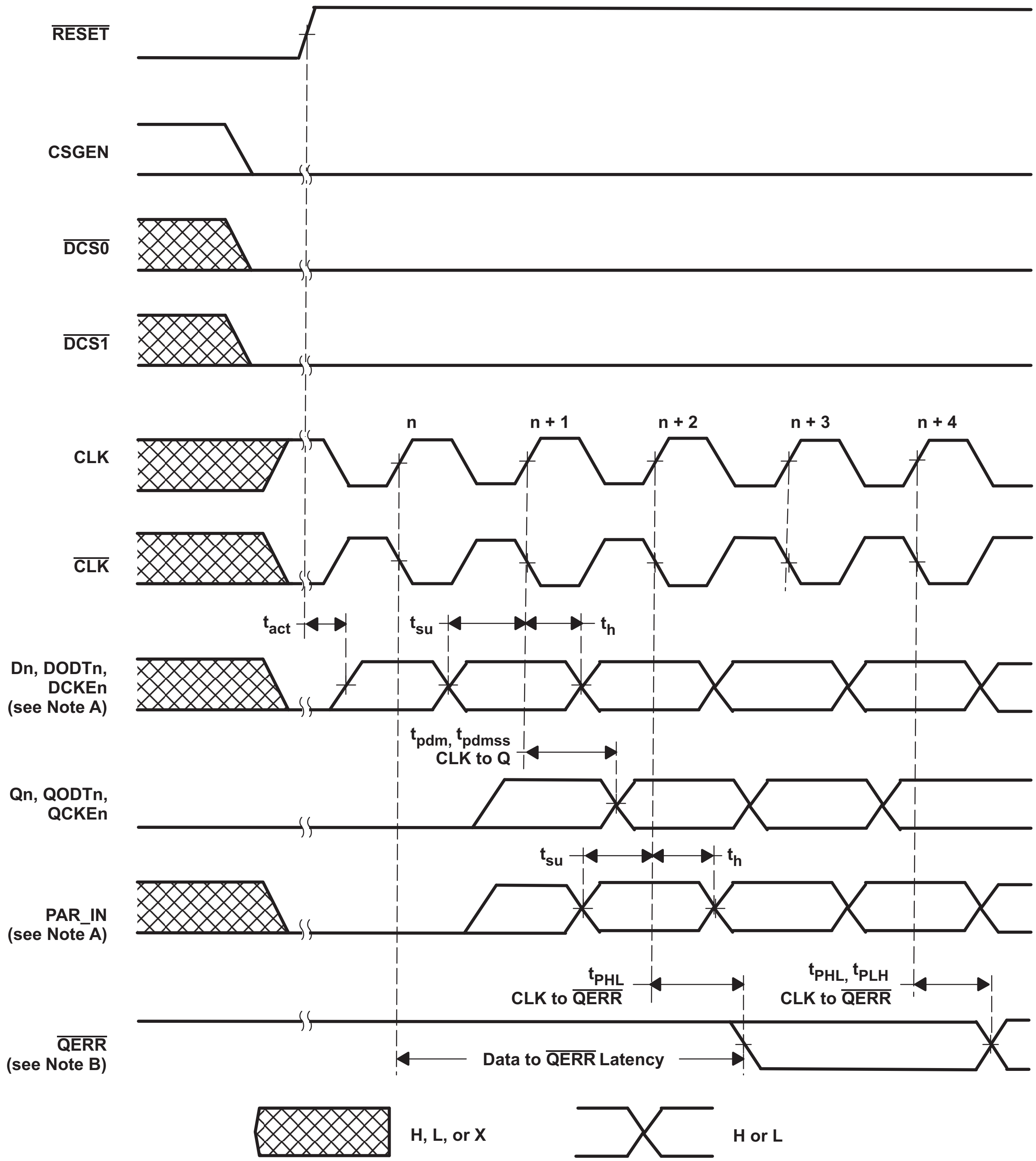
Logic Diagram for Register-B Configuration (Positive Logic); C = 1



Parity Logic Diagram for Register-B Configuration (Positive Logic); C = 1



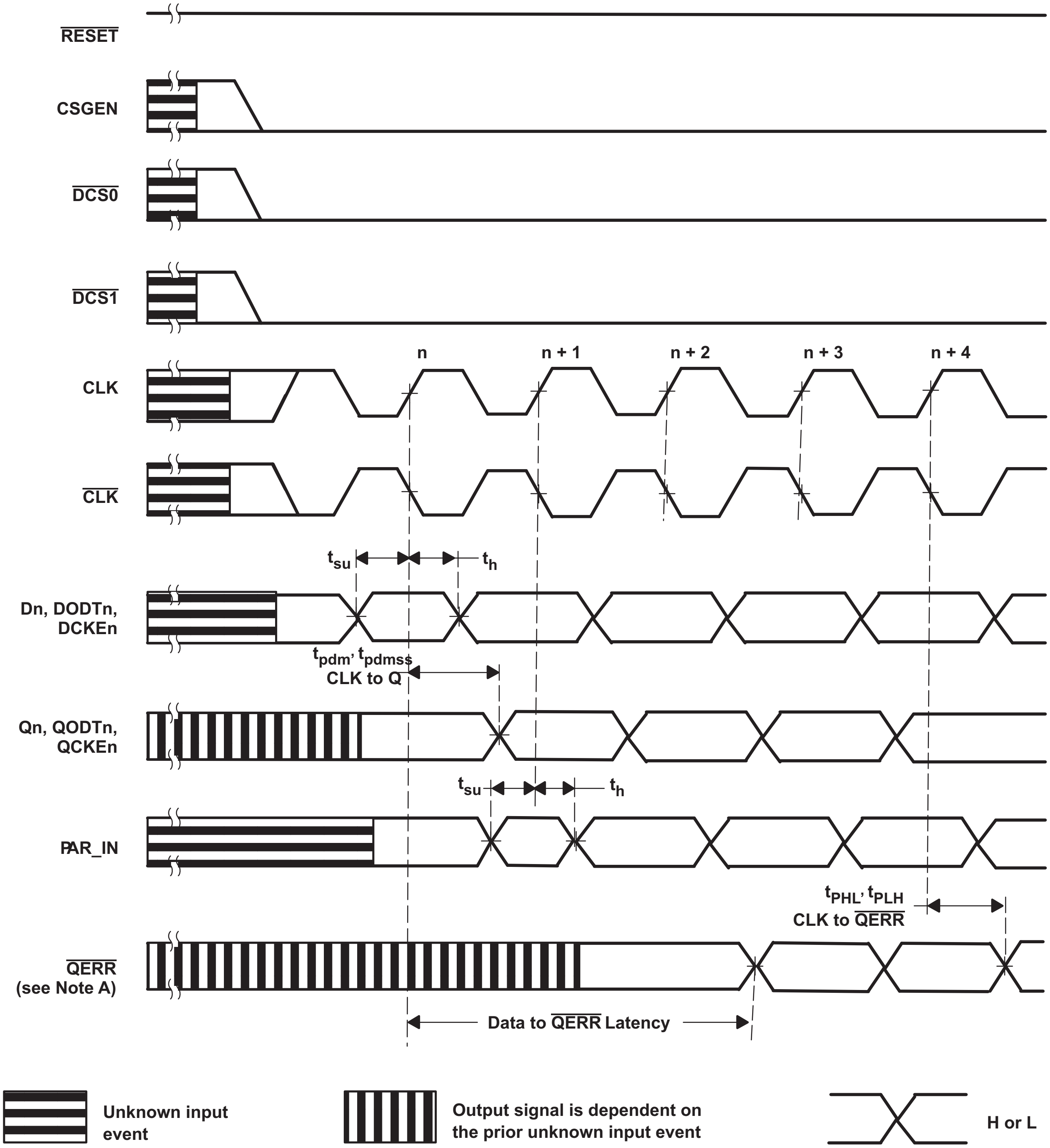
Timing Diagram for 74SSTUB32868 During Start-Up (RESET Switches From L to H)



A. After RESET is switched from low to high, all data and PAR_IN input signals must be set and held low for a minimum time of t_{act} max, to avoid a false error.

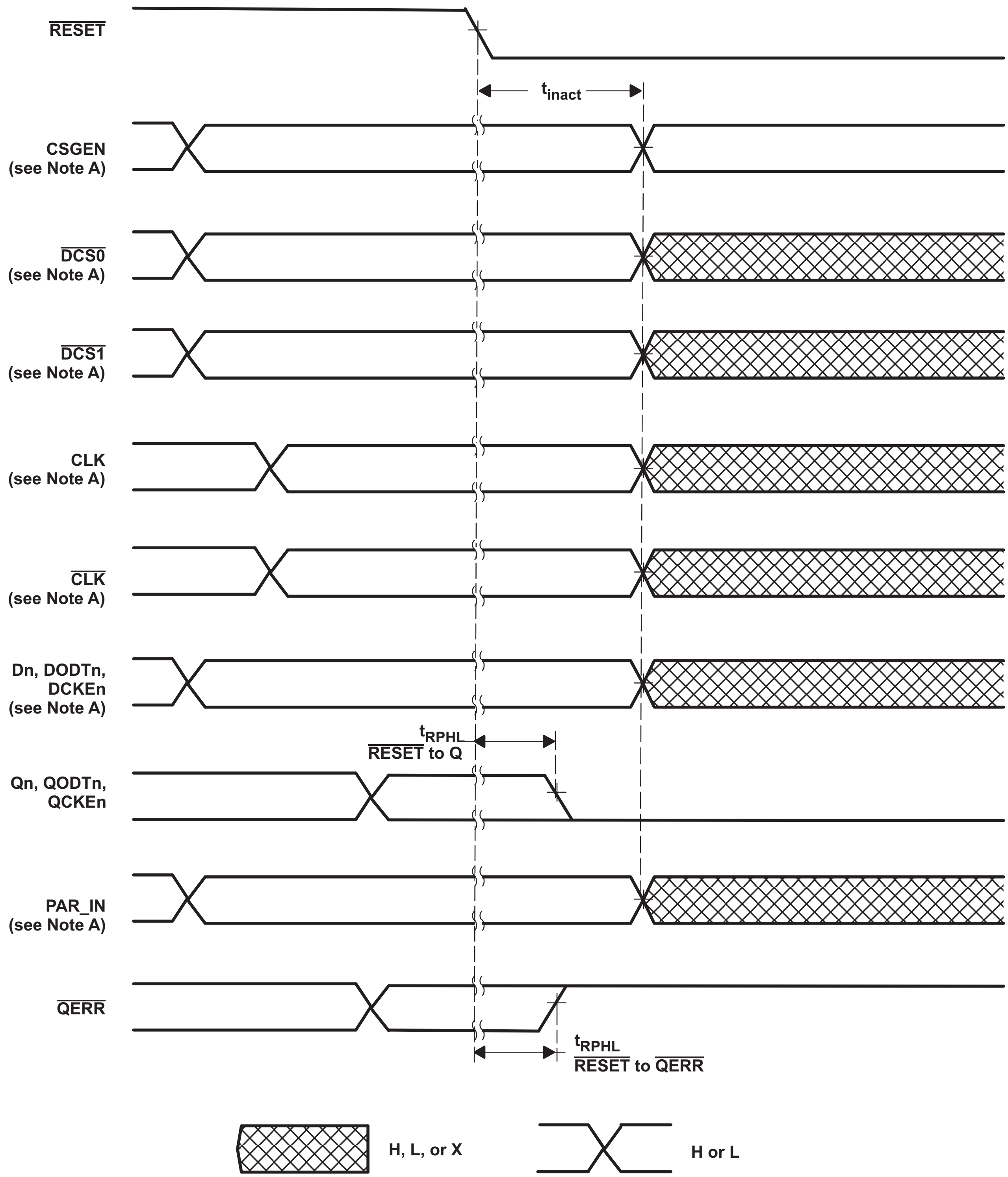
B. If the data is clocked in on the n-clock pulse, the QERR output signal is generated on the n + 2 clock pulse, and it is valid on the n + 3 clock pulse.

Timing Diagram for 74SSTUB32868 During Normal Operation ($\overline{\text{RESET}}$ = H)



A. If the data is clocked in on the n-clock pulse, the $\overline{\text{QERR}}$ output signal is generated on the n + 2 clock pulse, and it is valid on the n + 3 clock pulse. If an error occurs and the $\overline{\text{QERR}}$ output is driven low, it stays latched low for a minimum of two clock cycles or until $\overline{\text{RESET}}$ is driven low.

Timing Diagram for 74SSTUB32868 During Shut-Down (RESET Switches From H to L)



A. After RESET is switched from high to low, all data and clock input signals must be held at logic levels (not floating) for a minimum time of t_{inact} max, to avoid a false error.

TERMINAL FUNCTIONS

TERMINAL NAME	DESCRIPTION	ELECTRICAL CHARACTERISTICS
GND	Ground	Ground input
V_{CC}	Power supply voltage	1.8 V nominal
V_{REF}	Input reference voltage	0.9 V nominal
CLK	Positive master clock input	Differential input
$\overline{\text{CLK}}$	Negative master clock input	Differential input
C	Configuration control input - Register A or Register B	LVCMOS input
$\overline{\text{RESET}}$	Asynchronous reset input − resets registers and disables V_{REF}, data and clock differential-input receivers. When $\overline{\text{RESET}}$ is low, all the Q outputs are forced low and the $\overline{\text{QERR}}$ output is forced high.	LVCMOS input
CSGEN	Chip select gate enable − When high, D1−D28[1] inputs are latched only when at least one chip select input is low during the rising edge of the clock. When low, the D1−D28[1] inputs are latched and redriven on every rising edge of the clock.	LVCMOS input
D1-D28	Data input − clocked in on the crossing of the rising edge of CLK and the falling edge of $\overline{\text{CLK}}$	SSTL_18 input
$\overline{\text{DCS0}}$, $\overline{\text{DCS1}}$	Chip select inputs − These pins initiate DRAM address/command decodes, and as such at least one will be low when a valid address/command is present. The Register can be programmed to redrive all D inputs (CSGEN high) only when at least one chip select input is low. If CSGEN, $\overline{\text{DCS0}}$, and $\overline{\text{DCS1}}$ inputs are high, D1−D28[2] inputs will be disabled.	SSTL_18 input
DODT0, DODT1	The outputs of this register bit will not be suspended by the $\overline{\text{DCS0}}$ and $\overline{\text{DCS1}}$ control.	SSTL_18 input
DCKE0, DEKE1	The outputs of this register bit will not be suspended by the $\overline{\text{DCS0}}$ and $\overline{\text{DCS1}}$ control.	SSTL_18 input
PAR_IN	Parity input − arrives one clock cycle after the corresponding data input. Pulldown resistor of typical 150kΩ to GND.	SSTL_18 input with pulldown
Q1-Q28[3]	Data outputs that are suspended by the $\overline{\text{DCS0}}$ and $\overline{\text{DCS1}}$ control.	1.8 V CMOS output
$\overline{\text{QCS0}}$, $\overline{\text{QCS1}}$	Data output that will not be suspended by the $\overline{\text{DCS0}}$ and $\overline{\text{DCS1}}$ control.	1.8 V CMOS output
QODT0, QODT1	Data output that will not be suspended by the $\overline{\text{DCS0}}$ and $\overline{\text{DCS1}}$ control.	1.8 V CMOS output
QCKE0, QEKE1	Data output that will not be suspended by the $\overline{\text{DCS0}}$ and $\overline{\text{DCS1}}$ control.	1.8 V CMOS output
$\overline{\text{QERR}}$	Output error bit − generated two clock cycles after the corresponding data is registered.	Open-drain output
NC	No internal connection	

(1) Data inputs = D1−D5, D7, D9−D12, D17−D28 when C = 0.
Data inputs = D1−D12, D17−D20, D22, D24−D28 when C = 1.

(2) Data inputs = D1−D5, D7, D9−D12, D17−D28 when C = 0.
Data inputs = D1−D12, D17−D20, D22, D24−D28 when C = 1.

(3) Data outputs = Q1−Q5, Q7, Q9−Q12, Q17−Q28 when C = 0.
Data outputs = Q1−Q12, Q17−Q20, Q22, Q24−Q28 when C = 1.

FUNCTION TABLE

INPUTS							OUTPUTS			
$\overline{\text{RESET}}$	$\overline{\text{DCS0}}$	$\overline{\text{DCS1}}$	CSGEN	CLK	$\overline{\text{CLK}}$	dn, DODTn, DCKEn	Qn	$\overline{\text{QCS0}}$	$\overline{\text{QCS1}}$	QODT, QCKE
H	L	L	X	↑	↓	L	L	L	L	L
H	L	L	X	↑	↓	H	H	L	L	H
H	L	L	X	L or H	L or H	X	Q_0	Q_0	Q_0	Q_0
H	L	H	X	↑	↓	L	L	L	H	L
H	L	H	X	↑	↓	H	H	L	H	H
H	L	H	X	L or H	L or H	X	Q_0	Q_0	Q_0	Q_0
H	H	L	X	↑	↓	L	L	H	L	L
H	H	L	X	↑	↓	H	H	H	L	H
H	H	L	X	L or H	L or H	X	Q_0	Q_0	Q_0	Q_0
H	H	H	L	↑	↓	L	L	H	H	L
H	H	H	L	↑	↓	H	H	H	H	H
H	H	H	L	L or H	L or H	X	Q_0	Q_0	Q_0	Q_0
H	H	H	H	↑	↓	L	Q_0	H	H	L
H	H	H	H	↑	↓	H	Q_0	H	H	H
H	H	H	H	L or H	L or H	X	Q_0	Q_0	Q_0	Q_0
L	X or floating	X or floating	X or floating	X or floating	X or floating	L	L	L	L	L

PARITY AND STANDBY FUNCTION

INPUTS							OUTPUTS
$\overline{\text{RESET}}$	CLK	$\overline{\text{CLK}}$	$\overline{\text{DCS0}}$	$\overline{\text{DCS1}}$	Σ OF INPUTS = H D1 - D22	PAR_IN(1)	$\overline{\text{QERR}}$ (2)
H	↑	↓	L	X	Even	L	H
H	↑		L	X	Odd	L	L
H	↑	↓	L	X	Even	H	L
H	↑	↓	L	X	Odd	H	H
H	↑	↓	X	L	Even	L	H
H	↑	↓	X	L	Odd	L	L
H	↑	↓	X	L	Even	H	L
H	↑	↓	X	L	Odd	H	H
H	↑	↓	H	H	X	X	$\overline{\text{QERR}}_0$ (3)
H	L or H	L or H	X	X	X	X	$\overline{\text{QERR}}_0$
L	X or floating	X or floating	X or floating	X or floating	X	X or floating	H

(1) PAR_IN arrives one clock cycle after the data to which it applies.

(2) This transition assumes that $\overline{\text{QERR}}$ is high at the crossing of CLK going high and $\overline{\text{CLK}}$ going low. If $\overline{\text{QERR}}$ goes low, it stays latched low for a minimum of two clock cycles or until $\overline{\text{RESET}}$ is driven low. If two or more consecutive errors occur, the $\overline{\text{QERR}}$ output is driven low and latched low for a clock duration equal to the parity error duration or until $\overline{\text{RESET}}$ is driven low. For $\overline{\text{QERR}}$ computation, CSGEN is a “don’t care”.

(3) If $\overline{\text{DCS0}}$, $\overline{\text{DCS1}}$ and CSGEN are driven high, the device is placed in a low−power mode (LPM). If a parity error occurs on the clock cycle before the device enters the LPM and the $\overline{\text{QERR}}$ output is driven low, it stays latched low for the LPM duration plus two clock cycles or until $\overline{\text{RESET}}$ is driven low.

TIMING REQUIREMENTS

over recommended ranges of supply voltage, load, and operating free-air temperature (see Figure 1 and Note [1])

			V_{CC} = 1.8 V ±0.1 V		
			MIN	MAX	UNIT
$f_{(clock)}$	Clock frequency			410	MHz
t_w	Pulse duration, CLK, CLK high or low		1		ns
t_{act}	Differential inputs active time (see Note [2])			10	ns
t_{inact}	Differential inputs inactive time (see Note [3])			15	ns
t_{su}	Setup time	$\overline{\text{DCSn}}$ before CLK↑, $\overline{\text{CLK}}$↓, CSGEN high	600		ps
		DCSn before CLK↑, $\overline{\text{CLK}}$↓, CSGEN low	500		
		DODTn, DCKEn, and Data before CLK↑, $\overline{\text{CLK}}$↓	500		
		PAR_IN before CLK↑, $\overline{\text{CLK}}$↓	500		
t_h	Hold time	$\overline{\text{DCSn}}$, DODTn, DCKEn, and Data after CLK↑, $\overline{\text{CLK}}$↓	400		ps
		PAR_IN after CLK↑, $\overline{\text{CLK}}$↓	400		

(1) All inputs slew rate is 1 V/ns ±20%
(2) V_{REF} must be held at a valid input level and data inputs must be held low for a minimum time of t_{act} max, after $\overline{\text{RESET}}$ is taken high.
(3) V_{REF}, data, and clock inputs must be held at valid voltage levels (not floating) for a minimum time of t_{inact} max, after $\overline{\text{RESET}}$ is taken low.

SWITCHING CHARACTERISTICS

over recommended ranges of supply voltage, load, and operating free-air temperature (unless otherwise noted)

			V_{CC} = 1.8 V ±0.1 V		
PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
f_{max} (see Figure 2)			410		MHz
t_{pdm} [1] (production test, see Figure 1)	CLK and $\overline{\text{CLK}}$	Q	0.5	1.0	ns
t_{PLH} (see Figure 4)	CLK and $\overline{\text{CLK}}$	$\overline{\text{QERR}}$	1.2	3	ns
t_{PHL} (see Figure 4)			1	2.4	
t_{RPHL} [2] (see Figure 2)	$\overline{\text{RESET}}$	Q		3	ns
t_{RPLH} (see Figure 4)	$\overline{\text{RESET}}$	$\overline{\text{QERR}}$		3	ns

(1) The typical difference between min and max does not exceed 400 ps.
(2) Includes 350-ps test-load transmission line delay.

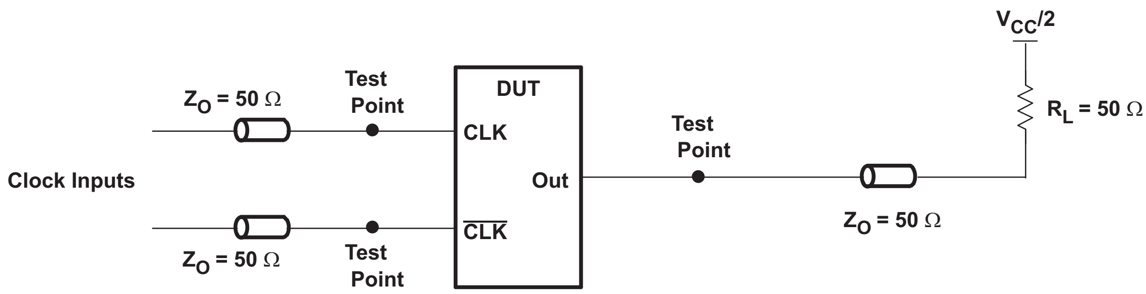
OUTPUT SLEW RATES

over operating free-air temperature range (unless otherwise noted) (see Figure 3)

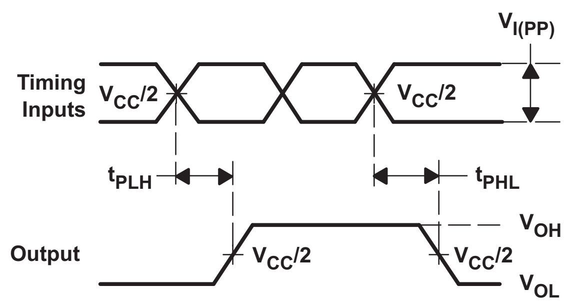
			V_{CC} = 1.8 V ±0.1 V		
PARAMETER	FROM	TO (OUTPUT)	MIN	MAX	UNIT
dV/dt_r	20%	80%	1	5	V/ns
dV/dt_f	80%	20%	1	5	V/ns
dV/dt_Δ [1]	20% to 80%	20% to 80%		1	V/ns

(1) The difference between dV/dr_r (rising edge rate) and dV/dt_f (falling edge).

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



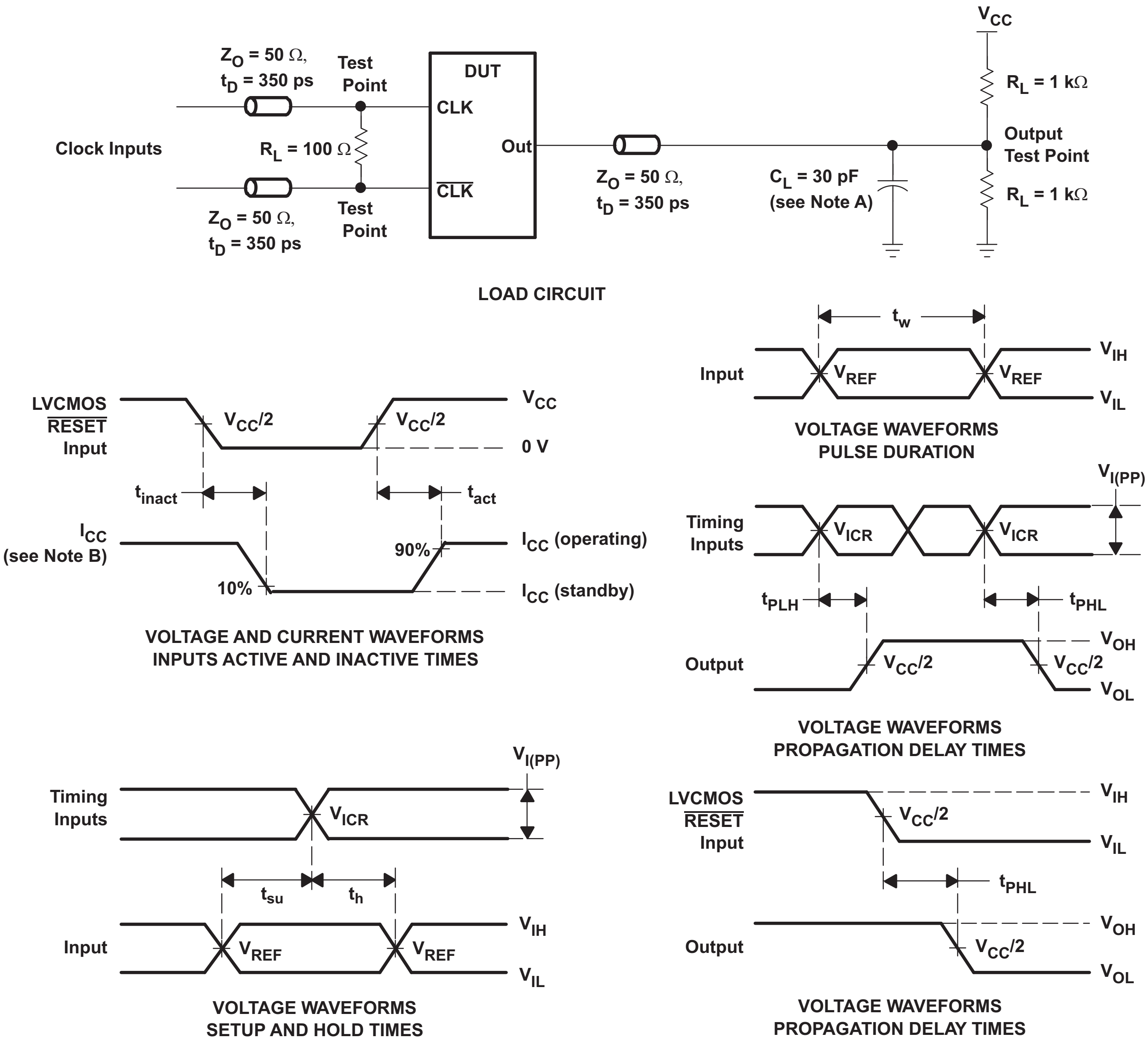
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

Figure 1. Output Load Circuit for Production Test

Propagation Delay (Design Goal as per JEDEC Specification)

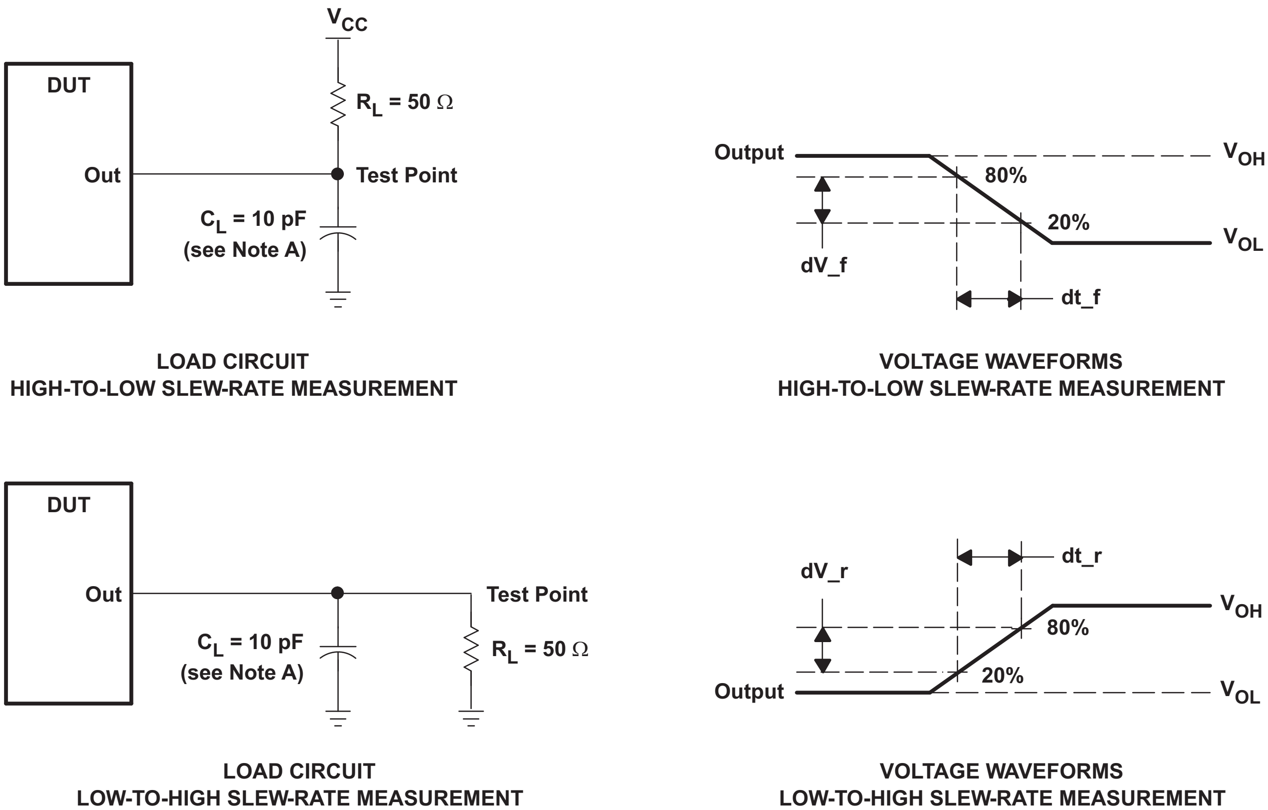
			V_{CC} = 1.8 V ±0.1 V		
PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t_{pdm} (1)	CLK and $\overline{\text{CLK}}$	Q	1.1	1.5	ns
t_{pdmss} (1)	CLK and $\overline{\text{CLK}}$	Q		1.6	ns

(1) Includes 350-ps test-load transmission line delay.



A. C_L includes probe and jig capacitance.
B. I_{CC} tested with clock and data inputs held at V_{CC} or GND, and I_O = 0 mA.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, input slew rate = 1 V/ns ±20% (unless otherwise noted).
D. The outputs are measured one at a time with one transition per measurement.
E. $V_{REF} = V_{CC}/2$
F. $V_{IH} = V_{REF}$ + 250 mV (ac voltage levels) for differential inputs. $V_{IH} = V_{CC}$ for LVCMOS input.
G. $V_{IL} = V_{REF}$ - 250 mV (ac voltage levels) for differential inputs. V_{IL} = GND for LVCMOS input.
H. $V_{I(PP)}$ = 600 mV.
I. t_{PLH} and t_{PHL} are the same as t_{pd}.

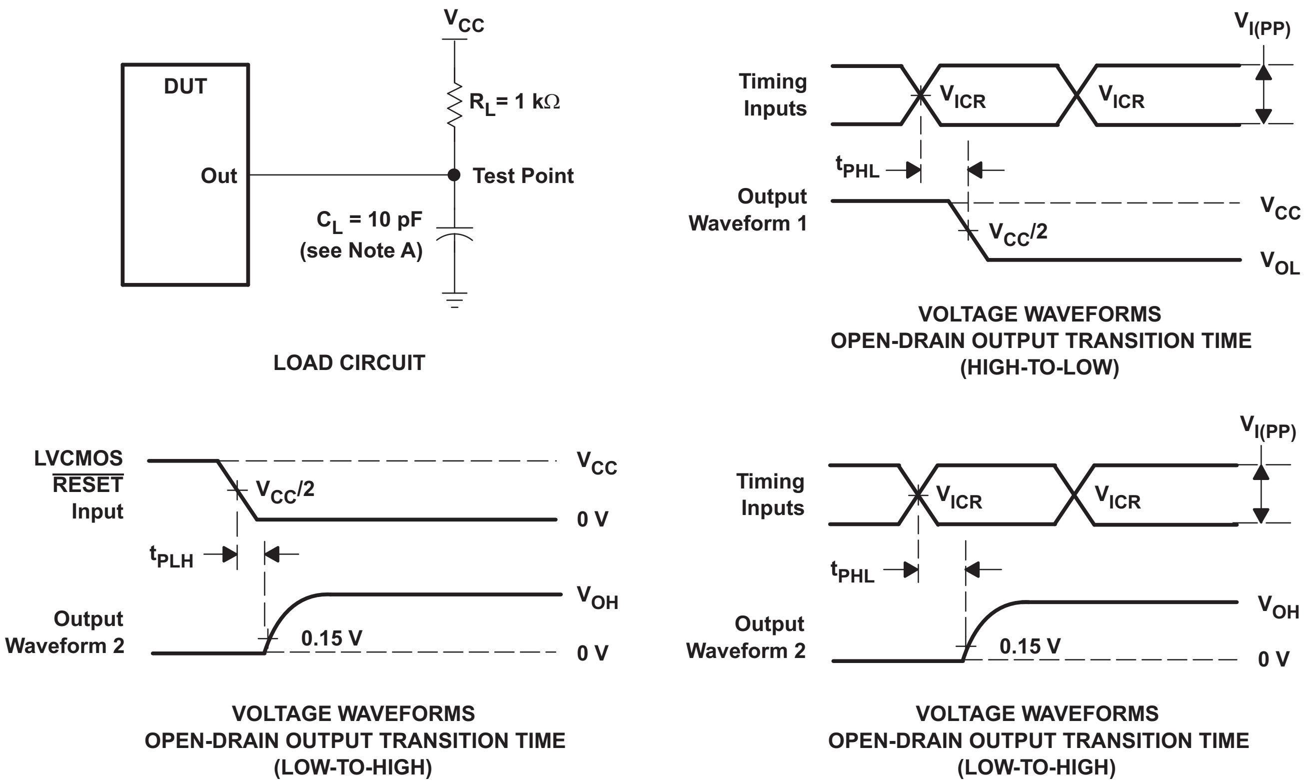
Figure 2. Data Output Load Circuit and Voltage Waveforms



A. C_L includes probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, input slew rate = 1 V/ns ±20% (unless otherwise specified).

Figure 3. Data Output Slew-Rate Measurement Information



A. C_L includes probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, input slew rate = 1 V/ns ±20% (unless otherwise specified).

C. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 4. Error Output Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
74SSTUB32868ZRHR	ACTIVE	NFBGA	ZRH	176	1000	RoHS & Green	SNAGCU	Level-3-260C-168 HR	-40 to 85	SB868	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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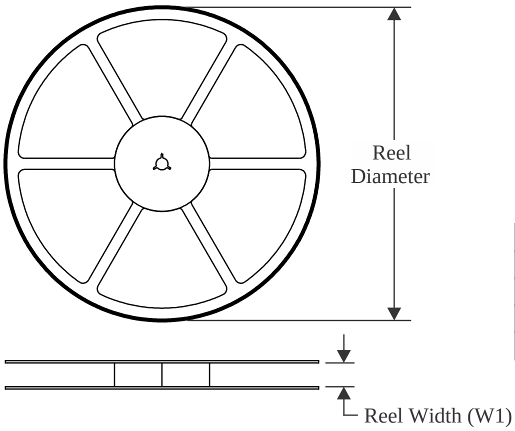
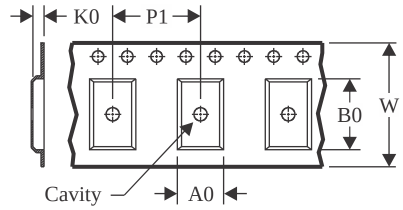
TAPE AND REEL INFORMATION

REEL DIMENSIONS

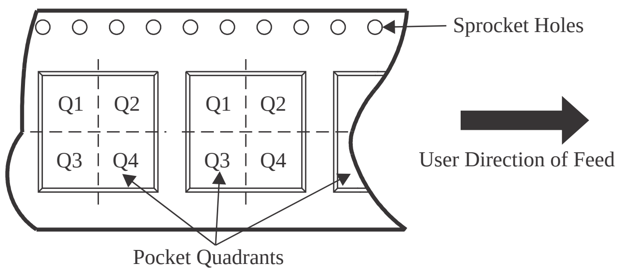


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

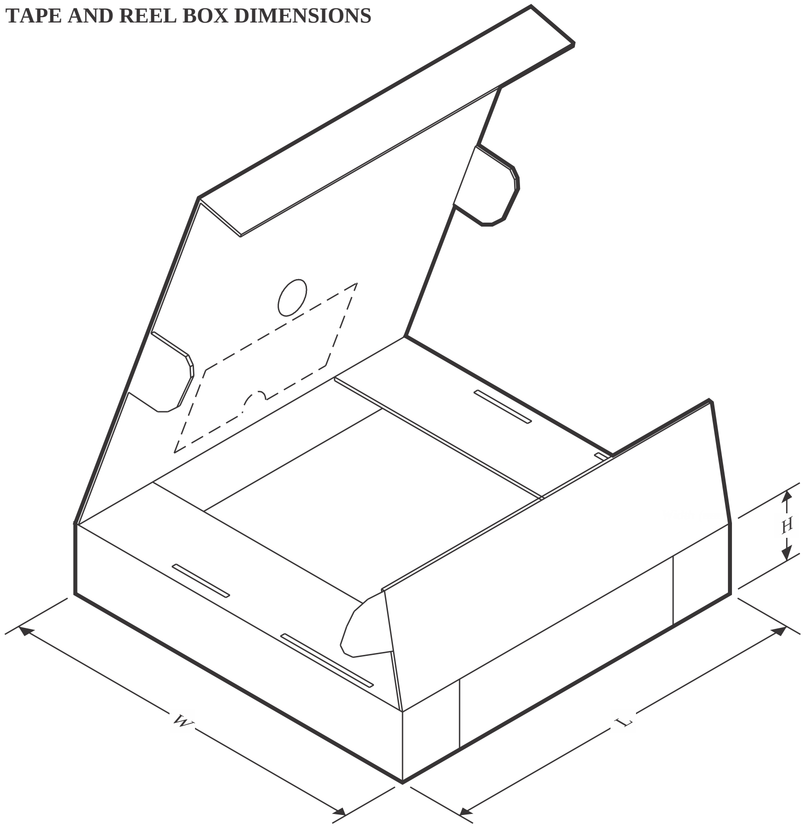
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74SSTUB32868ZRHR	NFBGA	ZRH	176	1000	330.0	24.4	6.3	15.3	1.65	12.0	24.0	Q1

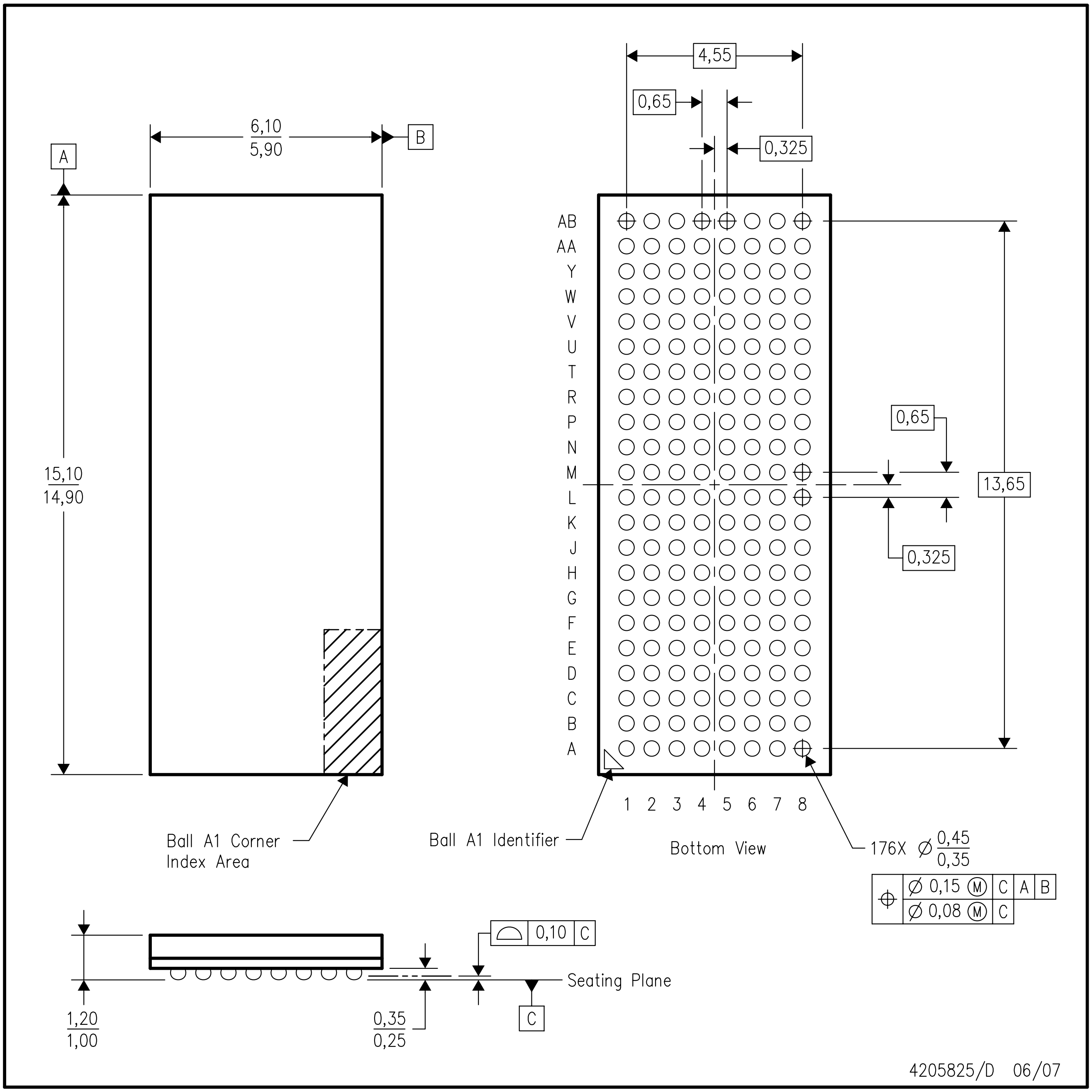
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74SSTUB32868ZRHR	NFBGA	ZRH	176	1000	350.0	350.0	43.0

ZRH (R-PBGA-N176) PLASTIC BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. Complies to JEDEC MO-246 variation B.
D. This package is lead-free. Refer to the 176 GRH package (drawing 4205824) for tin-lead (SnPb).

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