SN74CBT16214 12-Bit 1-of-3 FET Multiplexer/Demultiplexer

1 Features

- Member of the Texas Instruments Widebus™ Family
- 5-Ω Switch Connection Between Two Ports
- TTL-Compatible Input Levels

2 Applications

- Analog and Digital Multiplexing and Demultiplexing
- A/D and D/A Conversion
- Factory Automation
- Consumer Audio
- Programmable Logic Circuits
- Sensors

3 Description

The SN74CBT16214 provides 12 bits of high-speed TTL-compatible bus switching between three separate ports. The low ON-state resistance of the switch allows connections to be made with minimal propagation delay.

The device operates as a 12-bit bus-select switch via the data-select (S0–S2) terminals.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74CBT16214DGG	TSSOP (56)	8.10 mm × 14.00 mm
SN74CBT16214DL	SSOP (56)	10.35 mm x 18.42 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Logic Diagram (Positive Logic)

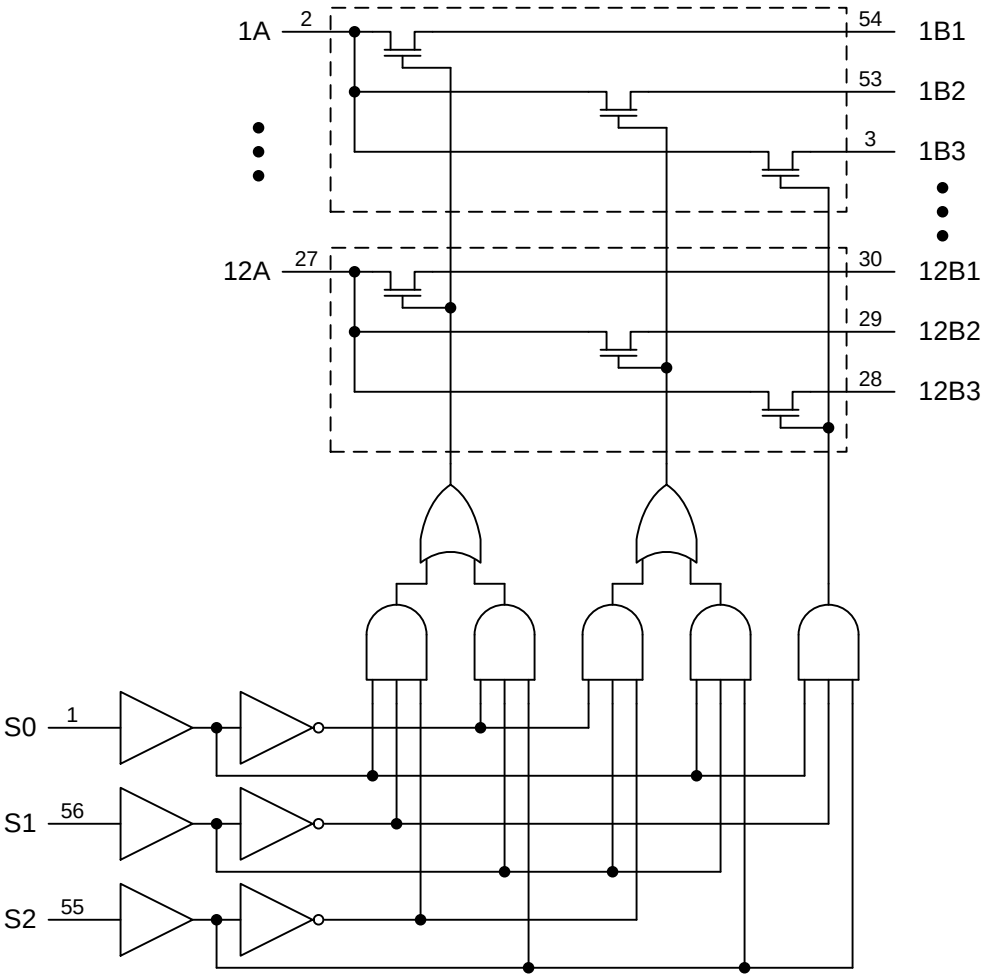


Table of Contents

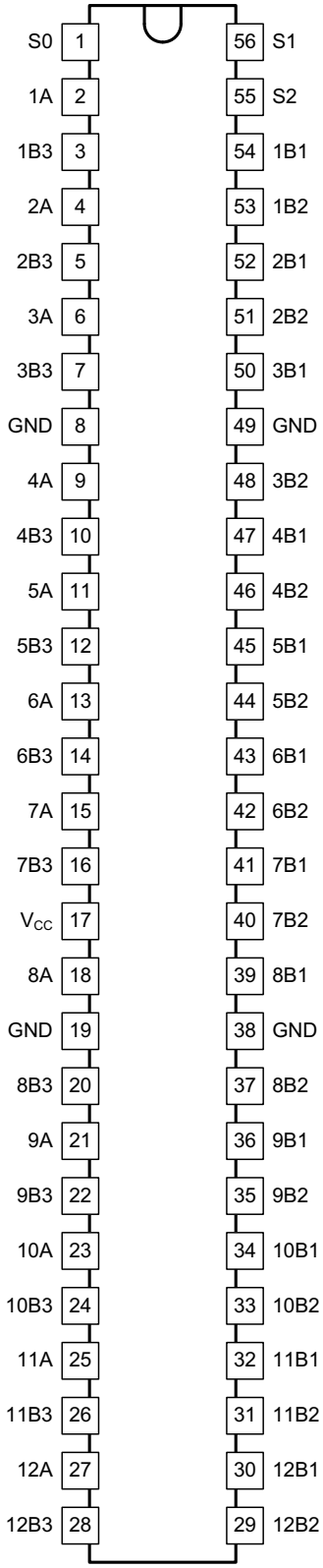
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision L (November 2001) to Revision M	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section.	1

5 Pin Configuration and Functions

DGG or DL Package
56-Pin TSSOP or SSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
S0	1	I	Select 0
1A	2	I/O	Channel 1 A
1B3	3	I/O	Channel 1 B3
2A	4	I/O	Channel 2 A
2B3	5	I/O	Channel 2 B3
3A	6	I/O	Channel 3 A
3B3	7	I/O	Channel 3 B3
GND	8	—	Ground
4A	9	I/O	Channel 4 A
4B3	10	I/O	Channel 4 B3
5A	11	I/O	Channel 5 A
5B3	12	I/O	Channel 5 B3
6A	13	I/O	Channel 6 A
6B3	14	I/O	Channel 6 B3
7A	15	I/O	Channel 7 A
7B3	16	I/O	Channel 7 B3
V_{CC}	17	—	Power supply
8A	18	I/O	Channel 8 A
GND	19	—	Ground
8B3	20	I/O	Channel 8 B3
9A	21	I/O	Channel 9 A
9B3	22	I/O	Channel 9 B3
10A	23	I/O	Channel 10 A
10B3	24	I/O	Channel 10 B3
11A	25	I/O	Channel 11 A
11B3	26	I/O	Channel 11 B3
12A	27	I/O	Channel 12 A
12B3	28	I/O	Channel 12 B3
12B2	29	I/O	Channel 12 B2
12B1	30	I/O	Channel 12 B1
11B2	31	I/O	Channel 11 B2
11B1	32	I/O	Channel 11 B1
10B2	33	I/O	Channel 10 B2
10B1	34	I/O	Channel 10 B1
9B2	35	I/O	Channel 9 B2
9B1	36	I/O	Channel 9 B1
8B2	37	I/O	Channel 8 B2
GND	38	—	Ground
8B1	39	I/O	Channel 8 B1
7B2	40	I/O	Channel 7 B2
7B1	41	I/O	Channel 7 B1
6B2	42	I/O	Channel 6 B2
6B1	43	I/O	Channel 6 B1
5B2	44	I/O	Channel 5 B2
5B1	45	I/O	Channel 5 B1
4B2	46	I/O	Channel 4 B2

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
4B1	47	I/O	Channel 4 B1
3B2	48	I/O	Channel 3 B2
GND	49	I/O	Ground
3B1	50	I/O	Channel 3 B1
2B2	51	I/O	Channel 2 B2
2B1	52	I/O	Channel 2 B1
1B2	53	I/O	Channel 1 B2
1B1	54	I/O	Channel 1 B1
S2	55	I	Select 2
S1	56	I	Select 1

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	–0.5	7	V
V_I	Input voltage(2)	–0.5	7	V
	Continuous channel current		128	mA
I_{IK}	Input clamp current, (V_I < 0)		50	mA
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
V_{IH}	High-level control input voltage	2		V
V_{IL}	Low-level control input voltage		0.8	V
T_A	Operating free-air temperature	–40	85	°C

(1) All unused control inputs of the device must be held at VCC or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.

6.4 Thermal Information

THERMAL METRIC[1]		SN74CBT16214		UNIT
		DGG (TSSOP)	DL (SSOP)	
		56 PINS	56 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	64	56	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP[1]	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = –18 mA				–1.2	V
I_I		V_{CC} = 0,	V_I = 5.5 V				10	µA
		V_{CC} = 5.5 V,	V_I = 5.5 V or GND				±1	
I_{CC}		V_{CC} = 5.5 V,	I_O = 0,	V_I = V_{CC} or GND			3	µA
ΔI_{CC}[2]	Control inputs	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
C_i		V_I = 3 V or 0				4		pF
$C_{io(OFF)}$		V_O = 3 V or 0,	S_0, S_1, and S_2 = GND			7.5		pF
r_{on}[3]		V_{CC} = 4 V, TYP at V_{CC} = 4 V	V_I = 2.4 V,	I_I = 15 mA		14	20	Ω
		V_{CC} = 4.5 V	V_I = 0	I_I = 64 mA		4	7	Ω
				I_I = 30 mA		4	7	
			V_I = 2.4 V,	I_I = 15 mA		6	12	

(1) All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.
(2) This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.
(3) Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

6.6 Switching Characteristics

over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4 V		V_{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}[1]	A or B	B or A		0.35		0.25	ns
t_{pd}	S	B or A		15.3	5.5	13.9	ns
t_{en}	S	A or B		16	5.1	14.5	ns
t_{dis}	S	A or B		12.1	3.6	11.7	ns

(1) The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

6.7 Typical Characteristics

over operating free-air temperature range (unless otherwise noted)

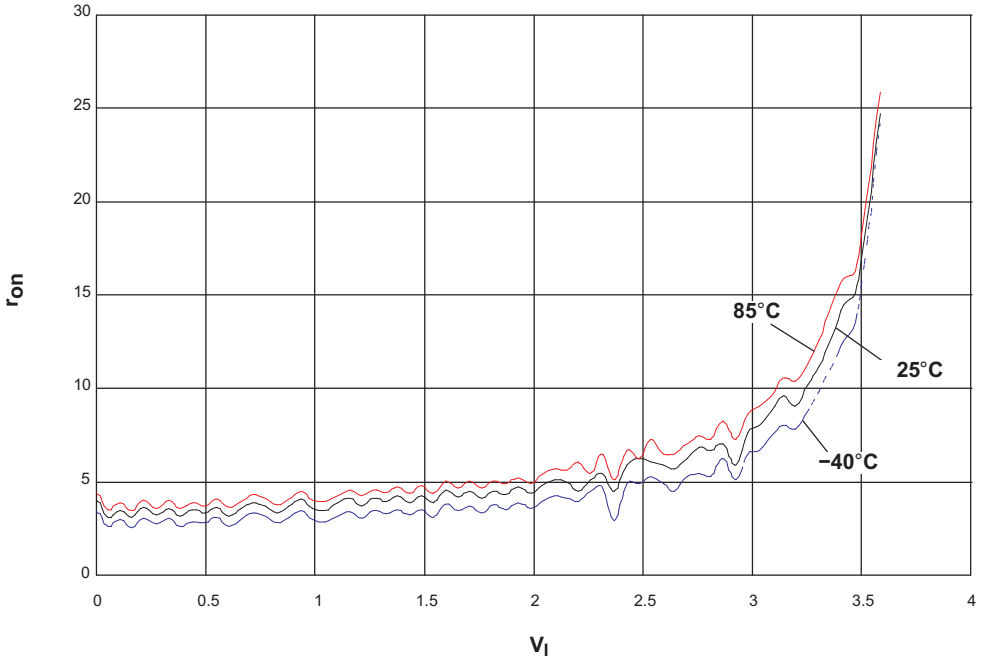
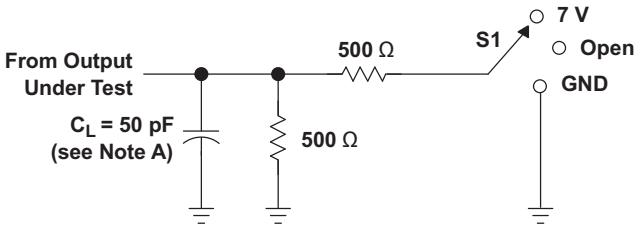


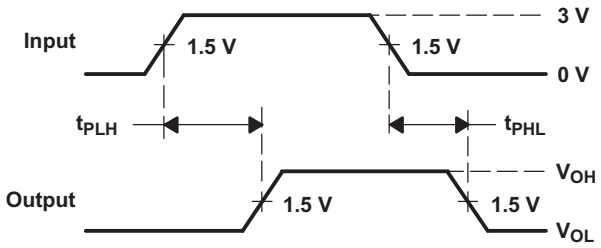
Figure 1. r_{ON} vs. V_I, V_{CC} = 5 V

7 Parameter Measurement Information

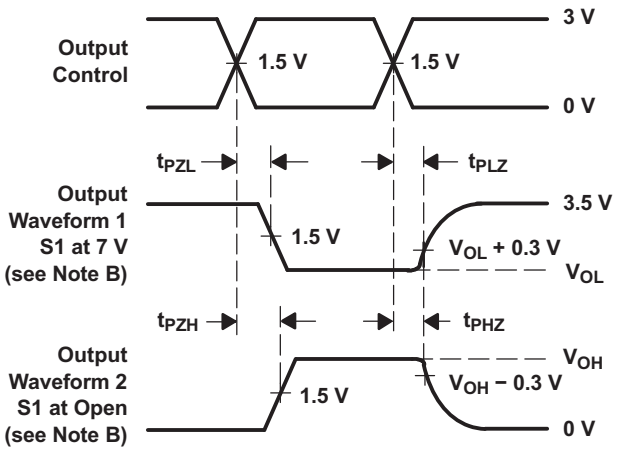


LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 2. Load Circuit and Voltage Waveforms

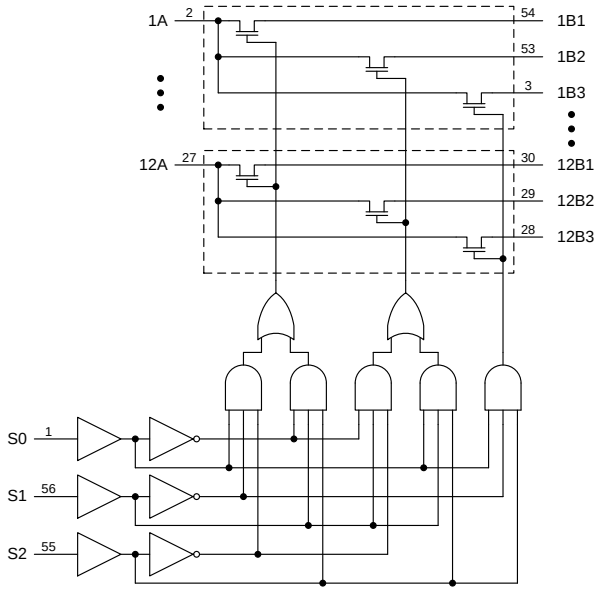
8 Detailed Description

8.1 Overview

The SN74CBT16214 provides 12 bits of high-speed TTL-compatible bus switching between three separate ports. The low ON-state resistance of the switch allows connections to be made with minimal propagation delay.

The device operates as a 12-bit bus-select switch via the data-select (S0–S2) terminals.

8.2 Functional Block Diagram



8.3 Feature Description

The typical R_{ON} for each port is 5 Ω, reducing the amount of signal attenuation through the switch from higher impedance switches. Inputs operate with TTL-compatible voltages.

8.4 Device Functional Modes

Table 1 lists the functional modes for SN74CBT16214.

Table 1. Function Table

INPUTS			INPUT/OUTPUT A	FUNCTION
S2	S1	S0		
L	L	L	Z	Disconnect
L	L	H	B1	A port = B1 port
L	H	L	B2	A port = B2 port
L	H	H	Z	Disconnect
H	L	L	Z	Disconnect
H	L	H	B3	A port = B3 port
H	H	L	B1	A port = B1 port
H	H	H	B2	A port = B2 port

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN74CBT16214 is typically used to expand a single 12-bit bus to three separate 12-bit busses. Fewer bits can be used as well if the unused inputs are tied to either ground or V_{CC}.

9.2 Typical Application

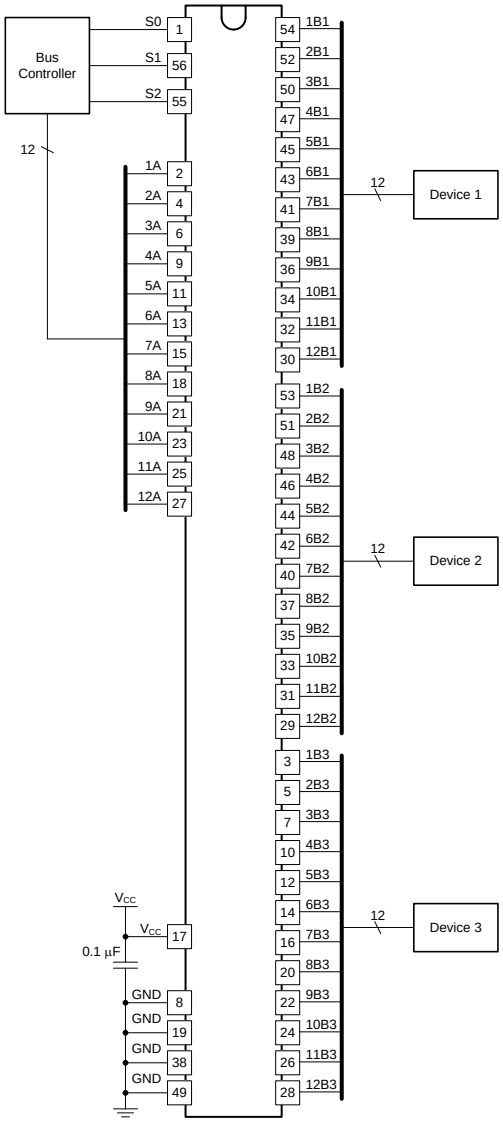


Figure 3. Typical Application Simplified Schematic

9.2.1 Design Requirements

The 0.1-uF capacitor should be placed as close as possible to the V_{CC} pin of the device.

Typical Application (continued)

9.2.2 Detailed Design Procedure

1. Recommended Input Conditions
   - For switch time specifications, see propagation delay times in *Switching Characteristics*.
   - Inputs should remain between 0.5 V and 7 V, regardless of V_{CC}.
   - For input voltage level specifications for control inputs, see V_{IH} and V_{IL} in *Recommended Operating Conditions*.
2. Input/output current consideration: The SN74CBT16214 does not have internal current drive circuitry and thus cannot sink or source current. Any current will be passed through the device.

9.2.3 Application Curve

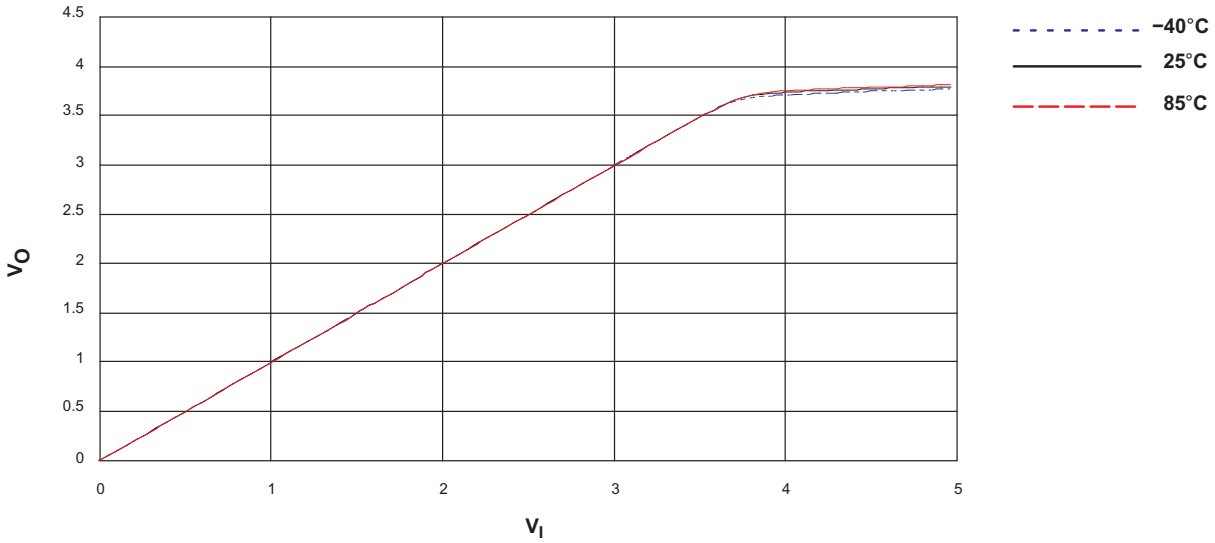


Figure 4. V_O vs V_I, V_{CC} = 5 V

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Electrical Characteristics*.

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single-supply, a 0.1-µF bypass capacitor is recommended. If there are multiple pins labeled V_{CC}, then a 0.01-µF or 0.022-µF capacitor is recommended for each V_{CC} because the V_{CC} pins will be tied together internally. For devices with dual-supply pins operating at different voltages, for example V_{CC} and V_{DD}, a 0.1-µF bypass capacitor is recommended for each supply pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

11 Layout

11.1 Layout Guidelines

Reflections and matching are closely related to loop antenna theory, but different enough to warrant their own discussion. When a PCB trace turns a corner at a 90° angle, a reflection can occur. This is primarily due to the change of width of the trace. At the apex of the turn, the trace width is increased to 1.414 times its width. This upsets the transmission line characteristics, especially the distributed capacitance and self–inductance of the trace — resulting in the reflection. It is a given that not all PCB traces can be straight, and so they will have to turn corners. Figure 5 shows progressively better techniques of rounding corners. Only the last example maintains constant trace width and minimizes reflections.

11.2 Layout Example

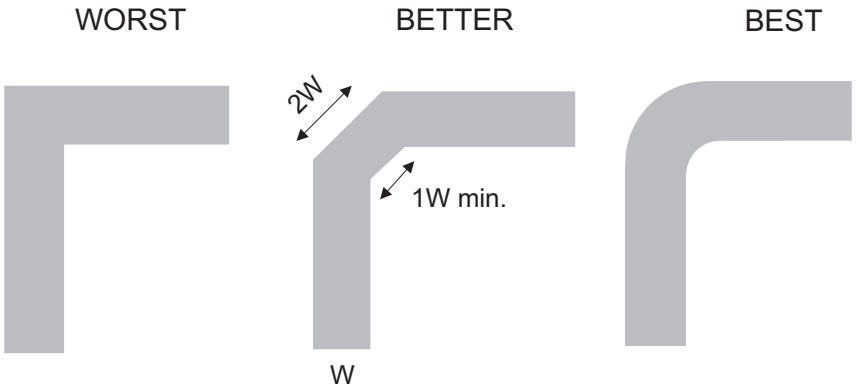


Figure 5. Trace Example

12 Device and Documentation Support

12.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74CBT16214DGGR	ACTIVE	TSSOP	DGG	56	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT16214	Samples
SN74CBT16214DL	ACTIVE	SSOP	DL	56	20	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT16214	Samples
SN74CBT16214DLR	ACTIVE	SSOP	DL	56	1000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT16214	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

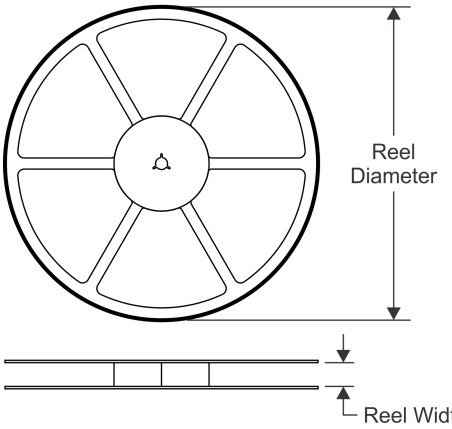
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

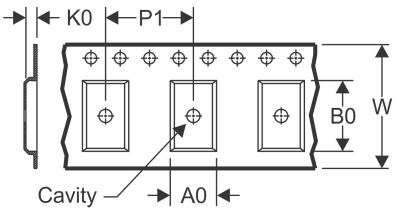
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

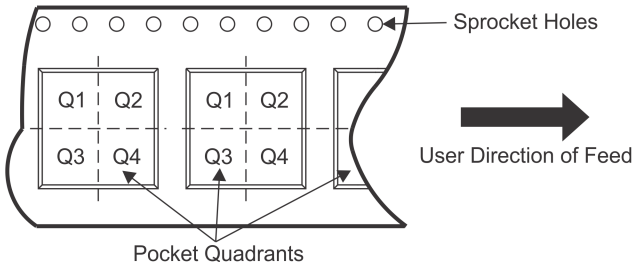


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

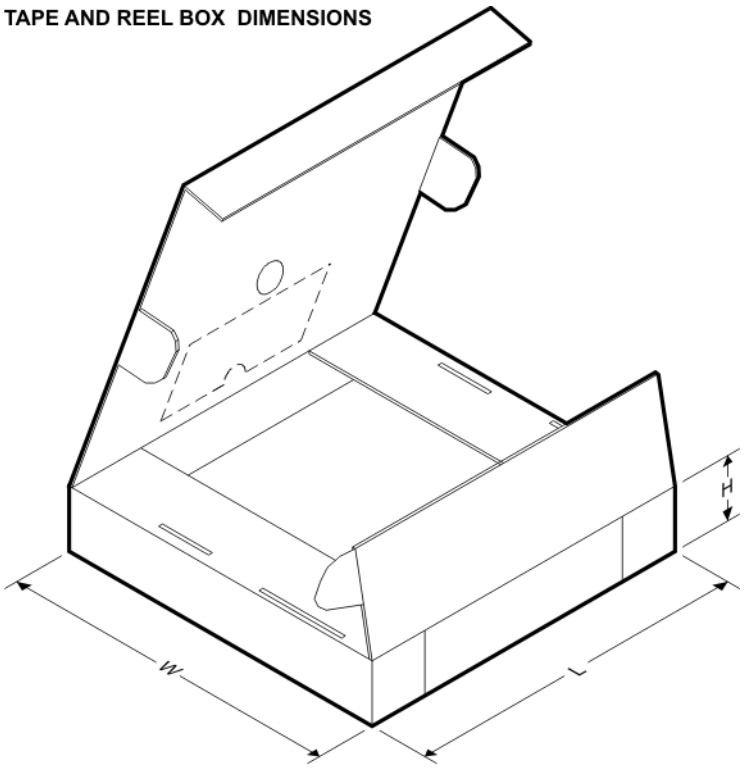
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CBT16214DGGR	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1
SN74CBT16214DLR	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1

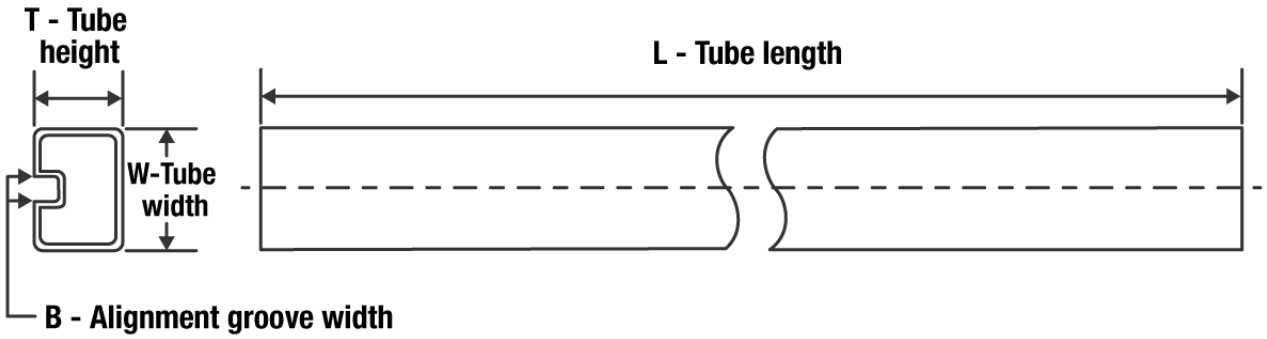
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74CBT16214DGGR	TSSOP	DGG	56	2000	367.0	367.0	45.0
SN74CBT16214DLR	SSOP	DL	56	1000	367.0	367.0	55.0

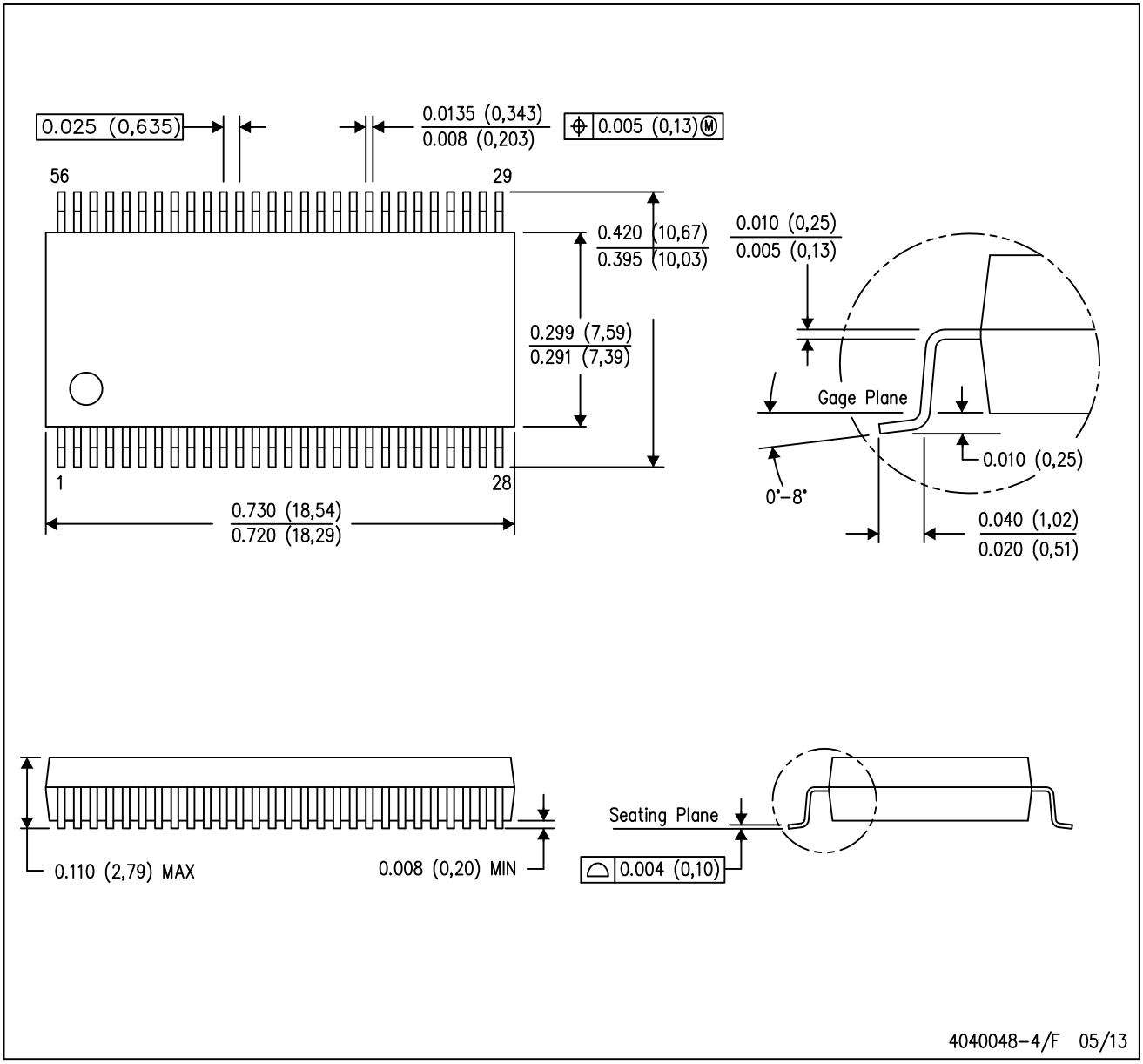
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74CBT16214DL	DL	SSOP	56	20	473.7	14.24	5110	7.87

DL (R–PDSO–G56) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MO–118

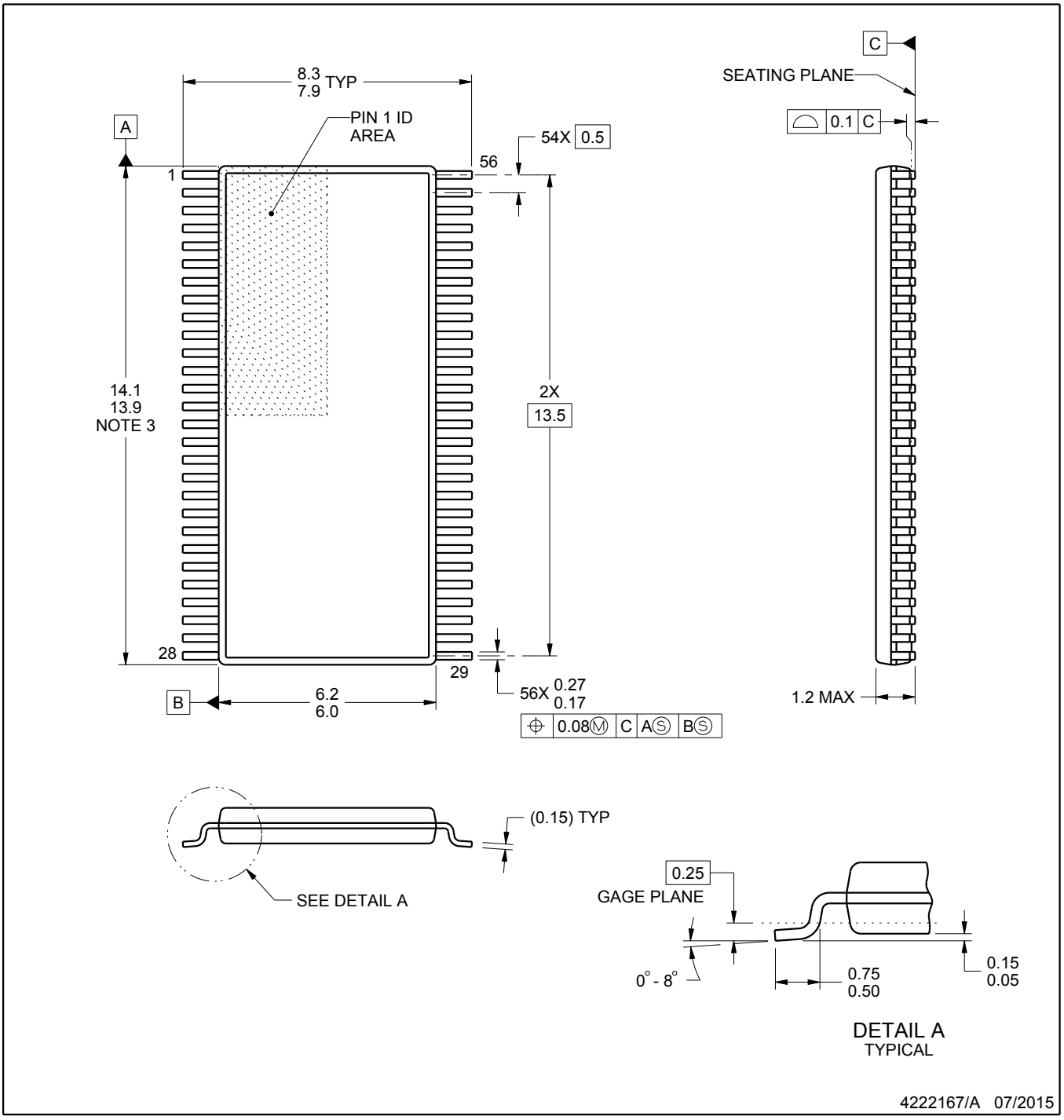
PowerPAD is a trademark of Texas Instruments.

PACKAGE OUTLINE

DGG0056A

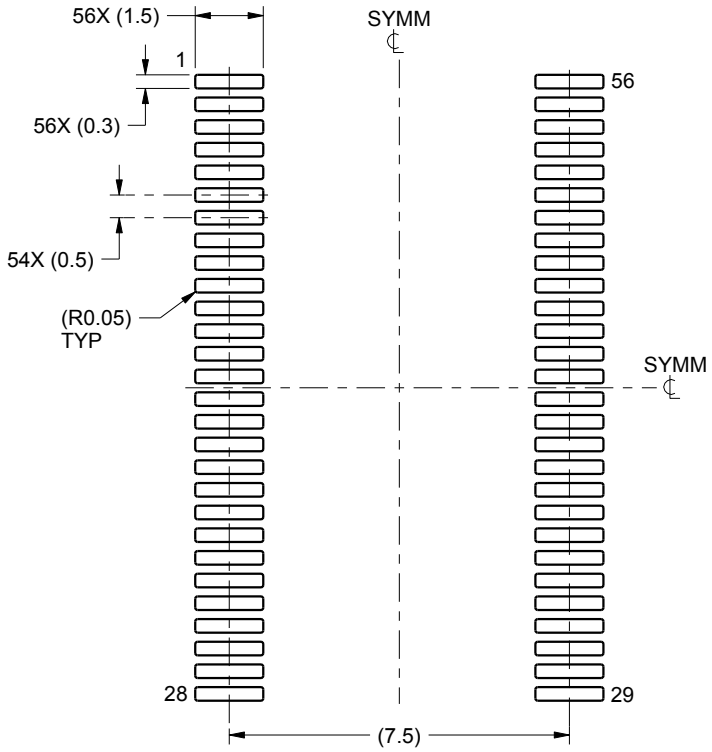
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

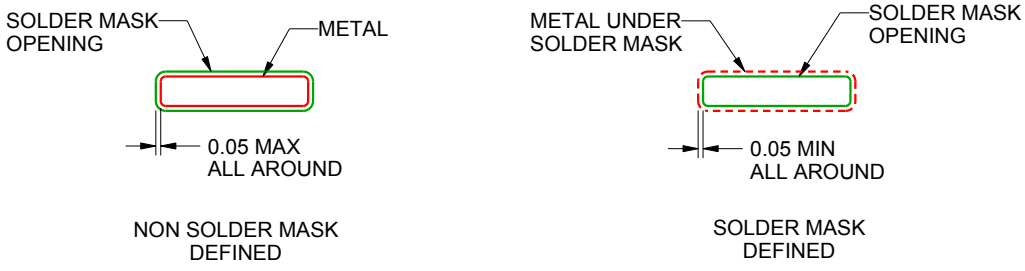


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
SCALE:6X

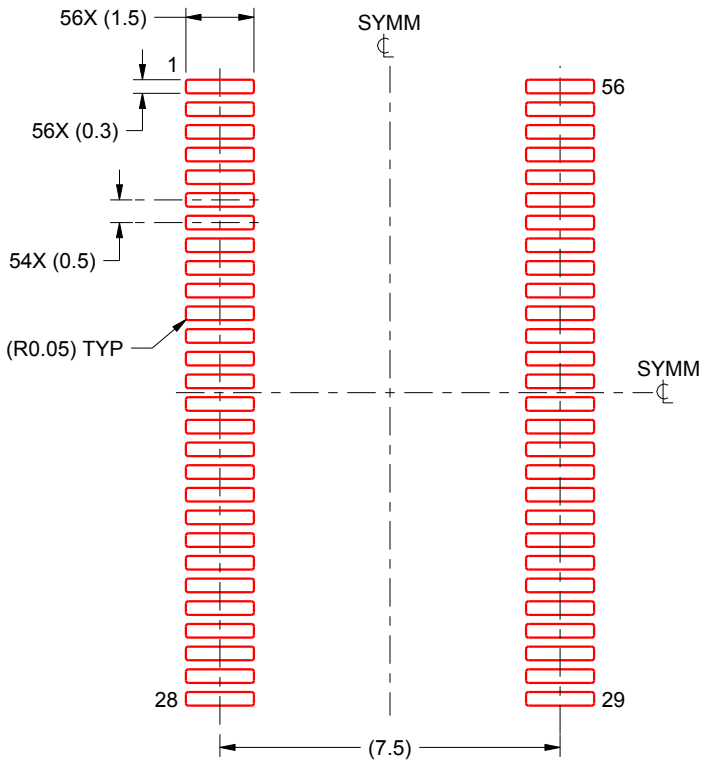


SOLDER MASK DETAILS

4222167/A 07/2015

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4222167/A 07/2015

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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