LM4876 Boomer® Audio Power Amplifier Series 1.1W Audio Power Amplifier with Logic Low Shutdown

Check for Samples: LM4876

FEATURES

- **Does Not Require Output Coupling Capacitors, Bootstrap Capacitors, Or Snubber Circuits**
- **10-pin VSSOP and 8-pin SOIC Packages**
- **Unity-Gain Stable**
- **External Gain Set**

APPLICATIONS

- **Mobile Phones**
- **Portable Computers**
- **Desktop Computers**
- **Low-Voltage Audio Systems**

KEY SPECIFICATIONS

- **THD+N at 1kHz for 1W Continuous Average Output Power into 8Ω 0.5% (max)**
- **Output Power At 1kHz Into 8Ω with 10% THD+N 1.5 W (typ)**
- **Shutdown Current 0.01μA (typ)**
- **Supply Voltage Range 2.0V to 5.5 V**

DESCRIPTION

The LM4876 is a single 5V supply bridge-connected audio power amplifier capable of delivering 1.1W (typ) of continuous average power to an 8Ω load with 0.5% THD+N.

Like other audio amplifiers in the Boomer series, the LM4876 is designed specifically to provide high quality output power with a minimal amount of external components. The LM4876 does not require output coupling capacitors, bootstrap capacitors, or snubber networks. It is perfectly suited for low-power portable systems.

The LM4876 features an active low externally controlled, micro-power shutdown mode. Additionally, the LM4876 features an internal thermal shutdown protection mechanism. For PCB space efficiency, the LM4876 is available in VSSOP and SOIC surface mount packages.

The unity-gain stable LM4876's closed loop gain is set using external resistors.

Typical Application

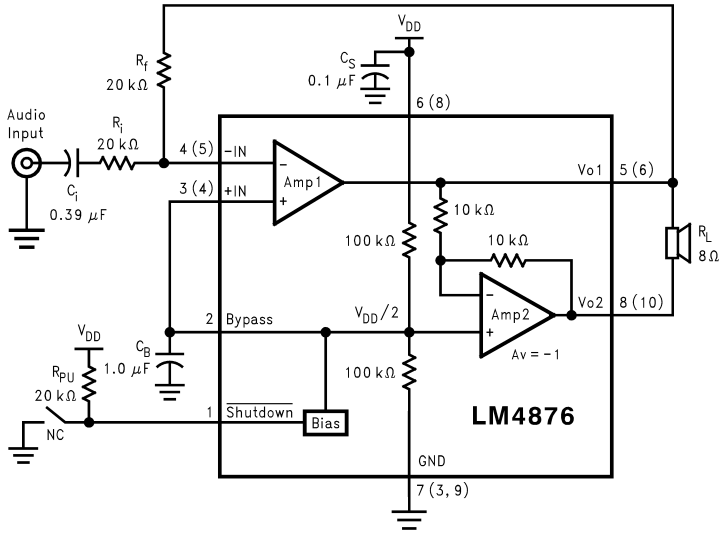


Figure 1. Typical LM4876 Audio Amplifier Application Circuit
Numbers in ( ) are specific to the 10-pin VSSOP package.

Connection Diagrams

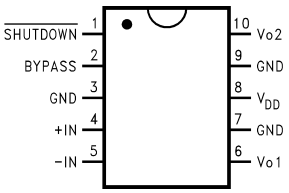


Figure 2. VSSOP Package – Top View
See Package Number DGS

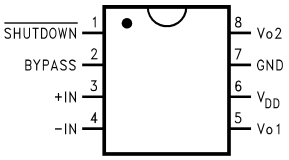


Figure 3. SOIC Package – Top View
See Package Number D

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)

Supply Voltage			6.0V
Storage Temperature			−65°C to +150°C
Input Voltage			−0.3V to V_{DD} +0.3V
Power Dissipation(3)			Internally Limited
ESD Susceptibility(4)			2500V
ESD Susceptibility(5)			250V
Junction Temperature			150°C
Soldering Information	Small Outline Package	Vapor Phase (60 sec.)	215°C
		Infrared (15 sec.)	220°C
θ_{JC} (typ)—DGS			56°C/W
θ_{JA} (typ)—DGS			210°C/W
θ_{JC} (typ)—D			35°C/W
θ_{JA} (typ)—D			140°C/W

(1) If Military/Aerospace specified devices are required, please contact the Texas Instruments' Sales Office/ Distributors for availability and specifications.
(2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions that ensure specific performance limits. This assumes that the device operates within the Operating Ratings. Specifications are not ensured for parameters where no limit is given. The typical value, however, is a good indication of device performance.
(3) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX}–T_A)/\theta_{JA}$ or the number given in Absolute Maximum Ratings, whichever is lower. For the LM4876, T_{JMAX} = 150°C. The typical junction-to-ambient thermal resistance is 140°C/W for the D package and 210°C/W for the DGS package.
(4) Human body model, 100 pF discharged through a 1.5 kΩ resistor.
(5) Machine Model, 220 pF–240 pF discharged through all pins.

Operating Ratings

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$	−40°C ≤ T_A ≤ 85°
Supply Voltage		2.0V ≤ V_{DD} ≤ 5.5V

Electrical Characteristics (1)(2)

The following specifications apply for V_{DD} = 5V unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM4876		Units (Limits)
			Typical (3)	Limit (4)	
V_{DD}	Supply Voltage			2.0	V (min)
				5.5	V (max)
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, I_o = 0A	6.5	10.0	mA (max)
I_{SD}	Shutdown Current	V_{PIN1} = 0V	0.01	2	µA (max)
V_{OS}	Output Offset Voltage	V_{IN} = 0V	5	50	mV (max)
P_o	Output Power	THD = 0.5% (max); f = 1 kHz; R_L = 8Ω	1.10	1.0	W (min)
		THD+N = 10%; f = 1 kHz; R_L = 8Ω	1.5		W
THD+N	Total Harmonic Distortion+Noise	P_o = 1 Wrms; A_{VD} = 2; 20 Hz ≤ f ≤ 20 kHz; R_L = 8Ω	0.25		%
PSRR	Power Supply Rejection Ratio	V_{DD} = 4.9V to 5.1V	65		dB

(1) All voltages are measured with respect to the ground pin, unless otherwise specified.
(2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions that ensure specific performance limits. This assumes that the device operates within the Operating Ratings. Specifications are not ensured for parameters where no limit is given. The typical value, however, is a good indication of device performance.
(3) Typicals are measured at 25°C and represent the parametric norm.
(4) Limits are ensured to AOQL (Average Outgoing Quality Level).

Electrical Characteristics V_{DD} = 5/3.3/2.6V

Symbol	Parameter	Conditions	LM4876		Units (Limits)
			Typical (1)	Limit (2)	
V_{IH}	Shutdown Input Voltage High			1.2	V(min)
V_{IL}	Shutdown Input Voltage Low			0.4	V(max)

(1) Typicals are measured at 25°C and represent the parametric norm.
(2) Limits are ensured to AOQL (Average Outgoing Quality Level).

External Components Description

(Figure 1)

Components		Functional Description
1.	R_i	Inverting input resistance which sets the closed-loop gain in conjunction with R_f. This resistor also forms a high pass filter with C_i at $f_C = 1/(2\pi R_i C_i)$.
2.	C_i	Input coupling capacitor which blocks the DC voltage at the amplifiers input terminals. Also creates a highpass filter with R_i at $f_C = 1/(2\pi R_i C_i)$. Refer to the section, SELECTING PROPER EXTERNAL COMPONENTS, for an explanation of how to determine the value of C_i.
3.	R_f	Feedback resistance which sets the closed-loop gain in conjunction with R_i.
4.	C_S	Supply bypass capacitor which provides power supply filtering. Refer to the POWER SUPPLY BYPASSING section for information concerning proper placement and selection of the supply bypass capacitor.
5.	C_B	Bypass pin capacitor which provides half-supply filtering. Refer to the section, SELECTING PROPER EXTERNAL COMPONENTS, for information concerning proper placement and selection of C_B.

Typical Performance Characteristics

THD+N vs Frequency

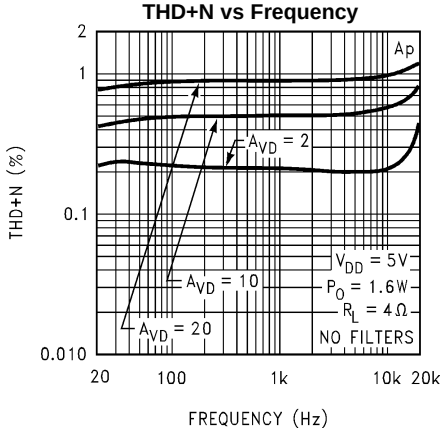


Figure 4.

THD+N vs Frequency

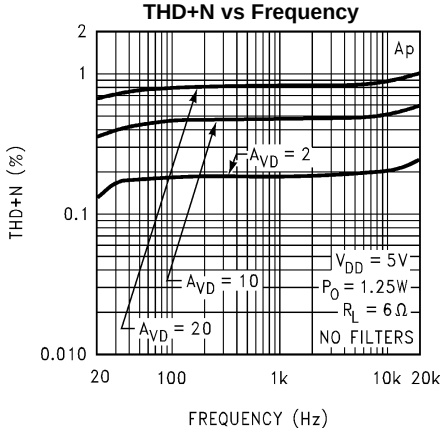


Figure 5.

THD+N vs Frequency

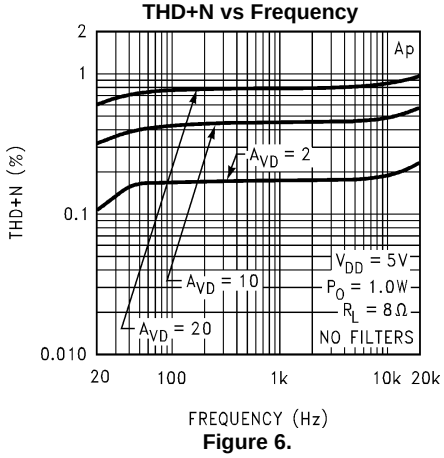


Figure 6.

THD+N vs Output Power

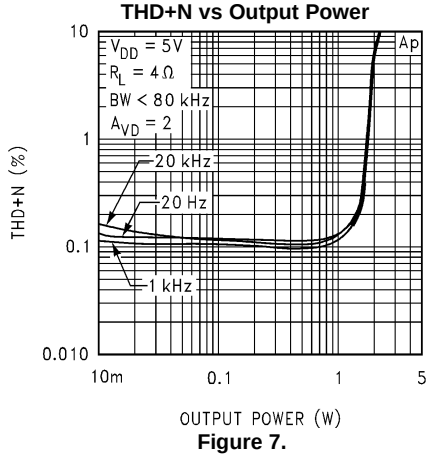


Figure 7.

THD+N vs Output Power

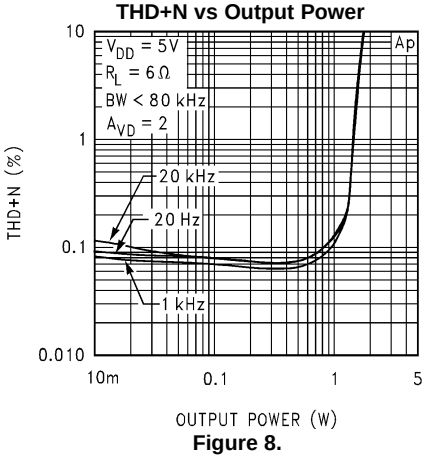


Figure 8.

THD+N vs Output Power

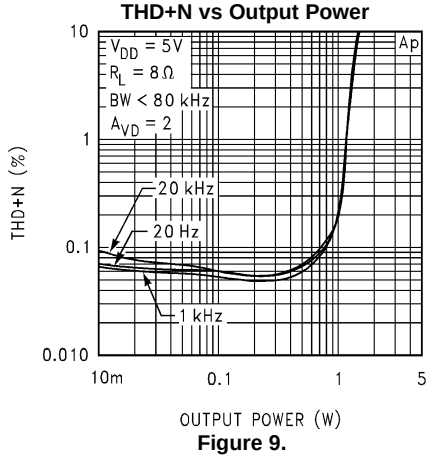


Figure 9.

Typical Performance Characteristics (continued)

Output Power vs Supply Voltage

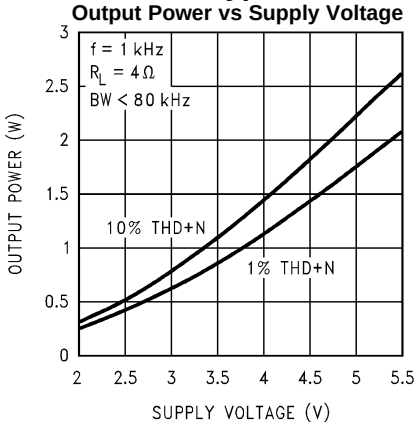


Figure 10.

Output Power vs Supply Voltage

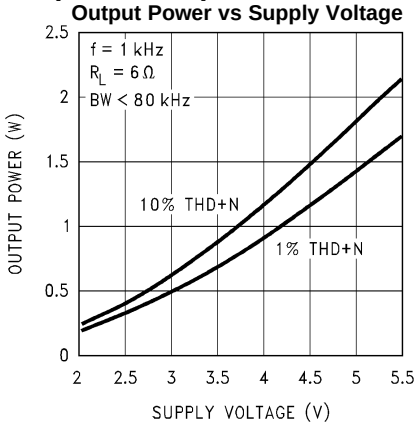


Figure 11.

Output Power vs Supply Voltage

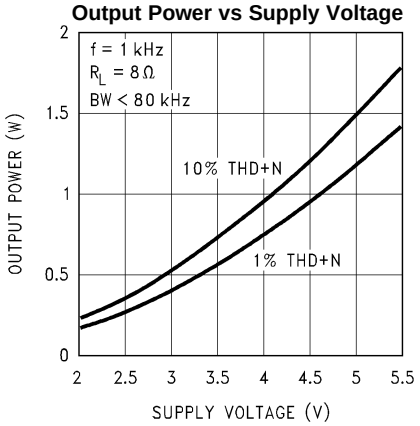


Figure 12.

Output Power vs Supply Voltage

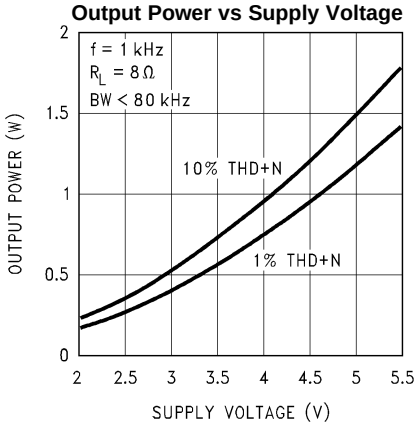


Figure 13.

Output Power vs Load Resistance

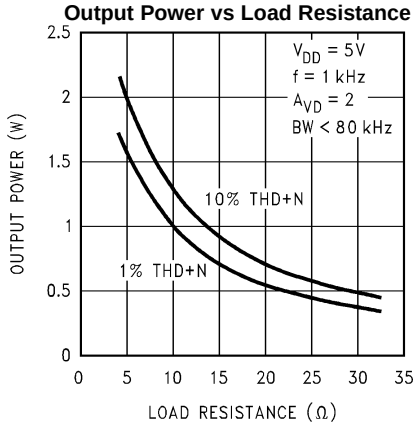


Figure 14.

Power Dissipation vs Output Power

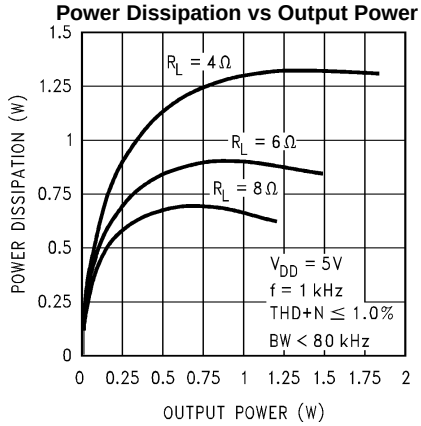


Figure 15.

Typical Performance Characteristics (continued)

Power Derating Curve

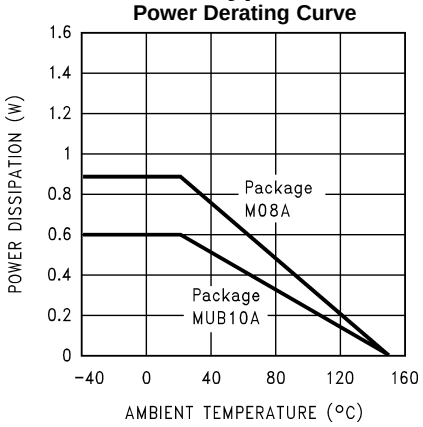


Figure 16.

Clipping Voltage vs Supply Voltage

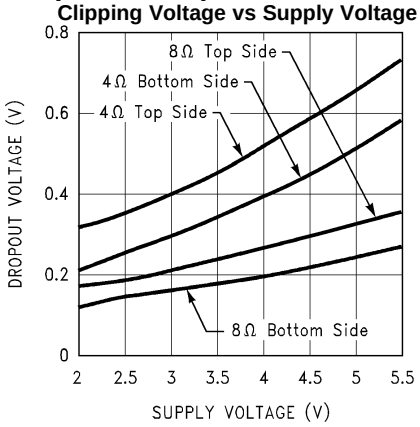


Figure 17.

Noise Floor

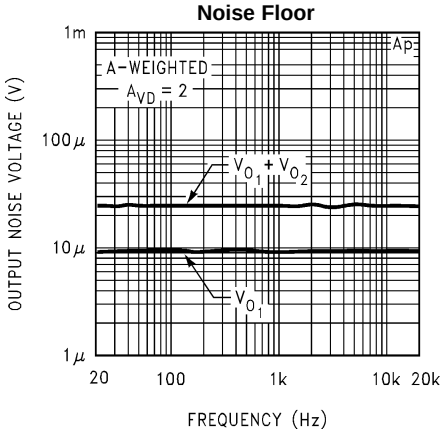


Figure 18.

Frequency Response vs Input Capacitor Size

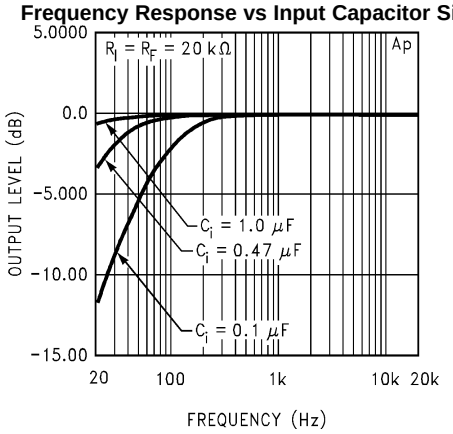


Figure 19.

Power Supply Rejection Ratio

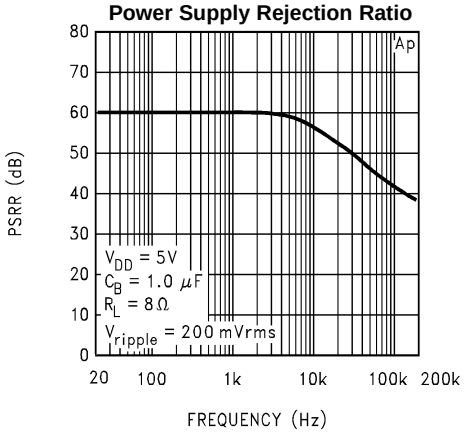


Figure 20.

Open Loop Frequency Response

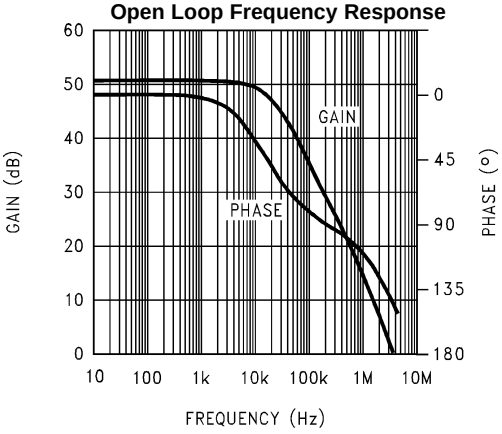


Figure 21.

Typical Performance Characteristics (continued)

Supply Current vs Supply Voltage

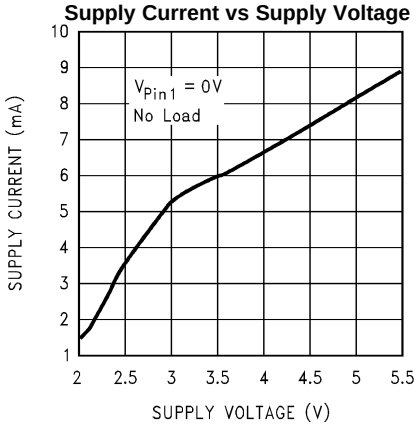


Figure 22.

Supply Current vs Shutdown Voltage
LM4876 @ VDD = 5/3.3/2.6Vdc

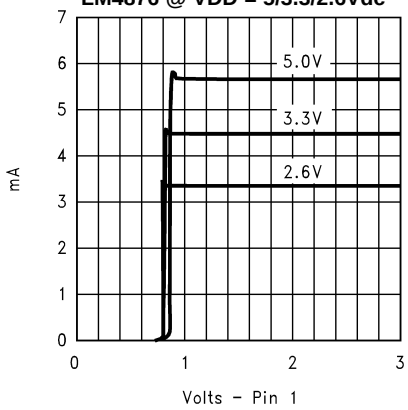


Figure 23.

APPLICATION INFORMATION

BRIDGE CONFIGURATION EXPLANATION

As shown in Figure 1, the LM4876 consists of two operational amplifiers. External resistors R_f and R_i set the closed-loop gain of Amp1, whereas two internal 40kΩ resistors set Amp2's gain at -1. The LM4876 drives a load, such as a speaker, connected between the two amplifier outputs, V_o1 and V_o2 .

Figure 1 shows that the Amp1 output serves as the Amp2 input, which results in both amplifiers producing signals identical in magnitude, but 180° out of phase. Taking advantage of this phase difference, a load is placed between V_o1 and V_o2 and driven differentially (commonly referred to as "bridge mode"). This results in a differential gain of

$$A_{VD} = 2 * (R_f/R_i) \quad (1)$$

Bridge mode is different from single-ended amplifiers that drive loads connected between a single amplifier's output and ground. For a given supply voltage, bridge mode has a distinct advantage over the single-ended configuration: its differential output doubles the voltage swing across the load. This results in four times the output power when compared to a single-ended amplifier under the same conditions. This increase in attainable output power assumes that the amplifier is not current limited or that the output signal is not clipped. To ensure minimum output signal clipping when choosing an amplifier's closed-loop gain, refer to the AUDIO POWER AMPLIFIER DESIGN section.

Another advantage of the differential bridge output is no net DC voltage across the load. This results from biasing V_o1 and V_o2 at half-supply. This eliminates the coupling capacitor that single supply, single-ended amplifiers require. Eliminating an output coupling capacitor in a single-ended configuration forces a single-supply amplifier's half-supply bias voltage across the load. The current flow created by the half-supply bias voltage increases internal IC power dissipation and may permanently damage loads such as speakers.

POWER DISSIPATION

Power dissipation is a major concern when designing a successful bridged or single-ended amplifier. Equation 2 states the maximum power dissipation point for a single-ended amplifier operating at a given supply voltage and driving a specified output load.

$$P_{DMAX} = (V_{DD})^2 /(2\pi^2 R_L) \text{ Single-Ended} \quad (2)$$

However, a direct consequence of the increased power delivered to the load by a bridge amplifier is higher internal power dissipation for the same conditions.

The LM4876 has two operational amplifiers in one package and the maximum internal power dissipation is four times that of a single-ended amplifier. Equation 3 states the maximum power dissipation for a bridge amplifier. However, even with this substantial increase in power dissipation, the LM4876 does not require heatsinking. From Equation 3, assuming a 5V power supply and an 8Ω load, the maximum power dissipation point is 633mW.

$$P_{DMAX} = 4*(V_{DD})^2 /(2\pi^2 R_L) \text{ Bridge Mode} \quad (3)$$

The maximum power dissipation point given by Equation 3 must not exceed the power dissipation given by Equation 4:

$$P_{DMAX} = (T_{JMAX} - T_A) /\theta_{JA} \quad (4)$$

The LM4876's T_{JMAX} = 150°C. In the D package, the LM4876's θ_{JA} is 140°C/W. At any given ambient temperature T_A, use Equation 4 to find the maximum internal power dissipation supported by the IC packaging. Rearranging Equation 4 results in Equation 5. This equation gives the maximum ambient temperature that still allows maximum power dissipation without violating the LM4876's maximum junction temperature.

$$T_A = T_{JMAX} - P_{DMAX} \theta_{JA} \quad (5)$$

For a typical application with a 5V power supply and an 8W load, the maximum ambient temperature that allows maximum power dissipation without exceeding the maximum junction temperature is approximately 61°C.

$$T_{JMAX} = P_{DMAX} \theta_{JA} + T_A \quad (6)$$

For the VSSOP10A package, θ_{JA} = 210°C/W. Equation 6 shows that T_{JMAX} , for the VSSOP10 package, is 158°C for an ambient temperature of 25°C and using the same 5V power supply and an 8Ω load. This violates the LM4876's 150°C maximum junction temperature when using the VSSOP10A package. Reduce the junction temperature by reducing the power supply voltage or increasing the load resistance. Further, allowance should be made for increased ambient temperatures. To achieve the same 61°C maximum ambient temperature found for the SOIC8 package, the VSSOP10 packaged part should operate on a 4.1V supply voltage when driving an 8Ω load. Alternatively, a 5V supply can be used when driving a load with a minimum resistance of 12Ω for the same 61°C maximum ambient temperature.

Fully charged Li-ion batteries typically supply 4.3V to portable applications such as cell phones. This supply voltage allows the LM4876 to drive loads with a minimum resistance of 9Ω without violating the maximum junction temperature when the maximum ambient temperature is 61°C.

The above examples assume that a device is a surface mount part operating around the maximum power dissipation point. Since internal power dissipation is a function of output power, higher ambient temperatures are allowed as output power or duty cycle decreases.

If the result of Equation 3 is greater than that of Equation 4, then decrease the supply voltage, increase the load impedance, or reduce the ambient temperature. If these measures are insufficient, a heat sink can be added to reduce θ_{JA}. The heat sink can be created using additional copper area around the package, with connections to the ground pin(s), supply pin and amplifier output pins. When adding a heat sink, the θ_{JA} is the sum of θ_{JC}, θ_{CS}, and θ_{SA}. (θ_{JC} is the junction-to-case thermal impedance, θ_{CS} is the case-to-sink thermal impedance, and θ_{SA} is the sink-to-ambient thermal impedance.) Refer to the Typical Performance Characteristics curves for power dissipation information at lower output power levels.

POWER SUPPLY BYPASSING

As with any power amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection. Applications that employ a 5V regulator typically use a 10µF in parallel with a 0.1µF filter capacitors to stabilize the regulator's output, reduce noise on the supply line, and improve the supply's transient response. However, their presence does not eliminate the need for local bypass capacitance at the LM4876's supply pins. Keep the length of leads and traces that connect capacitors between the LM4876's power supply pin and ground as short as possible. Connecting a 1µF capacitor between the BYPASS pin and ground improves the internal bias voltage's stability and improves the amplifier's PSRR. The PSRR improvements increase as the bypass pin capacitor value increases. Too large, however, and the amplifier's click and pop performance can be compromised. The selection of bypass capacitor values, especially C_B, depends on desired PSRR requirements, click and pop performance (as explained in the section, SELECTING PROPER EXTERNAL COMPONENTS), system cost, and size constraints.

MICRO-POWER SHUTDOWN

The voltage applied to the $\overline{\text{SHUTDOWN}}$ pin controls the LM4876's shutdown function. Activate micro-power shutdown by applying a voltage below 400mV to the $\overline{\text{SHUTDOWN}}$ pin. When active, the LM4876's micro-power shutdown feature turns off the amplifier's bias circuitry, reducing the supply current. Though the LM4876 is in shutdown when 400mV is applied to the $\overline{\text{SHUTDOWN}}$ pin, the supply current may be higher than 0.01µA (typ) shutdown current. Therefore, for the lowest supply current during shutdown, connect the $\overline{\text{SHUTDOWN}}$ pin to ground. The relationship between the supply voltage, the shutdown current, and the voltage applied to the $\overline{\text{SHUTDOWN}}$ pin is shown in Typical Performance Characteristics curves.

There are a few ways to control the micro-power shutdown. These include using a single-pole, single-throw switch, a microprocessor, or a microcontroller. When using a switch, connect an external pull-down resistor between the $\overline{\text{SHUTDOWN}}$ pin and GND. Connect the switch between the $\overline{\text{SHUTDOWN}}$ pin and V_{CC}. Select normal amplifier operation by closing the switch. Opening the switch connects the $\overline{\text{SHUTDOWN}}$ pin to GND through the pull-down resistor, activating micro-power shutdown. The switch and resistor ensure that the $\overline{\text{SHUTDOWN}}$ pin will not float. This prevents unwanted state changes. In a system with a microprocessor or a microcontroller, use a digital output to apply the control voltage to the $\overline{\text{SHUTDOWN}}$ pin. Driving the $\overline{\text{SHUTDOWN}}$ pin with active circuitry eliminates the pull down resistor.

SELECTING PROPER EXTERNAL COMPONENTS

Optimizing the LM4876's performance requires properly selecting external components. Though the LM4876 operates well when using external components with wide tolerances, best performance is achieved by optimizing component values.

The LM4876 is unity-gain stable, giving a designer maximum design flexibility. The gain should be set to no more than a given application requires. This allows the amplifier to achieve minimum THD+N and maximum signal-to-noise ratio. These parameters are compromised as the closed-loop gain increases. However, low gain demands input signals with greater voltage swings to achieve maximum output power. Fortunately, many signal sources such as audio CODECs have outputs of $1V_{RMS}$ ($2.83V_{P-P}$). Please refer to the AUDIO POWER AMPLIFIER DESIGN section for more information on selecting the proper gain.

Input Capacitor Value Selection

Amplifying the lowest audio frequencies requires high value input coupling capacitor (C_i in Figure 1). A high value capacitor can be expensive and may compromise space efficiency in portable designs. In many cases, however, the speakers used in portable systems, whether internal or external, have little ability to reproduce signals below 150 Hz. Applications using speakers with this limited low frequency response reap little improvement by using a large input capacitor.

Besides affecting system cost and size, C_i also affects the LM4876's click and pop performance. When the supply voltage is first applied, a transient (pop) is created as the charge on the input capacitor changes from zero to a quiescent state. The magnitude of the pop is directly proportional to the input capacitor's size. Higher value capacitors need more time to reach a quiescent DC voltage (usually $V_{CC}/2$) when charged with a fixed current. The amplifier's output charges the input capacitor through the feedback resistor, R_f. Thus, pops can be minimized by selecting an input capacitor value that is no higher than necessary to meet the desired -3dB frequency.

As shown in Figure 1, the input resistor (R_I) and the input capacitor, C_I produce a -3dB high pass filter cutoff frequency that is found using Equation 7.

$$f_{-3dB} = 2\pi R_{IN} C_I \quad (7)$$

As an example when using a speaker with a low frequency limit of 150Hz, Equation 7 gives a value of C_i equal to 0.1µF. The 0.22µF C_i shown in Figure 1 allows for a speaker whose response extends down to 75Hz.

Bypass Capacitor Value Selection

Besides minimizing the input capacitor size, careful consideration should be paid to value of, C_B, the capacitor connected to the BYPASS pin. Since C_B determines how fast the LM4876 settles to quiescent operation, its value is critical when minimizing turn-on pops. The slower the LM4876's outputs ramp to their quiescent DC voltage (nominally 1/2 V_{DD}), the smaller the turn-on pop. Choosing C_B equal to 1.0µF along with a small value of C_i (in the range of 0.1µF to 0.39µF), produces a click-less and pop-less shutdown function. As discussed above, choosing C_i as small as possible helps minimize clicks and pops.

AUDIO POWER AMPLIFIER DESIGN

Audio Amplifier Design: Driving 1W into an 8Ω Load

The following are the desired operational parameters:

Power Output	$1W_{RMS}$
Load Impedance	8Ω
Input Level	$1V_{RMS}$
Input Impedance	20kΩ
Bandwidth	100Hz–20kHz ± 0.25dB

The design begins by specifying the minimum supply voltage necessary to obtain the specified output power. One way to find the minimum supply voltage is to use the Output Power vs Supply Voltage curve in the Typical Performance Characteristics section. Another way, using Equation 8, is to calculate the peak output voltage necessary to achieve the desired output power for a given load impedance. To account for the amplifier's dropout voltage, two additional voltages, based on the Dropout Voltage vs Supply Voltage in the Typical Performance Characteristics curves, must be added to the result obtained by Equation 8. This results in Equation 9.

$$V_{OUTPEAK} = \sqrt{(2R_L P_O)} \quad (8)$$

$$V_{CC} \geq (V_{OUTPEAK} + (V_{ODTOP} + V_{ODBOT})) \quad (9)$$

The Output Power vs Supply Voltage graph for an 8Ω load indicates a minimum supply voltage of 4.6V. This is easily met by the commonly used 5V supply voltage. The additional voltage creates the benefit of headroom, allowing the LM4876 to produce peak output power in excess of 1W without clipping or other audible distortion. The choice of supply voltage must also not create a violation of maximum power dissipation as explained above in the POWER DISSIPATION section.

After satisfying the LM4876's power dissipation requirements, the minimum differential gain is found using Equation 10.

$$\sqrt{(P_O R_L)/(V_{IN})} = V_{ORMS}/V_{INRMS} \quad (10)$$

Thus, a minimum gain of 2.83 allows the LM4876's to reach full output swing and maintain low noise and THD+N performance. For this example, let A_{VD} = 3.

The amplifier's overall gain is set using the input (R_i) and feedback (R_f) resistors. With the desired input impedance set at 20kΩ, the feedback resistor is found using Equation 11.

$$R_f/R_i = A_{VD}/2$$

where

- The value of R_f is 30kΩ. (11)

The last step in this design example is setting the amplifier's -3dB low frequency bandwidth. To achieve the desired ±0.25dB pass band magnitude variation limit, the low frequency response must extend to at least one-fifth the lower bandwidth limit and the high frequency response must extend to at least five times the upper bandwidth limit. The results is an

f_L = 100 Hz/5 = 20Hz

and an

F_H = 20 kHz*5 = 100kHz

As mentioned in the External Components Description section, R_i and C_i create a highpass filter that sets the amplifier's lower bandpass frequency limit. Find the coupling capacitor's value using Equation 12.

$$Ci \geq 1/(2\pi R i f_L) \quad (12)$$

The result is

1/(2π*20kΩ*20Hz) = 0.398µF.

Use a 0.39µF capacitor, the closest standard value.

The product of the desired high frequency cutoff (100kHz in this example) and the differential gain, A_{VD}, determines the upper passband response limit. With A_{VD} = 3 and f_H = 100kHz, the closed-loop gain bandwidth product (GBWP) is 150kHz. This is less than the LM4876's 4MHz GBWP. With this margin, the amplifier can be used in designs that require more differential gain and avoid performance-restricting bandwidth limitations.

REVISION HISTORY

Changes from Revision D (May 2013) to Revision E	Page
• Changed layout of National Data Sheet to TI format	11

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM4876M/NOPB	ACTIVE	SOIC	D	8	95	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LM4876M	Samples
LM4876MM/NOPB	ACTIVE	VSSOP	DGS	10	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	G76	Samples
LM4876MX/NOPB	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LM4876M	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

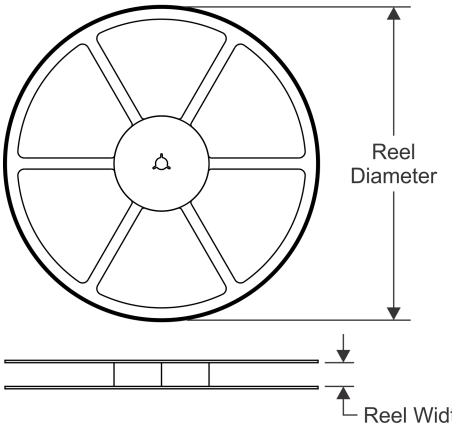
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

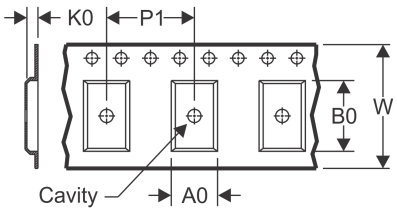
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

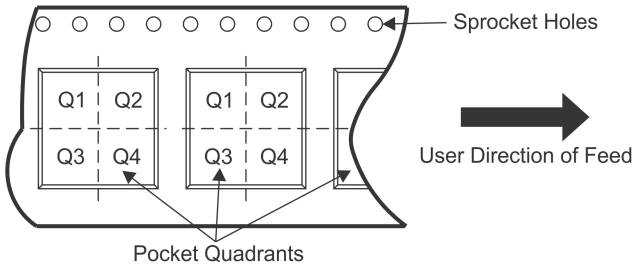


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

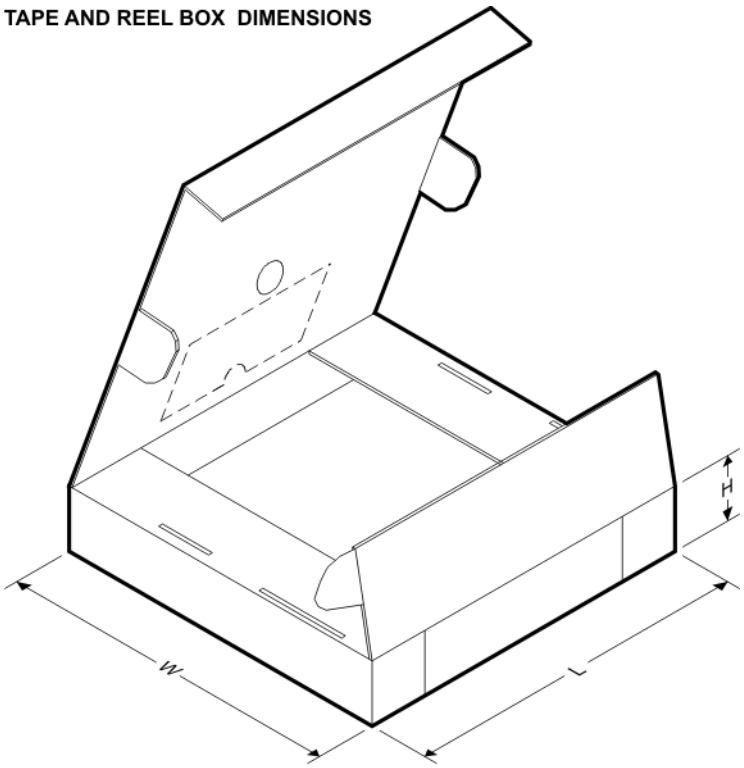
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM4876MM/NOPB	VSSOP	DGS	10	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM4876MX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

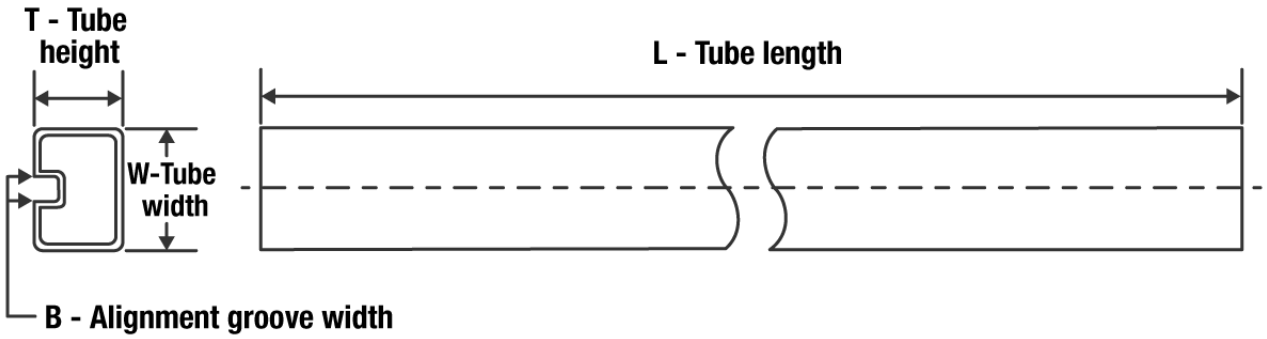
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM4876MM/NOPB	VSSOP	DGS	10	1000	208.0	191.0	35.0
LM4876MX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

TUBE



*All dimensions are nominal

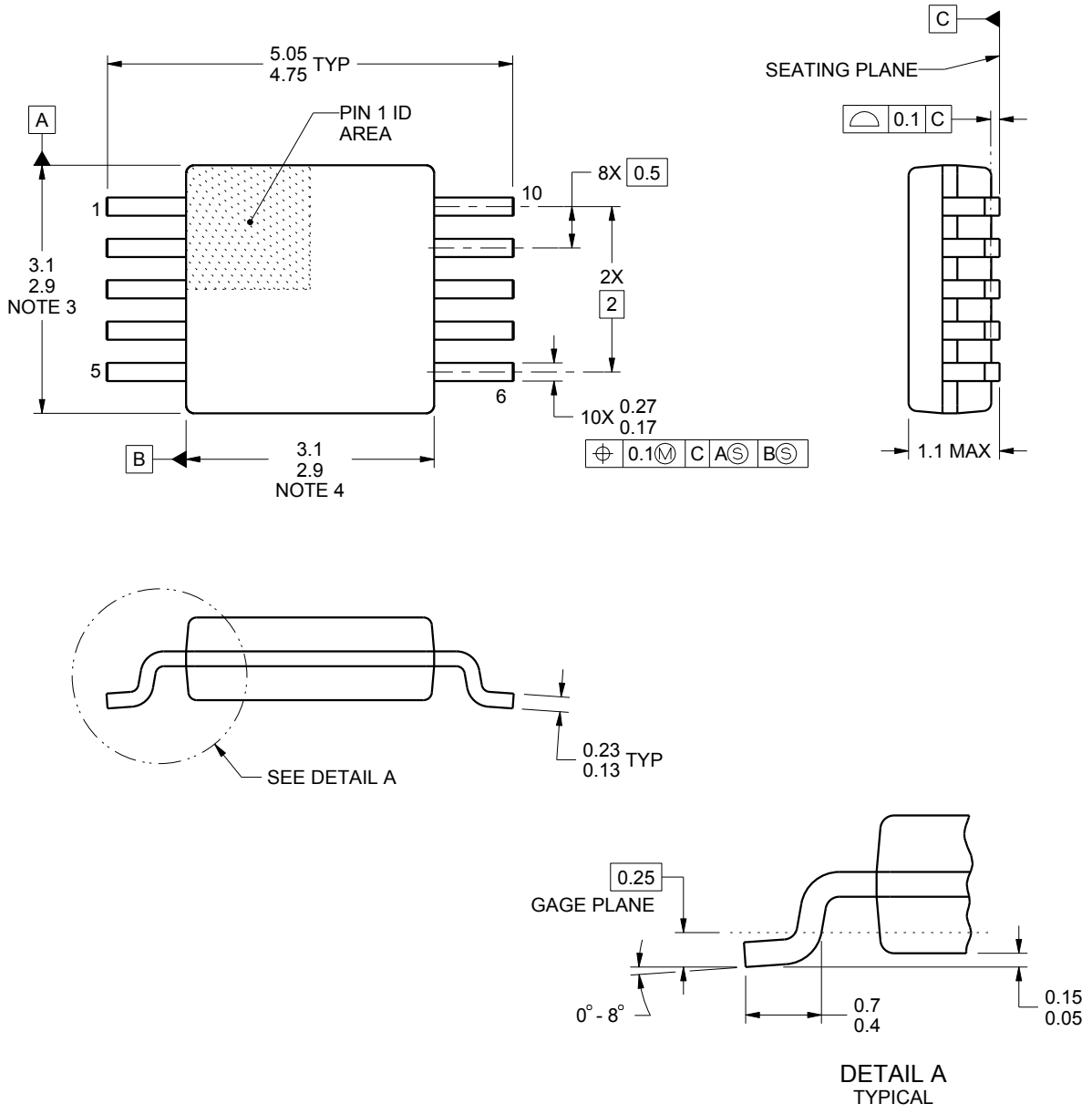
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM4876M/NOPB	D	SOIC	8	95	495	8	4064	3.05

PACKAGE OUTLINE

DGS0010A

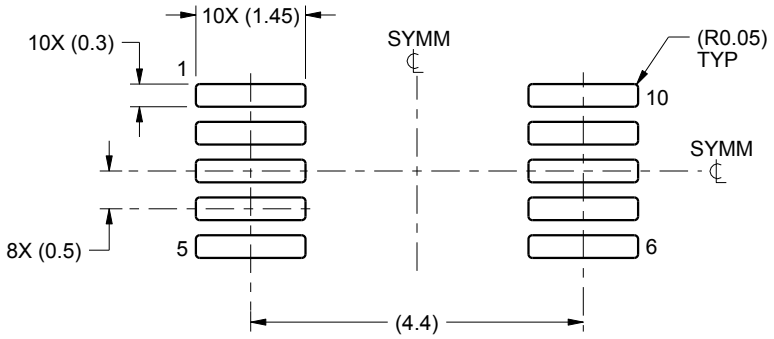
VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

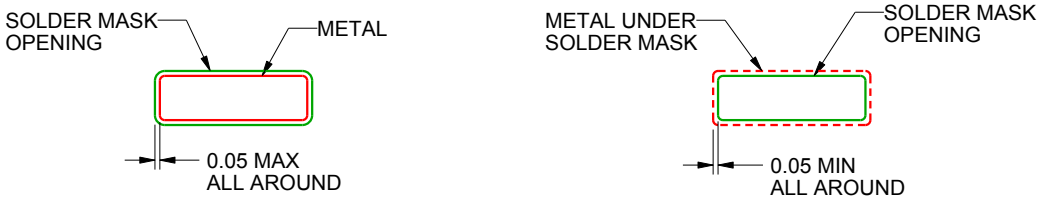


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X

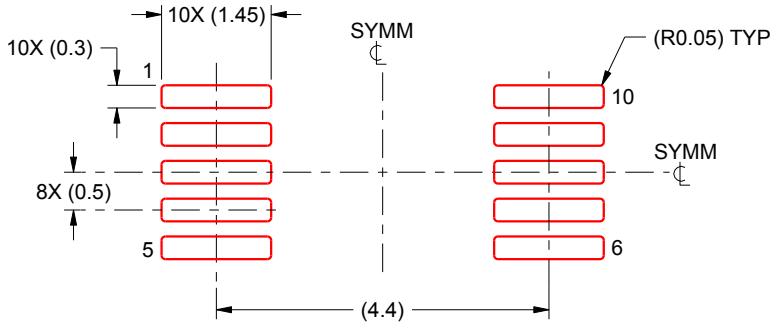


SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

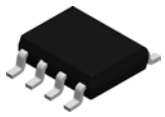


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

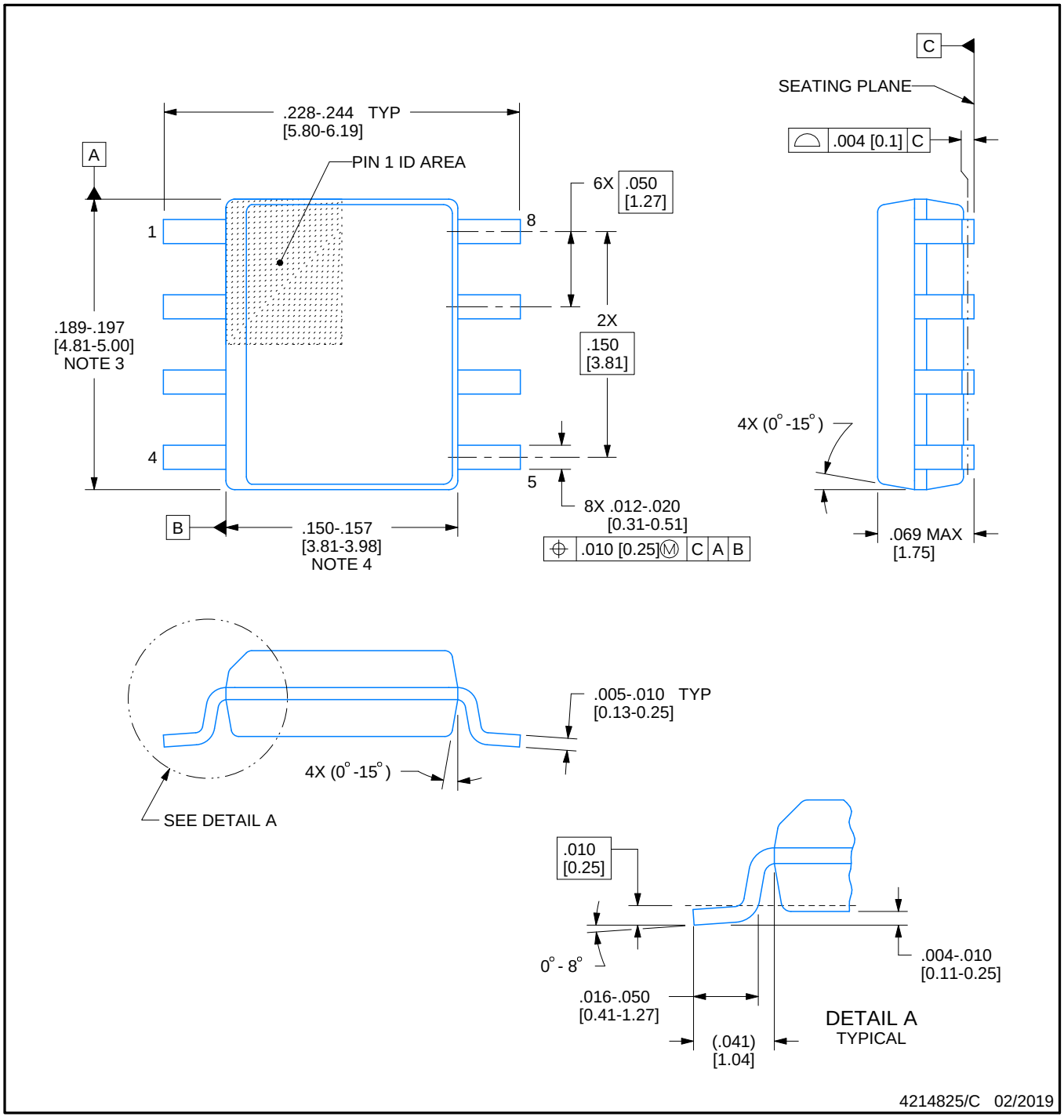


PACKAGE OUTLINE

D0008A

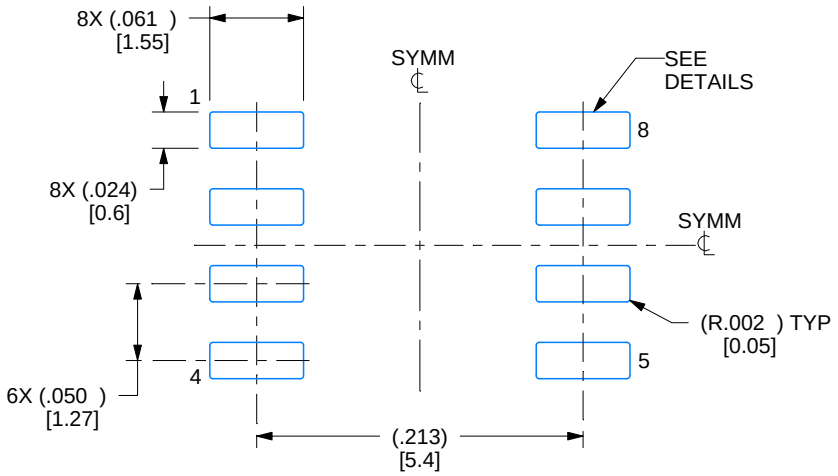
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

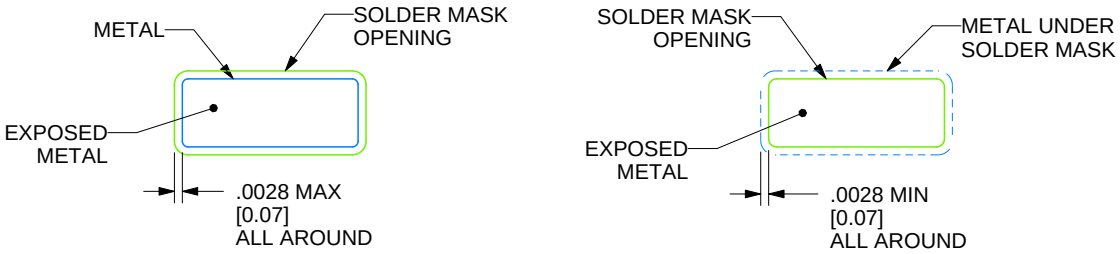


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

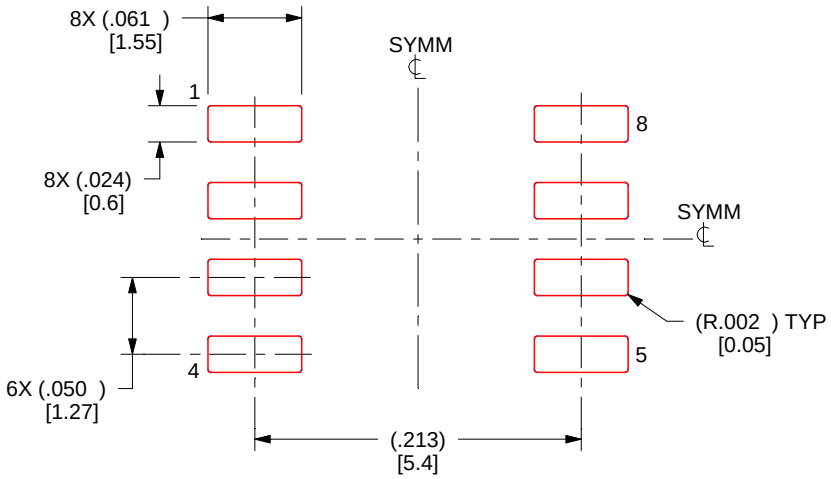
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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