

## LM2767 Switched Capacitor Voltage Converter

### 1 Features

- Doubles input supply voltage
- SOT-23 5-pin package
- 20- $\Omega$  typical output impedance
- 96% typical conversion efficiency at 15 mA

### 2 Applications

- [Cellular phones](#)
- [Pagers](#)
- PDAs, organizers
- Operational amplifier power suppliers
- Interface power suppliers
- [Handheld instruments](#)

### 3 Description

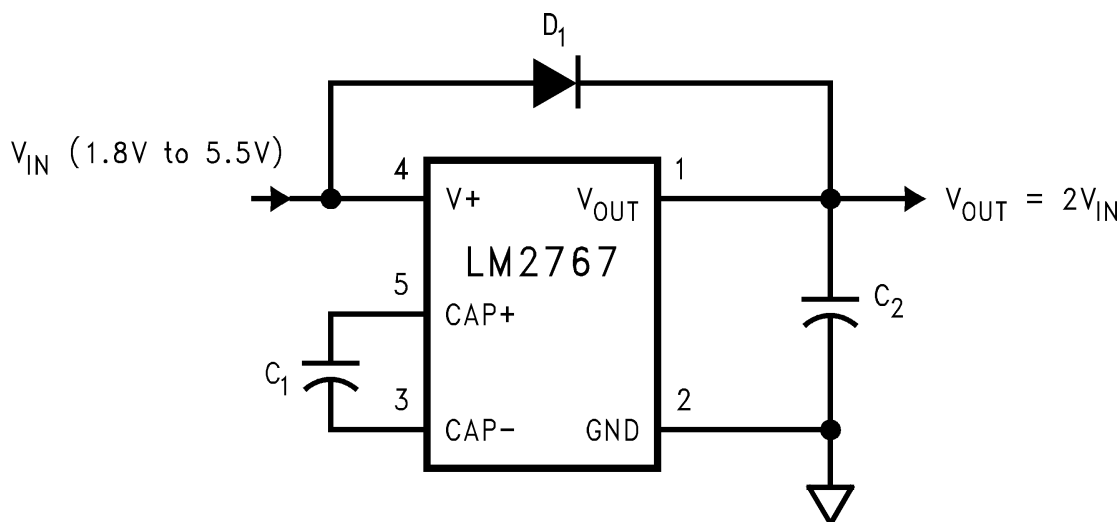
The LM2767 CMOS charge-pump voltage converter operates as a voltage doubler for an input voltage in the range of 1.8 V to 5.5 V. Two low-cost capacitors and a diode are used in this circuit to provide at least 15 mA of output current.

The LM2767 operates at 11-kHz switching frequency to avoid audio voice-band interference. With an operating current of only 40  $\mu$ A (operating efficiency greater than 90% with most loads), the LM2767 provides ideal performance for battery-powered systems. The device is manufactured in a 5-pin SOT-23 package.

#### Device Information

PART NUMBER	PACKAGE <sup>(1)</sup>	BODY SIZE (NOM)
LM2767	SOT-23 (5)	2.90 mm $\times$ 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Typical Application



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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

### Changes from Revision D (August 2015) to Revision E (January 2022) Page

- Updated the numbering format for tables, figures, and cross-references throughout the document. .... 1
- Added additional I<sub>L</sub> specification test condition ..... 5

### Changes from Revision C (May 2013) to Revision D (August 2015) Page

- Added *Device Information* and *Pin Configuration and Functions* sections, ESD Rating table, *Feature Description*, *Device Functional Modes*, *Application and Implementation*, *Power Supply Recommendations*, *Layout*, *Device and Documentation Support*, and *Mechanical, Packaging, and Orderable Information* sections ..... 1

## 5 Pin Configuration and Functions

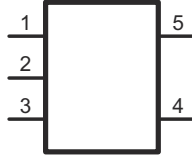


Figure 5-1. DBV Package 5-Pin SOT-23 Top View

Table 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NUMBER	NAME		
1	VOUT	Power	Positive voltage output.
2	GND	Ground	Power supply ground input.
3	CAP-	Power	Connect this pin to the negative terminal of the charge-pump capacitor.
4	V+	Power	Power supply positive voltage input.
5	CAP+	Power	Connect this pin to the positive terminal of the charge-pump capacitor.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1) (2)</sup>

	MIN	MAX	UNIT
Supply voltage (V+ to GND, or V+ to V <sub>OUT</sub> )		5.8	V
V <sub>OUT</sub> continuous output current		30	mA
Output short-circuit duration to GND <sup>(3)</sup>		1	sec
Continuous power dissipation (T <sub>A</sub> = 25°C) <sup>(4)</sup>		400	mW
T <sub>JMax</sub> <sup>(4)</sup>		150	°C
Storage temperature, T <sub>stg</sub>	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) If Military/Aerospace specified devices are required, contact the TI Sales Office/ Distributors for availability and specifications.
- (3) V<sub>OUT</sub> may be shorted to GND for one second without damage. For temperatures above 85°C, V<sub>OUT</sub> must not be shorted to GND or device may be damaged.
- (4) The maximum allowable power dissipation is calculated by using  $P_{DMax} = (T_{JMax} - T_A)/R_{\theta JA}$ , where T<sub>JMax</sub> is the maximum junction temperature, T<sub>A</sub> is the ambient temperature, and R<sub>θJA</sub> is the junction-to-ambient thermal resistance of the specified package.

### 6.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub> Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V
	Machine model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±200	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Junction temperature	-40		100	°C
Ambient temperature	-40		85	°C
Lead temperature (soldering, 10 sec.)			240	°C

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		LM2767	UNIT
		DBV (SOT-23)	
		5 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	210	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## 6.5 Electrical Characteristics

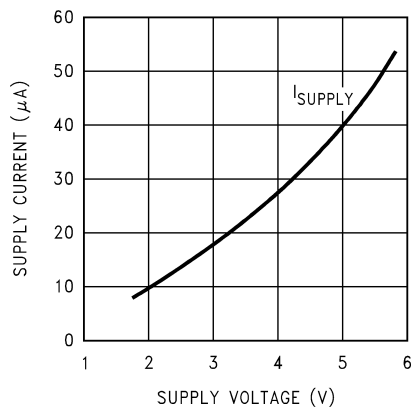
Unless otherwise specified, typical limits are for  $T_J = 25^\circ\text{C}$ , minimum and maximum limits apply over the full operating temperature range:  $V_+ = 5\text{ V}$ ,  $C_1 = C_2 = 10\ \mu\text{F}$ .<sup>(1)</sup>

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_+$	Supply voltage		1.8		5.5	V
$I_Q$	Supply current	No load		40	90	$\mu\text{A}$
$I_L$	Output current	$2.5\text{ V} \leq V_+ \leq 5.5\text{ V}$	15			mA
		$1.8\text{ V} \leq V_+ < 2.5\text{ V}$	10			mA
$R_{OUT}$	Output resistance <sup>(2)</sup>	$I_L = 15\text{ mA}$		20	40	$\Omega$
$f_{OSC}$	Oscillator frequency	See <sup>(3)</sup>	8	22	50	kHz
$f_{SW}$	Switching frequency	See <sup>(3)</sup>	4	11	25	kHz
$P_{EFF}$	Power efficiency	$R_L$ (5 k $\Omega$ ) between GND and OUT	98%			
		$I_L = 15\text{ mA}$ to GND	96%			
$V_{OEFF}$	Voltage conversion efficiency	No load	99.96%			

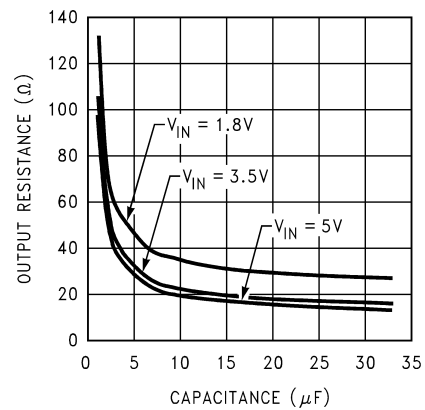
- (1) In the test circuit, capacitors  $C_1$  and  $C_2$  are 10- $\mu\text{F}$ , 0.3- $\Omega$  maximum ESR capacitors. Capacitors with higher ESR may increase output resistance, and reduce output voltage and efficiency.
- (2) Specified output resistance includes internal switch resistance and capacitor ESR. See the details in [Section 9](#) for positive voltage doubler.
- (3) The output switches operate at one half of the oscillator frequency,  $f_{OSC} = 2 \times f_{SW}$ .

## 6.6 Typical Characteristics

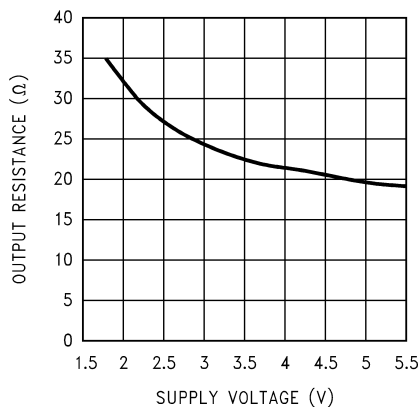
(Circuit of [Figure 7-1](#),  $V_{IN} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$  unless otherwise specified).



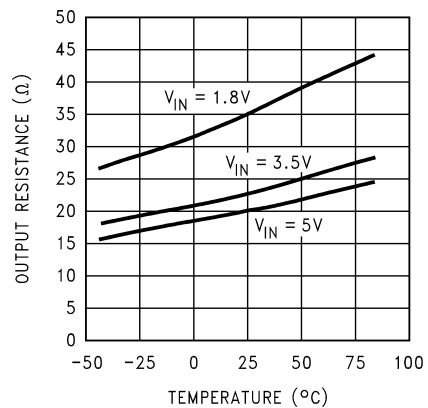
**Figure 6-1. Supply Current vs Supply Voltage**



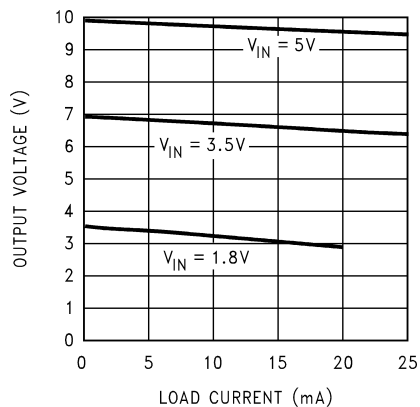
**Figure 6-2. Output Resistance vs Capacitance**



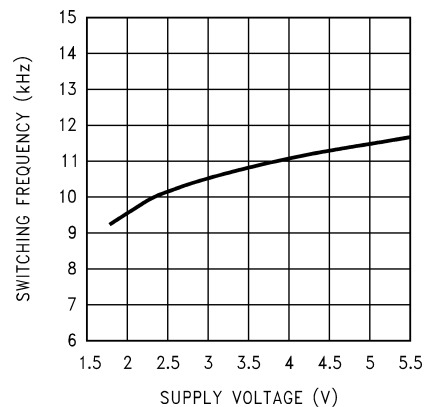
**Figure 6-3. Output Resistance vs Supply Voltage**



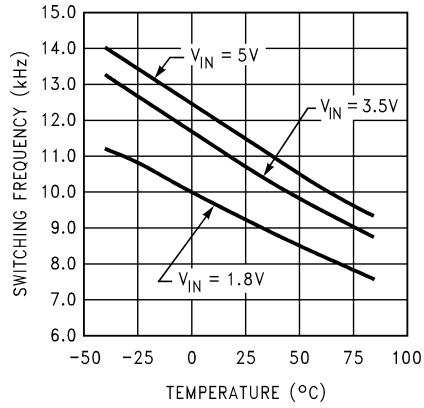
**Figure 6-4. Output Resistance vs Temperature**



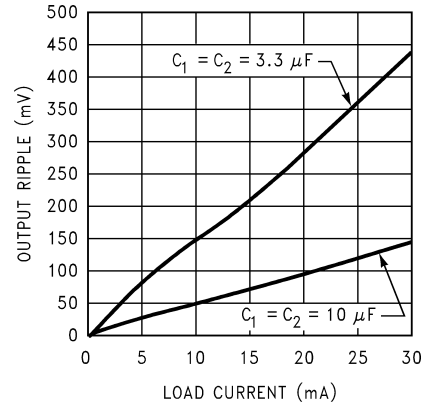
**Figure 6-5. Output Voltage vs Load Current**



**Figure 6-6. Switching Frequency vs Supply Voltage**



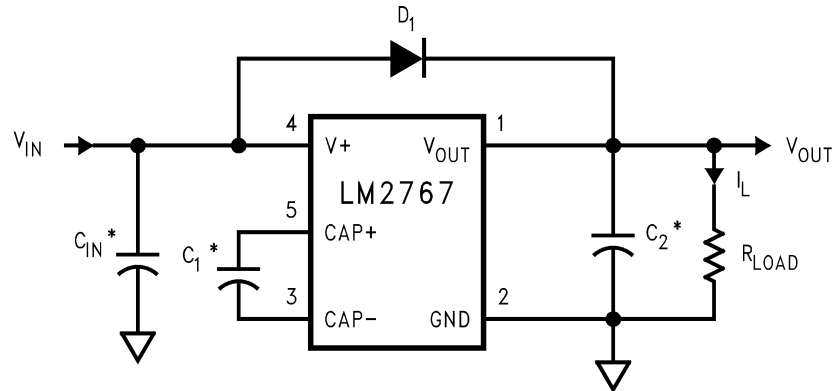
**Figure 6-7. Switching Frequency vs Temperature**



**Figure 6-8. Output Ripple vs Load Current**

## 7 Parameter Measurement Information

### 7.1 Test Circuit



\*  $C_{IN}$ ,  $C_1$ , and  $C_2$  are  $10\ \mu\text{F}$  OS-CON capacitors.

**Figure 7-1. LM2767 Test Circuit**

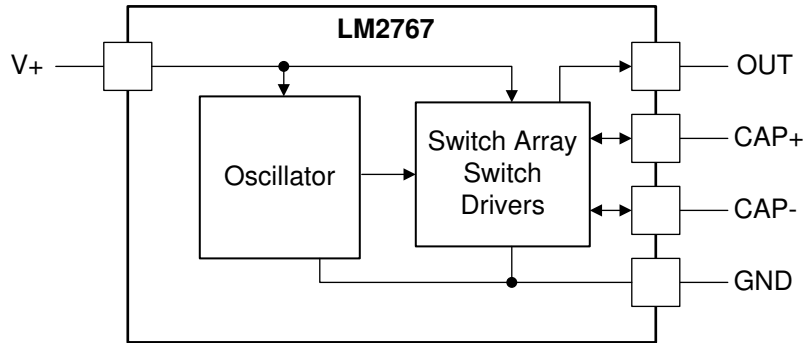


## 8 Detailed Description

### 8.1 Overview

The LM2767 CMOS charge-pump voltage converter operates as a voltage doubler for an input voltage in the range of 1.8 V to 5.5 V. Two low-cost capacitors and a diode (needed during start-up) are used in this circuit.

### 8.2 Functional Block Diagram



### 8.3 Feature Description

The LM2767 contains four large CMOS switches which are switched in a sequence to double the input supply voltage. Energy transfer and storage are provided by external capacitors. [Figure 9-2](#) illustrates the voltage conversion scheme. When  $S_2$  and  $S_4$  are closed,  $C_1$  charges to the supply voltage  $V+$ . During this time interval, switches  $S_1$  and  $S_3$  are open. In the next time interval,  $S_2$  and  $S_4$  are open; at the same time,  $S_1$  and  $S_3$  are closed, the sum of the input voltage  $V+$  and the voltage across  $C_1$  gives the  $2V+$  output voltage when there is no load. The output voltage drop when a load is added is determined by the parasitic resistance ( $R_{ds(on)}$  of the MOSFET switches and the ESR of the capacitors) and the charge transfer loss between capacitors. Details are discussed in [Section 9](#).

### 8.4 Device Functional Modes

The LM2767 is always enabled when power is applied to the  $V+$  pin ( $1.8\text{ V} \leq V_{IN} \leq 5.5\text{ V}$ ). To disable the part, power must be removed.

## 9 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 9.1 Application Information

The LM2767 provides a simple and efficient means of creating an output voltage level equal to twice that of the input voltage. Without the need of an inductor, the application solution size can be reduced versus the magnetic DC-DC converter solution.

### 9.2 Typical Application

The main application of the LM2767 is to double the input voltage. The range of the input supply voltage is 1.8 V to 5.5 V.

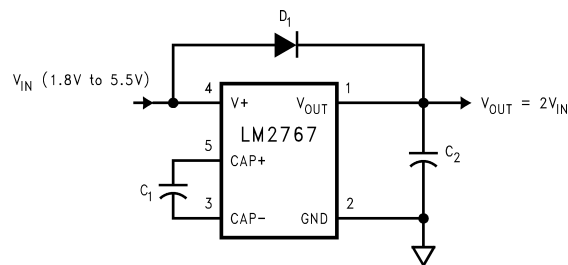


Figure 9-1. LM2767 Typical Application

#### 9.2.1 Design Requirements

For typical switched-capacitor voltage converter applications, use the parameters listed in [Table 9-1](#).

Table 9-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Minimum input voltage	1.8 to 5.5 V
Output current (minimum)	15 mA
Switching frequency	11 kHz (typical)

#### 9.2.2 Detailed Design Procedure

##### 9.2.2.1 Positive Voltage Doubler

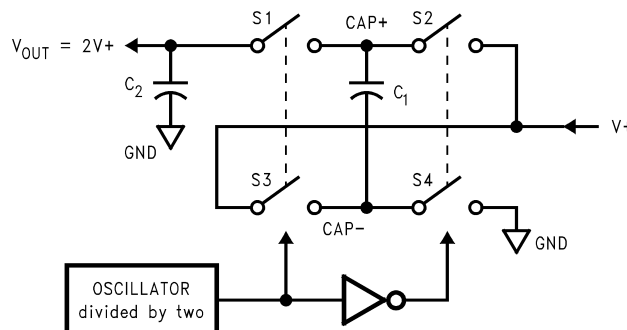


Figure 9-2. Voltage Doubling Principle

The output characteristics of this circuit can be approximated by an ideal voltage source in series with a resistance. The voltage source equals 2 V+. The output resistance  $R_{out}$  is a function of the ON resistance of the internal MOSFET switches, the oscillator frequency, and the capacitance and ESR of  $C_1$  and  $C_2$ . Because the switching current charging and discharging  $C_1$  is approximately twice the output current, the effect of the ESR of the pumping capacitor  $C_1$  is multiplied by four in the output resistance. The output capacitor  $C_2$  is charging and discharging at a current approximately equal to the output current, therefore, its ESR only counts once in the output resistance. A good approximation of  $R_{out}$  is:

$$R_{OUT} \cong 2R_{SW} + \frac{2}{f_{OSC} \times C_1} + 4ESR_{C1} + ESR_{C2} \quad (1)$$

where

- $R_{SW}$  is the sum of the ON resistance of the internal MOSFET switches shown in [Figure 9-2](#).

The peak-to-peak output voltage ripple is determined by the oscillator frequency as well as the capacitance and ESR of the output capacitor  $C_2$ :

$$V_{RIPPLE} = \frac{I_L}{f_{OSC} \times C_2} + 2 \times I_L \times ESR_{C2} \quad (2)$$

High capacitance, low ESR capacitors can reduce both the output resistance and the voltage ripple.

The Schottky diode  $D_1$  is only needed to protect the device from turning on its own parasitic diode and potentially latching up. During start-up,  $D_1$  also quickly charges up the output capacitor to  $V_{IN}$  minus the diode drop thereby decreasing the start-up time. Therefore, the Schottky diode  $D_1$  must have enough current carrying capability to charge the output capacitor at start-up, as well as a low forward voltage to prevent the internal parasitic diode from turning on. A Schottky diode like 1N5817 can be used for most applications. If the input voltage ramp is less than 10 V/ms, a smaller Schottky diode like MBR0520LT1 can be used to reduce the circuit size.

### 9.2.2.2 Capacitor Selection

As discussed in [Section 9.2.2.1](#), the output resistance and ripple voltage are dependent on the capacitance and ESR values of the external capacitors. The output voltage drop is the load current times the output resistance, and the power efficiency is

$$\eta = \frac{P_{OUT}}{P_{IN}} = \frac{I_L^2 R_L}{I_L^2 R_L + I_L^2 R_{OUT} + I_Q(V+)} \quad (3)$$

where

- $I_Q(V+)$  is the quiescent power loss of the device; and
- $I_L^2 R_{out}$  is the conversion loss associated with the switch on-resistance, the two external capacitors and their ESRs.

The selection of capacitors is based on the allowable voltage droop (which equals  $I_{out} R_{out}$ ), and the desired output voltage ripple. Low-ESR capacitors ([Table 9-2](#)) are recommended to maximize efficiency, reduce the output voltage drop and voltage ripple.

**Table 9-2. Low-ESR Capacitor Manufacturers**

MANUFACTURER	PHONE	WEBSITE	CAPACITOR TYPE
Nichicon Corp.	(847)-843-7500	<a href="http://www.nichicon.com">www.nichicon.com</a>	PL & PF series, through-hole aluminum electrolytic
AVX Corp.	(843)-448-9411	<a href="http://www.avxcorp.com">www.avxcorp.com</a>	TPS series, surface-mount tantalum
Sprague	(207)-324-4140	<a href="http://www.vishay.com">www.vishay.com</a>	593D, 594D, 595D series, surface-mount tantalum
Sanyo	(619)-661-6835	<a href="http://www.sanyovideo.com">www.sanyovideo.com</a>	OS-CON series, through-hole aluminum electrolytic
Murata	(800)-831-9172	<a href="http://www.murata.com">www.murata.com</a>	Ceramic chip capacitors
Taiyo Yuden	(800)-348-2496	<a href="http://www.t-yuden.com">www.t-yuden.com</a>	Ceramic chip capacitors

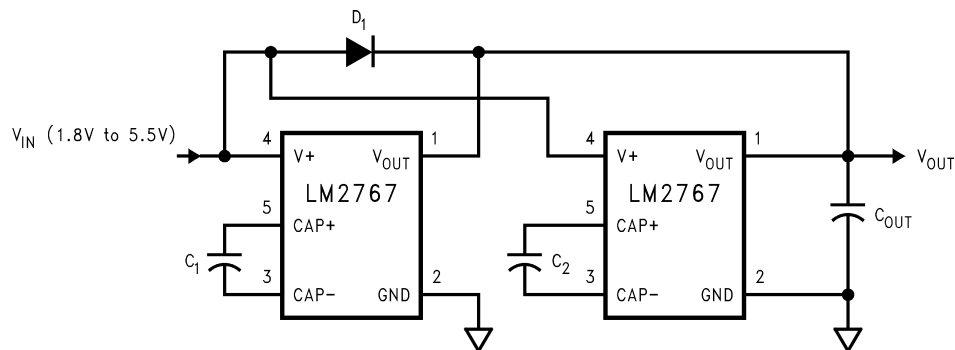
**Table 9-2. Low-ESR Capacitor Manufacturers (continued)**

MANUFACTURER	PHONE	WEBSITE	CAPACITOR TYPE
Tokin	(408)-432-8020	<a href="http://www.tokin.com">www.tokin.com</a>	Ceramic chip capacitors

### 9.2.2.3 Paralleling Devices

Any number of LM2767 devices can be paralleled to reduce the output resistance. Because there is no closed loop feedback, as found in regulated circuits, stable operation is assured. Each device must have its own pumping capacitor  $C_1$ , while only one output capacitor  $C_{OUT}$  is needed as shown in Figure 9-3. The composite output resistance is:

$$R_{OUT} = \frac{R_{OUT \text{ of each LM2767}}}{\text{Number of Devices}} \quad (4)$$

**Figure 9-3. Lowering Output Resistance by Paralleling Devices**

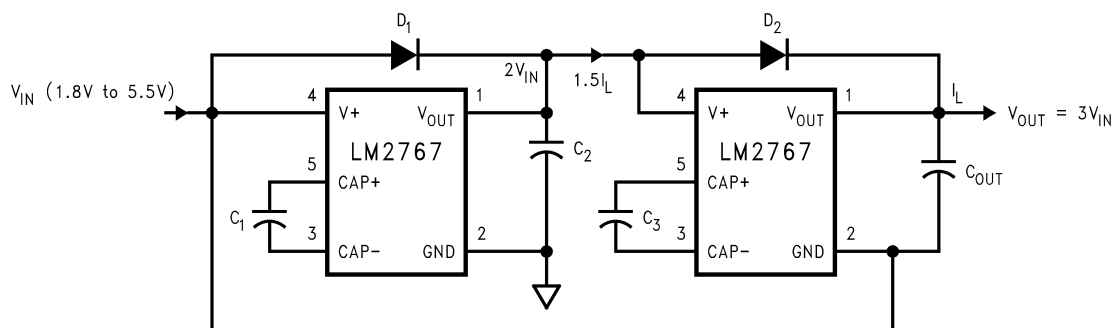
### 9.2.2.4 Cascading Devices

Cascading the several LM2767 devices is an easy way to produce a greater voltage (a two-stage cascade circuit is shown in Figure 9-4).

The effective output resistance is equal to the weighted sum of each individual device:

$$R_{OUT} = 1.5 R_{OUT\_1} + R_{OUT\_2} \quad (5)$$

Note that increasing the number of cascading stages is practically limited because it significantly reduces the efficiency, increases the output resistance and output voltage ripple.

**Figure 9-4. Increasing Output Voltage By Cascading Devices**

### 9.2.2.5 Regulating $V_{OUT}$

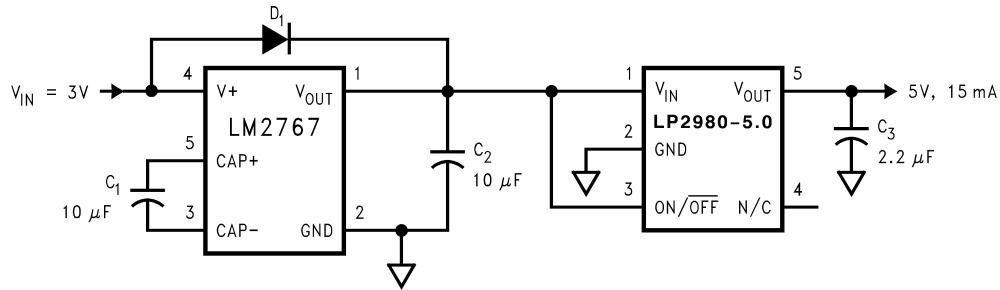
It is possible to regulate the output of the LM2767 by use of a low dropout regulator (such as LP2980-5.0). The whole converter is depicted in Figure 9-5.

A different output voltage is possible by use of LP2980-3.3, LP2980-3.0, or LP2980-ADJ.

The following conditions must be satisfied simultaneously for worst case design:

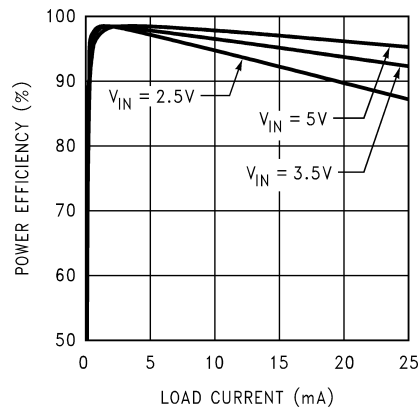
$$2V_{IN\_MIN} > V_{OUT\_MIN} + V_{DROD\_MAX} (LP2980) + I_{OUT\_MAX} \times R_{OUT\_MAX} \quad (6)$$

$$2V_{IN\_MAX} < V_{OUT\_MAX} + V_{DROD\_MIN} (LP2980) + I_{OUT\_MIN} \times R_{OUT\_MIN} \quad (7)$$



**Figure 9-5. Generate a Regulated 5-V From 3-V Input Voltage**

### 9.2.3 Application Curve



**Figure 9-6. Efficiency vs Load Current**

## 10 Power Supply Recommendations

The LM2767 is designed to operate from as an inverter over an input voltage supply range from 1.8 V and 5.5 V. This input supply must be well-regulated and capable to supply the required input current. If the input supply is located far from the device, additional bulk capacitance may be required in addition to the ceramic bypass capacitors.

## 11 Layout

### 11.1 Layout Guidelines

Use the following steps as a reference to ensure the device is stable across its intended operating voltage and current range.

- Place CIN on the top layer (same layer as the LM2767) and as close to the device as possible. Connecting the input capacitor through short, wide traces to both the V+ and GND pins reduces the inductive voltage spikes that occur during switching which can corrupt the V+ line.
- Place COUT on the top layer (same layer as the LM2767) and as close as possible to the OUT and GND pin. The returns for both CIN and COUT must come together at one point, as close to the GND pin as possible. Connecting COUT through short, wide traces reduce the series inductance on the OUT and GND pins that can corrupt the VOUT and GND lines and cause excessive noise in the device and surrounding circuitry.
- Place C1 on the top layer (same layer as the LM2767 device) and as close to the device as possible. Connect the flying capacitor through short, wide traces to both the CAP+ and CAP– pins.

### 11.2 Layout Example

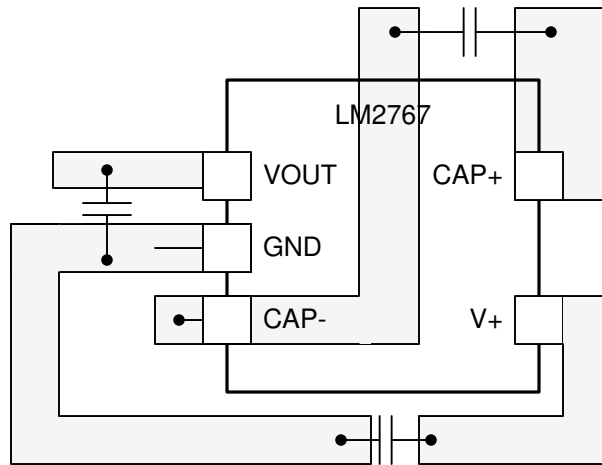


Figure 11-1. LM2767 Layout Example

## 12 Device and Documentation Support

### 12.1 Device Support

#### 12.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

#### 12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

#### 12.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

#### 12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

#### 12.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

#### 12.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM2767M5	ACTIVE	SOT-23	DBV	5	1000	Non-RoHS & Green	Call TI	Level-1-260C-UNLIM	-40 to 85	S17B	<a href="#">Samples</a>
LM2767M5/NOPB	ACTIVE	SOT-23	DBV	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	S17B	<a href="#">Samples</a>
LM2767M5X/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	S17B	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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# DBV0005A



# PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



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**NOTES:**

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

# EXAMPLE BOARD LAYOUT

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

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NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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