LP38869 1A FlexCap, Low-Dropout Linear Regulator with 0.75% Accuracy

Check for Samples: LP38869

FEATURES

- **Operating Input Supply Range: +2.7V to + 5.5V**
- **Maximum Continuous Output Current: 1A**
- **Preset Output Voltage of 2.5V, or Adjustable Output Voltage From 0.8V to 5.0V**
- **Pre-Set Output Initial V_{OUT} Tolerance ±0.5%**
- **Adjustable V_{REF} Tolerance of ±0.75%**
- **PSRR of 50dB at 100kHz**
- **Low 200 mV Dropout at 1A**
- **Typical 2 µA Supply Current in Shutdown Mode**
- **Adjustable Soft-Start for Output Current**
- **Fold-Back Output Current Limit**
- **Stable With Ceramic, Tantalum, or Aluminum Capacitors**
- **Stable With 1uF Input/Output Capacitors**
- **Thermal Shutdown**
- **16-pin HTSSOP Package**

APPLICATIONS

- **DSA, FPGA and MCU Power Supply**
- **SMPS Post-Regulator**
- **Applications Requiring Sequencing**
- **Gibabit SERDES Termination Supply**

DESCRIPTION

The LP38869 low-dropout linear regulator operates with an input voltage supply from +2.7V to +5.5V input, and delivers a specified 1A load current with a low 200 mV dropout. The high 50 dB PSRR at 100 kHz results from a high gain control loop that also yields excellent transient response. Coupled with a high accuracy output voltage, ±0.75 % over temperature, the LP38869 is an ideal power supply for FPGAs, DSPs or MCUs. Output voltage is preset at +2.5V, or may be adjustable between +0.8V to +5V with an external resistor divider.

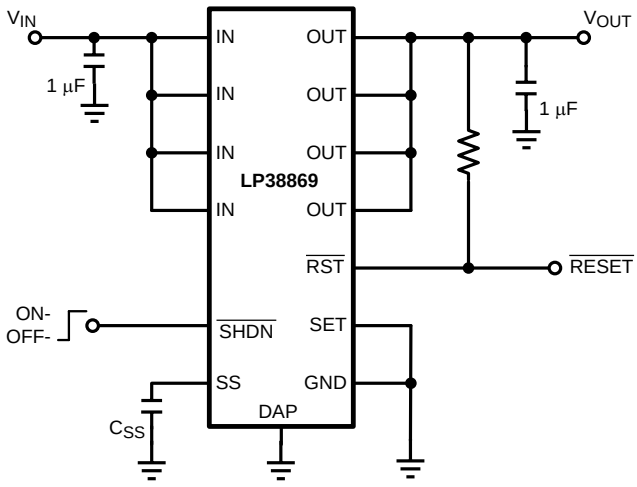
The LP38869 only needs 1 µF output capacitance for stability. The FlexCap compensation allows the use of any type of output capacitor, regardless of ESR. Other features include: Soft-Start; delayed reset output; low-power shutdown; short-circuit protection; and thermal shutdown protection

Ground Pin Current: Typically less than 1 mA at 1A load

Shutdown Mode: Typically 2 µA quiescent current when the $\overline{SHDN}$ pin is pulled low.

Simplified Compensation: Stable with any type of output capacitor.

Typical Application Circuit



Connection Diagram

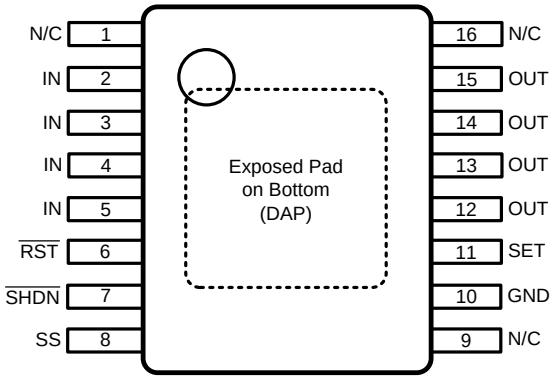


Figure 1. Top View
16-Pin HTSSOP

Pin Descriptions for 16-Pin HTSSOP Packages

Pin #	Pin Name	Description	Application Information
1	N/C	No Connection	No Internal Electrical Connection
2, 3, 4, 5	IN	Positive power input	Operates from +2.7V to +5.5V. Bypass capacitor is required, located close to the package; 1 µF is recommended as a minimum value
6	$\overline{\text{RST}}$	$\overline{\text{RESET}}$ Output	Open-drain output is low when V_{OUT} is 8% below normal regulation voltage. If regulation returns $\overline{\text{RST}}$ remains low for at least 3ms afterwards. Use large value pull-up resistor (100 kΩ) to V_{OUT} to obtain output voltage.
7	$\overline{\text{SHDN}}$	$\overline{\text{SHUTDOWN}}$ Input	A logic low state on the $\overline{\text{SHDN}}$ input will turn the regulator off, and will discharge any capacitor on the SS pin. A logic high on the $\overline{\text{SHDN}}$ pin will turn the regulator ON.
8	SS	Soft-Start control	Connect a capacitor from SS to GND. If SS is left open SS feature is disabled
9	N/C	No Connection	No Internal Electrical Connection
10	GND	Power Ground	Return connection for input and output voltages.
11	SET	Operational Mode Selection	Used to select between Pre-Set Mode or Adjustable Mode. Connect to ground (Pre-Set Mode) or to a resistor divider from V_{OUT} to SET pin to GND (Adjustable Mode).
12, 13, 14, 15	OUT	Regulated output	Regulated output voltage. A bypass capacitor is required, located close to the package; 1 µF recommended as the minimum value
16	N/C	No Connection	No Internal Electrical Connection
DAP	Exposed Pad	Thermal Connection	Solder the DAP to a copper plane under the package to improve thermal performance. DAP can be connected to ground at device Pin 10. Optionally, but not recommended, the DAP can be left floating. Do not connect DAP to any potential other than ground. See Operating Region and Power Dissipation.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)

VIN to GND (Survival)	-0.3V to 6.0V
All other inputs to GND	-0.3V to 6.0V
Power Dissipation (Survival)	Internally Limited
I_{OUT} (Survival)	Internally Limited
ESD Rating(3),Human Body Model	2 kV
Storage Temperature Range	-65°C to +150°C
Junction Temperature	150°C
Peak Reflow Temperature (4)	260°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but does not ensure specific performance limits. For ensured specifications and conditions, see the Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. Test method is per JESD22-A114.
(4) Peak Reflow Temperatures for Surface Mount devices are defined in *Absolute Maximum Ratings for Soldering* (literature number SNOA549).

Operating Ratings(1)

V_{IN} Voltage	2.7V to 5.5V
$V_{\overline{SHDN}}$ Voltage	0V to 5.5V
$V_{\overline{RST}}$ Voltage	0V to V_{IN}
Junction Temperature (T_J) (2)	−40°C to +125°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but does not ensure specific performance limits. For ensured specifications and conditions, see the Electrical Characteristics.
(2) Operating junction temperature must be evaluated, and derated as needed, based on ambient temperature (T_A), power dissipation (P_D), maximum allowable operating junction temperature ($T_{J(MAX)}$), and package thermal resistance (θ_{JA}). See Operating Region and Power Dissipation.

Electrical Characteristics

Unless otherwise specified: $V_{IN} = V_{OUT(NOM)} + 500$ mV, $V_{\overline{SHDN}} = V_{IN}$, $I_{OUT} = 10$ mA, $C_{IN} = 1$ µF MLCC, $C_{OUT} = 1$ µF MLCC, SS = Open. Limits in standard type are for $T_J = 25$°C only; limits in **boldface type** apply over the junction temperature (T_J) range of **-40°C to +125°C**. Minimum and Maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at $T_J = 25$°C, and are provided for reference purposes only.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IN}	Input Voltage Operating Range		**2.7**	-	**5.5**	V
UVLO	Input Under-Voltage Lock-Out	V_{IN} Rising or Falling Includes Hysteresis	**2.27**	2.45	**2.58**	V
ΔUVLO	UVLO Hysteresis		-	64	-	mV
V_{OUT}	Output Voltage Accuracy (Pre-Set Mode)	3.0V ≤ V_{IN} ≤ 5.5V, I_{OUT} = 1 mA, T_J = 25°C	-0.50	-	0.50	%
		I_{OUT} = 1 mA	**-0.75**	-	**0.75**	
V_{REF}	Regulated Feedback Voltage (Adjustable Mode)	I_{OUT} = 150 mA	**794**	800	**806**	mV
$\Delta V_{OUT(LINE)}$	Line Regulation (1)	ΔV_{IN} = 3.0 to 5.5V	-	0.0011	-	%/V
$\Delta V_{OUT(LOAD)}$	Load Regulation (2)	ΔI_{OUT} = 1 mA to 1A	-	0.2	**1.85**	%/A

(1) Line Regulation is the % change in V_{OUT} from $V_{OUT(NOM)}$ for every 1V change in V_{IN},Line Regulation = ((ΔV_{OUT} / $V_{OUT(NOM)}$) / ΔV_{IN}) x 100%
(2) Load Regulation is the % change in V_{OUT} from $V_{OUT(NOM)}$ for every 1A change in I_{OUT}, Load Regulation = ((ΔV_{OUT} / $V_{OUT(NOM)}$) / ΔI_{OUT}) x 100%

Electrical Characteristics (continued)

Unless otherwise specified: $V_{IN} = V_{OUT(NOM)} + 500$ mV, $V_{\overline{SHDN}} = V_{IN}$, $I_{OUT} = 10$ mA, $C_{IN} = 1$ µF MLCC, $C_{OUT} = 1$ µF MLCC, SS = Open. Limits in standard type are for $T_J = 25°C$ only; limits in **boldface type** apply over the junction temperature (T_J) range of **-40°C to +125°C**. Minimum and Maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at $T_J = 25°C$, and are provided for reference purposes only.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{GND}	Ground Pin Current	I_{OUT} = 100 µA	-	0.6	**2**	mA
		I_{OUT} = 1A	-	0.7	-	
I_{OFF}	Shutdown Supply Current	$V_{\overline{SHDN}}$ = 0.0V, V_{IN} = +5.5V, V_{OUT} = 0V	-	2	**20**	µA
	Adjustable Output Voltage Range	1 mA ≤ I_{OUT} ≤ 1 A	**0.8**	-	**5**	V
$I_{OUT(MAX)}$	Maximum Output Current	Continuous	**1.0**	-	-	A
I_{SC}	Short Circuit Current	V_{OUT} = 0V	**1.0**	1.9	-	A
I_{LIM}	In Regulation Current Limit	V_{SET} = 0.760V, -40°C ≤ T_J ≤ 85°C	2.0	3	-	A
		V_{SET} = 0.760V	**1.9**			
$V_{SET(TH)}$	SET Dual Mode Threshold	Threshold is where SET pin voltage rising from 0.0V deactivates the Pre-Set Mode	**35**	87	**138**	mV
I_{SET}	SET Pin Bias Current	V_{SET} = +0.900V	-	2	**300**	nA
V_{DO}	Dropout Voltage (3)	I_{OUT} = 1 mA	-	0.2	-	mV
		I_{OUT} = 1.0A	-	185	**330**	
$V_{\overline{SHDN}(ON)}$	$\overline{SHDN}$ ON Threshold	$V_{\overline{SHDN}}$ rising until output is acitve +2.7V ≤ V_{IN} ≤ +5.5V	**1.60**	0.86	-	V
$V_{\overline{SHDN}(OFF)}$	$\overline{SHDN}$ OFF Threshold	$V_{\overline{SHDN}}$ falling until output is shutdown +2.7V ≤ V_{IN} ≤ +5.5V	-	0.78	**0.58**	
$\Delta V_{\overline{SHDN}}$	$V_{\overline{SHDN}}$ Hysteresis	+2.7V ≤ V_{IN} ≤ +5.5V	-	80	-	mV
$I_{\overline{SHDN}}$	$\overline{SHDN}$ Input Bias Current	$V_{\overline{SHDN}}$ = 0V	-	0.002	**0.1**	µA
		$V_{\overline{SHDN}}$ = 5.5V	-	0.002	**0.1**	
I_{SS}	Soft-Start Charge Current	V_{SS}= 0.0V	-	6.7	-	µA
	$\overline{RST}$ Output Low Voltage	$I_{\overline{RST}(SINK)}$ = 1 mA	-	0.007	**0.1**	V
	Operating Input Voltage (V_{IN}) Range for $\overline{RST}$ Valid	$I_{\overline{RST}(SINK)}$ = 10 µA	**1.0**	-	**5.5**	V
$I_{\overline{RST}}$	$\overline{RST}$ Leakage	V_{IN} = 5.5V, $V_{\overline{RST}}$ = 5.5V	-	0.0	**1**	µA
$V_{\overline{RST}(TH)}$	$\overline{RST}$ Threshold	V_{OUT} falling from $V_{OUT(NOM)}$ until $\overline{RST}$ pin goes low	**86**	92	**97**	% OUT
$\Delta V_{\overline{RST}}$	$\overline{RST}$ Hysteresis	V_{OUT} rising from $V_{\overline{RST}(TH)}$ until $\overline{RST}$ pin goes high	-	10	-	mV
$t_{\overline{RST}(DELAY)}$	$\overline{RST}$ Release Delay time	Time from when V_{OUT} returns to normal to when $V_{\overline{RST}}$ goes high	**1.0**	3	**5.5**	ms
AC Parameters						
PSRR	Ripple Rejection	F = 100 kHz, C_{OUT} = 1 µF Ceramic, I_{OUT} = 300 mA	-	54	-	dB
V_{NOISE}	Output Noise	f = 10Hz to 100 kHz, C_{OUT} = 1µF Ceramic, I_{OUT} = 150 mA	-	50	-	μV_{RMS}
Thermal Characteristics						
T_{SD}	Thermal Shutdown	T_J rising	-	160	-	°C
ΔT_{SD}	Thermal Shutdown Hysteresis	T_J falling from T_{SD}	-	15	-	

(3) Dropout voltage (V_{DO}) is defined as the minimum input to output differential voltage at which the output voltage drops to 100 mV below the nominal value. For any output voltage less than 2.5V, the minimum V_{IN} operating voltage of 2.7V is the limiting factor, and dropout voltage is not a valid parameter.

Typical Performance Characteristics

Unless otherwise specified: T_J = 25°C, V_{IN} = 5.0V, $V_{\overline{SHDN}}$ = V_{IN}, V_{SET} = 0.0V, V_{OUT} = 2.5V, SS = Open, C_{IN} = 1 µF, C_{OUT} = 1 µF MLCC, I_{OUT} = 100mA

V_{OUT} vs. I_{OUT}

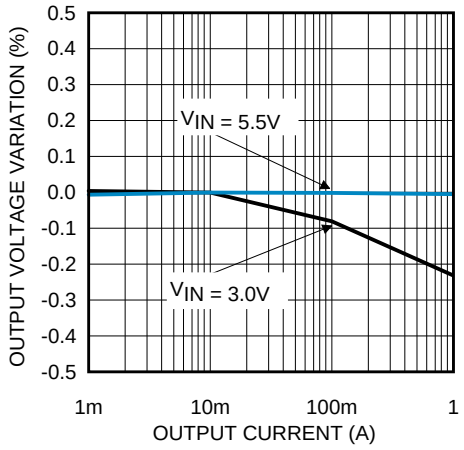


Figure 2.

V_{REF} vs. Temperature (T_J), V_{IN} = 2.7V

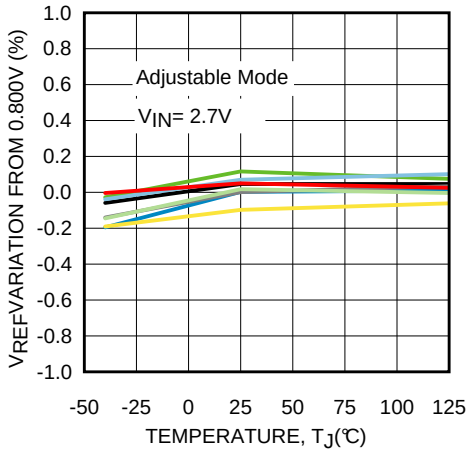


Figure 3.

V_{REF} vs. Temperature (T_J), V_{IN} = 5.5V

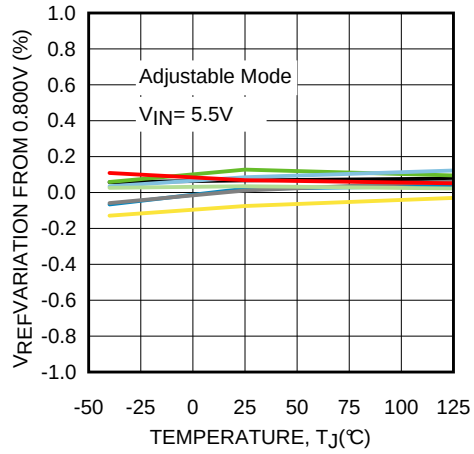


Figure 4.

I_{GND} vs. V_{IN}

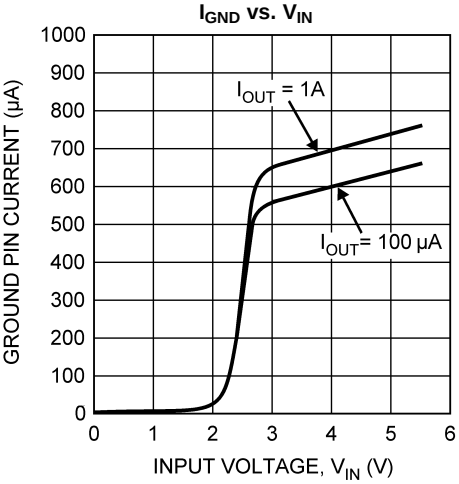


Figure 5.

I_{GND} vs. I_{OUT}, V_{IN} = 2.7V

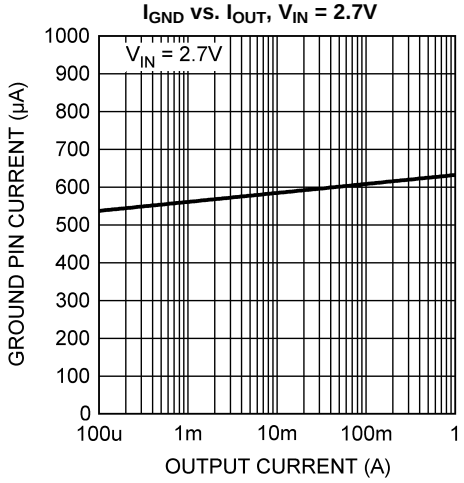


Figure 6.

I_{GND} vs I_{OUT}, V_{IN} = 3.0V

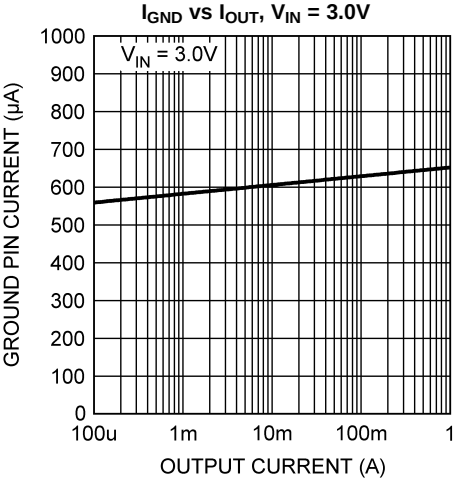


Figure 7.

Typical Performance Characteristics (continued)

Unless otherwise specified: T_J = 25°C, V_{IN} = 5.0V, $V_{\overline{SHDN}}$ = V_{IN}, V_{SET} = 0.0V, V_{OUT} = 2.5V, SS = Open, C_{IN} = 1 µF, C_{OUT} = 1 µF MLCC, I_{OUT} = 100mA

I_{GND} vs I_{OUT}, V_{IN} = 5.5V

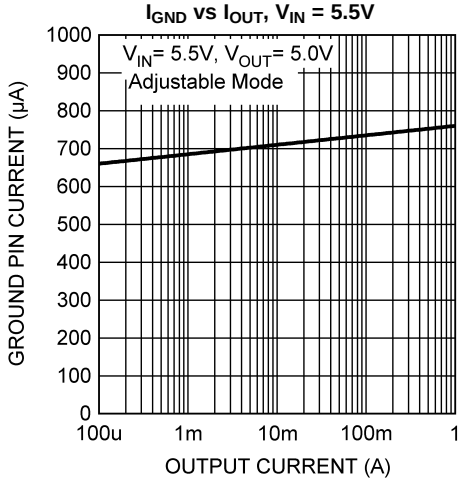


Figure 8.

I_{GND} vs Temperature (T_J), V_{IN} = 2.7V

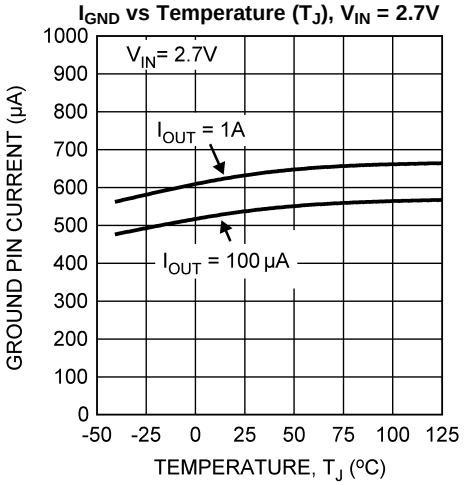


Figure 9.

I_{GND} vs Temperature (T_J), V_{IN} = 3.0V

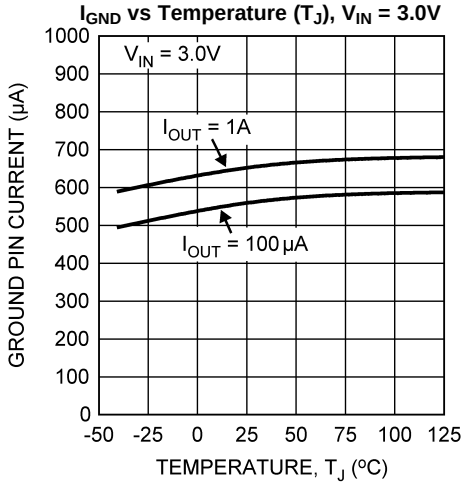


Figure 10.

I_{GND} vs Temperature (T_J), V_{IN} = 5.5V

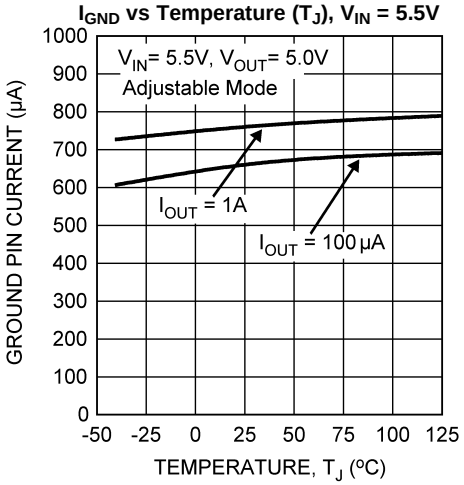


Figure 11.

Dropout Voltage (V_{DO}) vs I_{OUT}

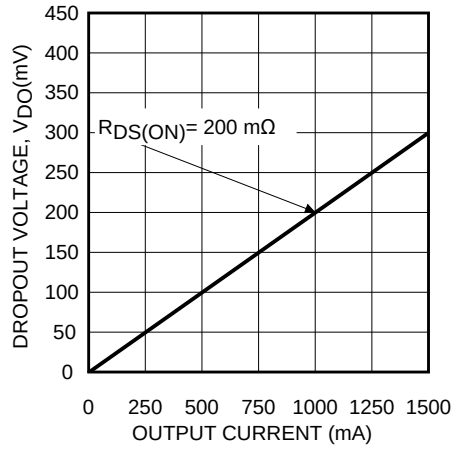


Figure 12.

Dropout Voltage (V_{DO}) vs V_{IN}

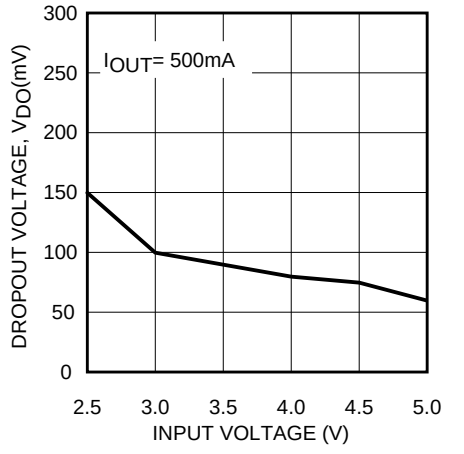


Figure 13.

Typical Performance Characteristics (continued)

Unless otherwise specified: T_J = 25°C, V_{IN} = 5.0V, $V_{\overline{SHDN}}$ = V_{IN}, V_{SET} = 0.0V, V_{OUT} = 2.5V, SS = Open, C_{IN} = 1 µF, C_{OUT} = 1 µF MLCC, I_{OUT} = 100mA

PSRR vs Frequency

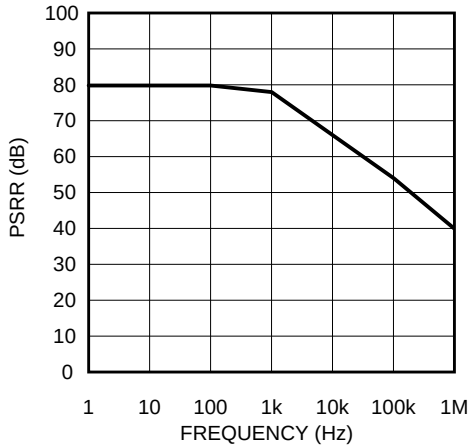


Figure 14.

Output Noise Density

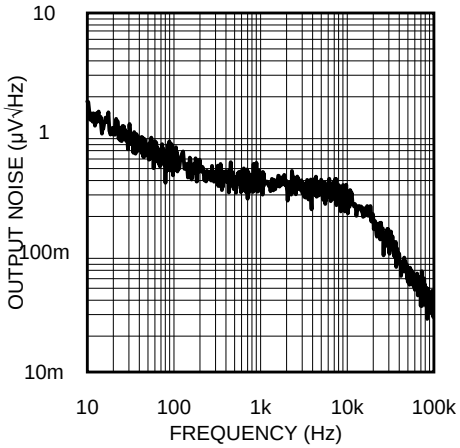


Figure 15.

Output Noise vs. I_{OUT}

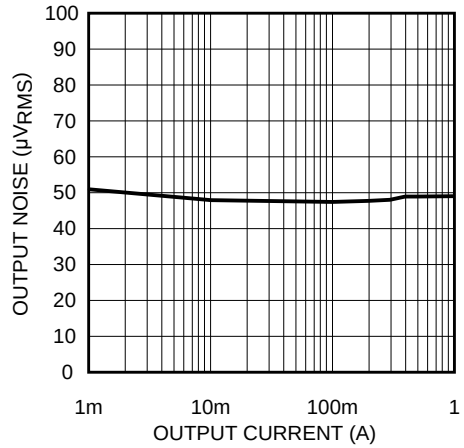


Figure 16.

Output Noise

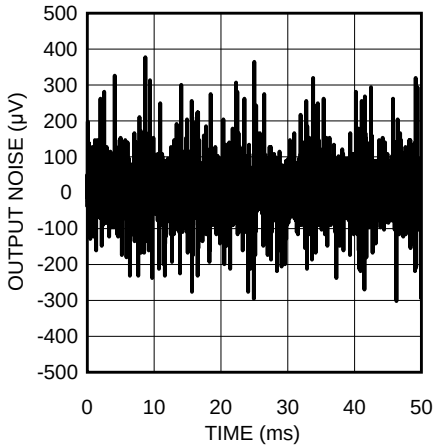


Figure 17.

Load Transient Response, V_{IN} = 5.0V

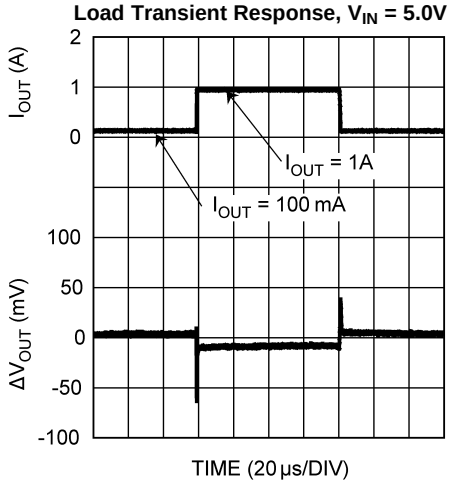


Figure 18.

Load Transient Response, V_{IN} = 3.0V

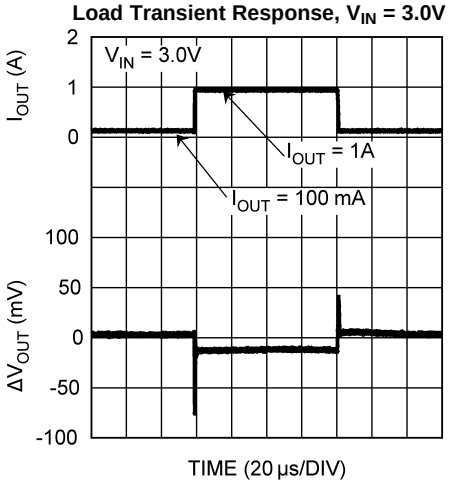


Figure 19.

Typical Performance Characteristics (continued)

Unless otherwise specified: T_J = 25°C, V_{IN} = 5.0V, $V_{\overline{SHDN}}$ = V_{IN}, V_{SET} = 0.0V, V_{OUT} = 2.5V, SS = Open, C_{IN} = 1 µF, C_{OUT} = 1 µF MLCC, I_{OUT} = 100mA

Load Transient Response, 10mA to 3A

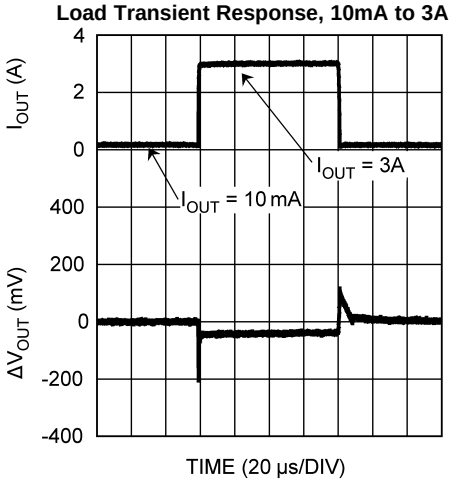


Figure 20.

Line Transient Response, I_{OUT} = 250mA

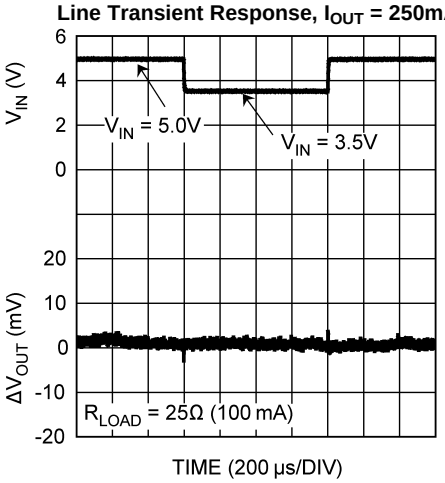


Figure 21.

Line Transient Response, I_{OUT} = 1A

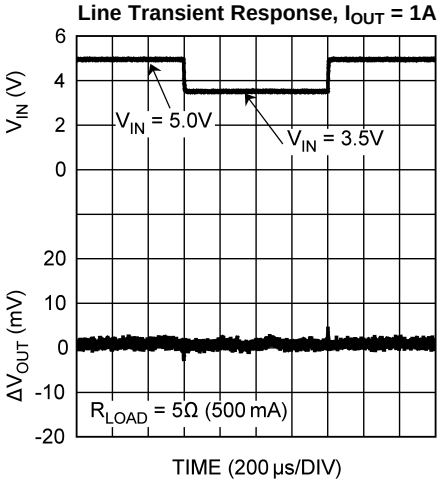


Figure 22.

$V_{\overline{SHDN}}$ to V_{OUT} Delay Time

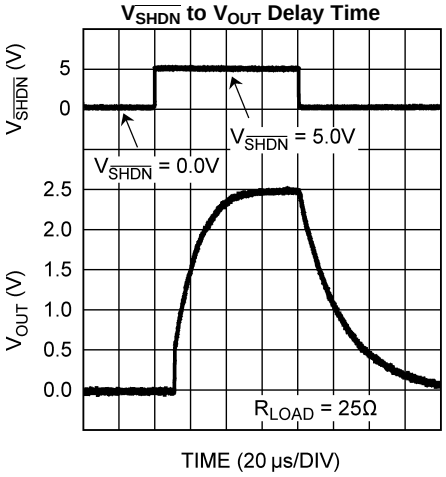


Figure 23.

$\overline{SHDN}$ Thresholds vs V_{IN}

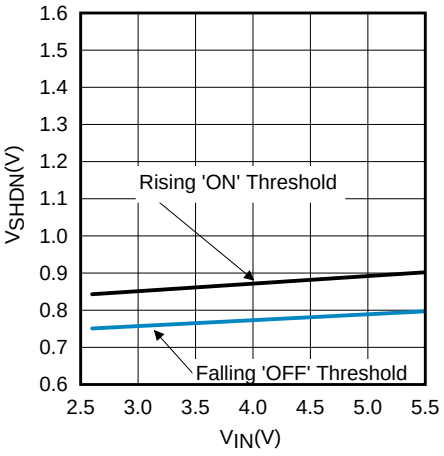


Figure 24.

$\overline{SHDN}$ Thresholds vs Temperature (T_J)

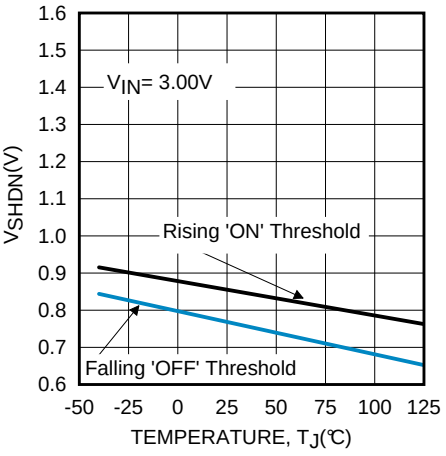


Figure 25.

Typical Performance Characteristics (continued)

Unless otherwise specified: T_J = 25°C, V_{IN} = 5.0V, $V_{\overline{SHDN}}$ = V_{IN}, V_{SET} = 0.0V, V_{OUT} = 2.5V, SS = Open, C_{IN} = 1 µF, C_{OUT} = 1 µF MLCC, I_{OUT} = 100mA

SET Threshold ($V_{SET(TH)}$) vs V_{IN}

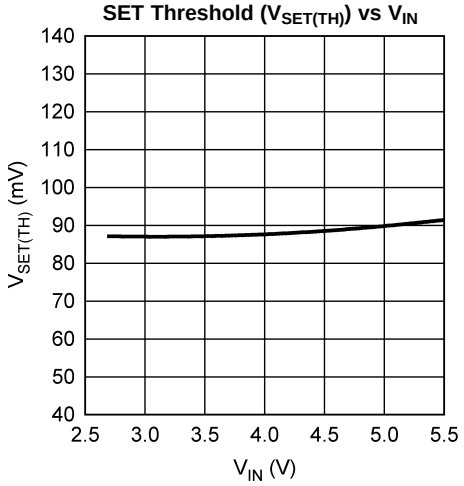


Figure 26.

Soft-Start, C_{SS}= 100nF

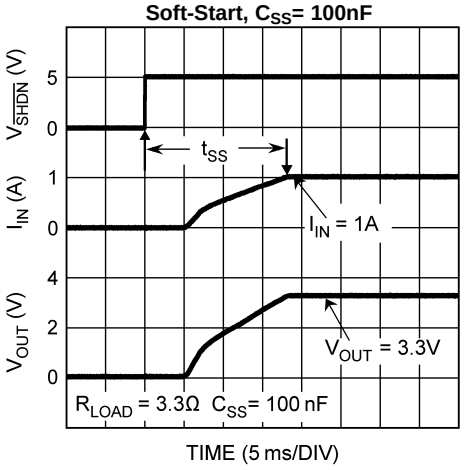


Figure 27.

UVLO vs Temperature (T_J)

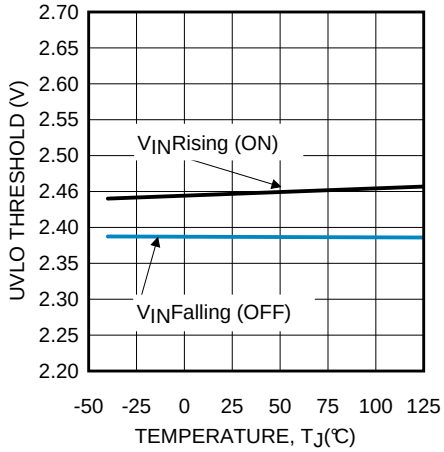


Figure 28.

$\overline{RST}$ Output, V_{OUT} Rising

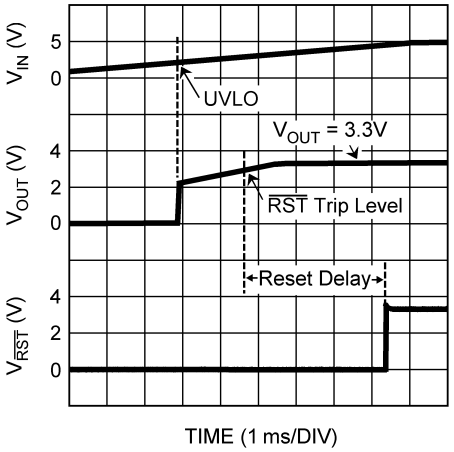


Figure 29.

$\overline{RST}$ Output, V_{OUT} Falling

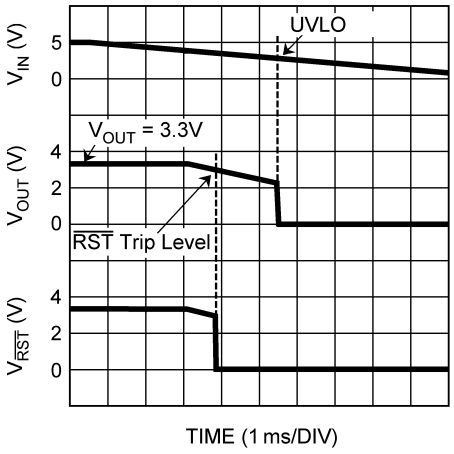


Figure 30.

BLOCK DIAGRAM

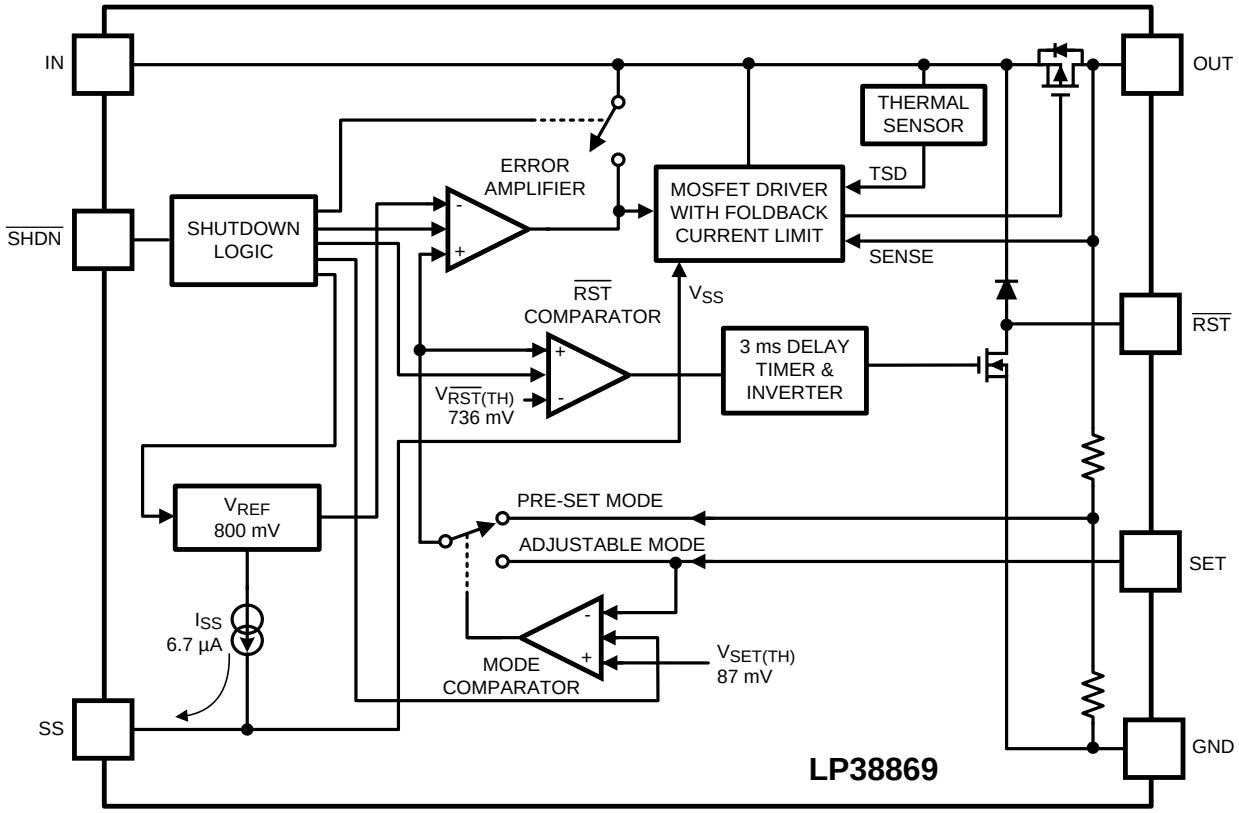


Figure 31. Functional Block Diagram

APPLICATIONS INFORMATION

The LP38869 is a dual mode LDO that operates either as a fixed output, 2.5V regulator, or as an adjustable output regulator from +0.8V to +5.0V. Output current is specified to be a minimum of 1A. The output requires a minimum 1µF of capacitance for stability.

Referring to the functional block diagram at Figure 31, the device consists or a 800 mV reference (V_{REF}), error amplifier, MOSFET driver, P-channel pass transistor, internal feedback divider, soft-start function, reset timer, and dual mode comparator, and a low V_{OUT} ($\overline{RST}$) comparator.

With the 800 mV reference connected to the error amplifier's inverting input, the error amplifier compares this reference with the selected feedback voltage and amplifies the difference. Usually the feedback voltage is connected to the error amplifier's inverting input, but in the case of the LP38869 the logic is inverted to drive a P-channel MOSFET. The MOSFET driver takes the error amplifier output and applies the appropriate gate drive to the P-channel transistor. For a high feedback voltage, the MOSFET gate is pulled higher, allowing less current to flow to the output. The low V_{OUT} comparator senses when the feedback voltage has dropped 8% below its expected level, causing $\overline{RST}$ pin to go low. The Dual Mode comparator monitors the voltage at the SET pin and selects the feedback path. If the SET pin voltage is below the typical 87 mV threshold, the internal feedback path is used and the output voltage is regulated to the factory-preset voltage. Otherwise, the output voltage is set with the external resistor-divider.

Capacitor Selection and Regulator Stability

Capacitors are required at the LP38869's input and output. Connect a 1 µF or greater capacitor(s) between V_{IN} and GND (C_{IN}), and between V_{OUT} and GND (C_{OUT}). Due to the LP38869's relatively high bandwidth, use only surface mount ceramic capacitors that have a low equivalent series resistance (ESR) and high self-resonant frequency (SRF). Make the input and output traces at least 2.5mm wide (the width of the four parallel pins), and connect C_{IN} and C_{OUT} within 6mm of the IC to minimize the impact of PC board trace inductance. The width of the ground trace should be maximized underneath the IC to ensure a good connection between device pin 10 (GND) and the ground side of the capacitors.

The output capacitor's ESR and SRF can affect stability and output noise. Use capacitors with a SRF of greater than 5 MHz and with an ESR of 60 mΩ or less to insure stability and optimum transient response. This is particularly true in applications with lower output voltage (V_{OUT} < 2V) and higher output current (I_{OUT} > 500 mA).

Since some capacitor dielectrics may vary over bias voltage and temperature, consult the capacitor manufacturer specifications to ensure that the capacitors meet these requirements over all voltage and temperature conditions.

Internal P-Channel Pass Transistor

The LP38869 features a 1A P-channel MOSFET pass transistor. Unlike similar designs using PNP pass transistors, P-channel MOSFETs require no continuous base (gate) drive, which reduces quiescent current. PNP based regulators also waste considerable current in dropout when the pass transistor saturates and uses a high base drive current under large loads. The LP38869 does not suffer from these problems and typically consumes only 600 uA of quiescent current, even in dropout.

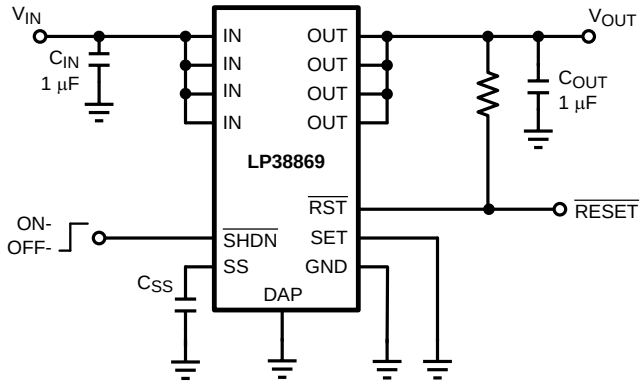


Figure 32. Typical Operating Circuit with Preset Output Voltage

Input-Output (Drop Out) Voltage

A regulator's minimum input-to-output voltage differential (dropout voltage) determines the lowest usable input voltage. In battery-powered systems, this determines the useful end-of-life battery voltage. Since a 200 mΩ P-channel MOSFET is used as the pass device, dropout voltage is the product of $R_{DS(ON)}$ and load current passing through it. The LP38869 operating current remains low in dropout.

For output voltages that are less than the UVLO threshold, the UVLO threshold itself will determine the minimum input voltage.

Output Voltage Selection

The LP38869 features Dual Mode operation. Connect the SET pin to GND as shown in Figure 32 for the Preset Mode where the output voltage is preset at the factory. In the Adjustable Mode, set the output voltage between +0.8V to +5.0V through two external resistors (R1 and R2) connected as a voltage divider to the SET pin as shown in Figure 33. The output voltage is set by the following equation.

$$V_{OUT} = V_{REF} \times (1 + (R1 / R2)) \quad (1)$$

where V_{REF} = 800 mV.

Solving for R1 with a known value for R2:

$$R1 = R2 \times ((V_{OUT} / V_{REF}) - 1) \quad (2)$$

In the Adjustable Mode the current through R1 and R2 should be much greater than the SET pin bias current to minimize any error that the bias current may cause. Up to 10 kΩ is acceptable for R2, with R1 scaled for the appropriate V_{OUT}.

In the Pre-Set voltage mode, the impedance between the SET pin and ground should be less than 10 kΩ. Otherwise, spurious conditions could cause the voltage at the SET pin to exceed the typical 87 mV Dual Mode threshold.

In the Adjustable Mode the resistors used for R1 and R2 should be high quality, tight tolerance, and with matching temperature coefficients. It is important to remember that, although the value of V_{REF} is ensured, the final value of V_{OUT} in the Adjustable Mode is not. The use of low quality resistors for R1 and R2 can easily produce an Adjustable Mode V_{OUT} value that is unacceptable.

Shutdown Mode

A logic low on the $\overline{SHDN}$ pin disables the LP38869. In shutdown mode, the pass transistor, control circuitry, reference, and all bias currents are turned off, reducing supply current to typically 2 µA. Connect $\overline{SHDN}$ to the IN pin for continuous operation if the function is not needed. In shutdown mode the $\overline{RST}$ pin is low and the Soft-Start capacitor is discharged.

$\overline{RST}$ Comparator

The open-drain $\overline{RST}$ pin goes low when V_{OUT} falls 8% below its nominal output voltage. The $\overline{RST}$ pin remains low for 3 ms after V_{OUT} has returned to its normal value. A 100 kΩ pull-up resistor from the $\overline{RST}$ pin to a suitable logic supply voltage (typically V_{OUT}) provides a logic control signal. The $\overline{RST}$ output logic signal can be used as a power on-reset signal to a micro-controller, or can drive an external LED for indicating a power failure. The $\overline{RST}$ pin is low during shutdown. The $\overline{RST}$ status remains valid for V_{IN} as low as 1V. When V_{IN} is less than 1V the $\overline{RST}$ pin status may not be valid.

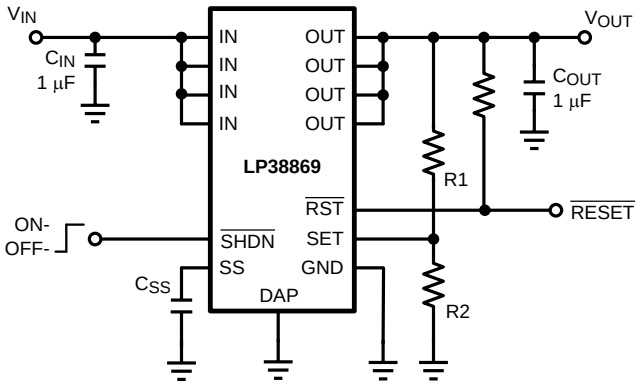


Figure 33. Typical Operating Circuit Adjustable Output Voltage

Soft-Start

As shown in Figure 34, a capacitor on the SS pin allows a gradual ramp-up of the LP38869's output current, reducing the initial in-rush current peaks at startup. When SHDN pin is driven low, the soft-start capacitor is discharged to 0.0V. When the SHDN is driven high, or power is applied to the device, a constant 6.7 µA current charges the Soft-Start capacitor from 0.0V. The resulting linear ramp voltage on SS increases the current-limit comparator threshold, limiting the P-channel gate drive. While the voltage on the Soft-Start pin (V_{SS}) is less than approximately 300 mV there will be no output current. When Vss rises above approximately 300mV, the output current limit will rise from zero to approximately 250 mA. As V_{SS} continues to rise the current limit will also rise proportionally so that when V_{SS} is at typically 1.25V the current limit will be at approximately 1A. As the current limit rises above 1A, the current limit control will pass from V_{SS} to internal biasing circuitry. See the Soft-Start Capacitor Selection section for details.

There is a delay time between when SHDN enables the LP38869 and when Soft-Start begins ramping up the output current limit. This delay time allows the LP38869 internal biasing to fully turn on and settle. The delay time is set by the time required for the Soft-Start charge current (I_{SS}) to charge the Soft-Start capacitor from 0.0V to typically 300 mV. This delay time accounts for approximately 25% of the total Soft-Start time (t_{SS}). With a 100 nF Soft-Start capacitor, the delay is approximately 4 ms with the remainder of the t_{SS} time (approximately 15 ms) allocated to raising the output current limit from zero to 1A.

Leaving the SS pin floating (open) will disable the Soft-Start feature by setting the t_{SS} time to zero.

If the current demand from the load is significantly less than 1A, the time needed for the current limit to ramp up to meet the actual current demand, after the delay time, will be a small fraction of the t_{SS} time.

Soft-Start Capacitor Selection

Unlike typical Soft-Start circuits that control the rise of the output voltage, the LP38869 Soft-Start controls rise of the output current limit. The resulting voltage rise across the load will depend on any reactive composition of the load.

A capacitor (C_{SS}) connected from the SS pin to GND causes the LP38869's output current to slowly rise from zero during start-up, reducing stress on the power path components and input supply. Soft-Start time (t_{SS}) is defined as the time from start-up (i.e. t = 0) until the current limit reaches 1A. The current limit will continue to rise beyond 1A as the SS capacitor continues to charge to a higher voltage.

Typically, the current limit will be at 1A when the voltage on the SS capacitor (Vss) has charged to 1.25V.

The time from start-up (V_{SS} = 0V) to when the output current limit reaches 1A (V_{SS} = 1.25V) , can be estimated by:

$$t_{SS} = (C_{SS} / I_{SS}) \times 1.25V \quad (3)$$

This can be simplified to:

$$t_{SS} = 0.186 \times C_{SS} \quad (4)$$

where C_{SS} is in nF, and the calculated t_{SS} result is in milli-seconds.

Typical Soft-Start capacitor values are between 10nF to 100nF. The typical t_{SS} with a C_{SS} of 100 nF is:

$$t_{SS} = (100 \text{ nF} / 6.7 \text{ uA}) \times 1.25\text{V} = 18.6 \text{ ms} \quad (5)$$

Use of a low leakage capacitor for C_{SS} is required, and voltage rating of 5V for C_{SS} is adequate.

Because the C_{SS} ramp is applied to the output current-limit comparator, the actual time for the output voltage to ramp-up depends on the actual load current demand and output capacitor value. Leaving the SS pin open will disable the Soft-Start behavior by setting the t_{SS} time to zero.

Current Limiting

The LP38869 features a 2A current limit when the output voltage is in regulation. When the output voltage drops by 8% below its nominal value, the current limit folds back to 1.7A. While the LP38869 output can be shorted to ground for an indefinite period of time without damaging the device, power dissipation due to continuous output currents of more than 1A may stress, or damage, adjacent components. The nominal current limit can be reduced by holding the voltage at the Soft-Start (SS) pin below 1.25V. For V_{SS} rising from approximately 300 mV to 1,25V the current limits scale proportionately with the V_{SS} by:

$$I_{LIM} = 1\text{A} \times (V_{SS} / 1.25\text{V}) \quad (6)$$

Since the SS pin sources a typical 6.7 µA current (I_{SS}), the current limit can be reduced below 1A by connecting a resistor (R_{SS}) between the SS pin and GND, so that:

$$I_{LIM} = 1\text{A} \times ((I_{SS} \times R_{SS}) / 1.25\text{V}) \quad (7)$$

where the typical I_{SS} = 6.7 µA.

The useful range of R_{SS} values is approximately 75 kΩ to 200 kΩ. R_{SS} values less than 75 kΩ may not be able to reliably raise V_{SS} above the minimum needed (typically 300 mV) to activate the current limit. R_{SS} values greater than 200 kΩ will only have a marginal impact on the nominal current limit.

With R_{SS} in place, Soft-Start can still be achieved by placing a capacitor (C_{SS}) in parallel with R_{SS}. The output current now ramps up asymptotically to the reduced current limit rather than the nominal value, increasing the soft-start time. The time required for the current limit to reach 90% of its steady-state value with R_{SS} in place is estimated by:

$$t_{SS} = 2.5 \times R_{SS} \times C_{SS} \quad (8)$$

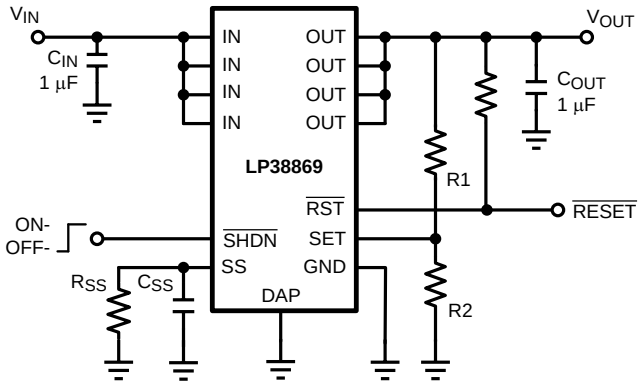


Figure 34. Typical Operating Circuit Soft-Start and Current Limit Reduction

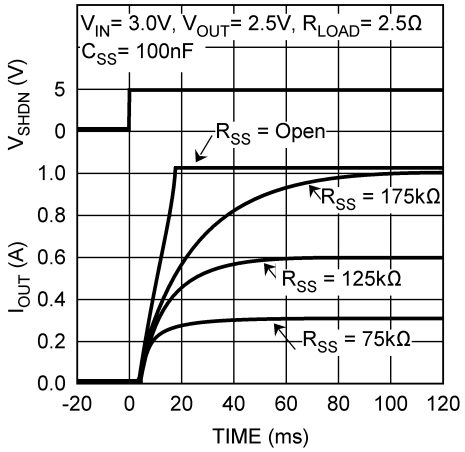


Figure 35. Typical Soft-Start Current Limit Behavior with C_{SS} = 100 nF

Thermal Overload Protection

Thermal overload protection limits total power dissipation in the LP38869. When the junction temperature exceeds typically T_J = +160°C, the thermal sensor turns off the pass transistor, allowing the LP38869 to cool. The thermal sensor turns the pass transistor on once the IC's junction temperature drops by approximately 15°C. Continuous short-circuit conditions will eventually result in a pulsed output current with a frequency that depends on the thermal resistance and thermal mass of the LP38869 package and PC board combination as well as the ambient temperature. Thermal overload protection is designed to protect the LP38869 in the event of fault conditions. For continuous operation, do not exceed the absolute maximum junction temperature rating of T_J = 150°C. Parametric ratings are not ensured if the junction rises above 125°C.

Operating Region and Power Dissipation

Maximum power dissipation of the LP38869 depends on the thermal resistance of the case and circuit board, the temperature difference between the die junction and ambient air, and the rate of air flow. The power dissipation across the device is defined by:

$$P_{DISS} = I_{OUT} \text{ X } (V_{IN} - V_{OUT}) \quad (9)$$

The resulting maximum power dissipation is:

$$P_{DISS(MAX)} = (T_{J(MAX)} - T_{A(MAX)}) / (\theta_{JA} \quad (10)$$

Where $(T_{J(MAX)} - T_{A(MAX)})$ is the maximum allowable junction temperature rise above the surrounding ambient air; and θ_{JA} is thermal resistance from the junction through the package DAP, to the PC board, copper traces, and other materials into the surrounding air.

Figure 36 uses this formula to show a range of allowable dissipation values that will keep the junction temperature ($T_{J(MAX)}$) inside the Maximum Operating Junction Temperature of 125°C.

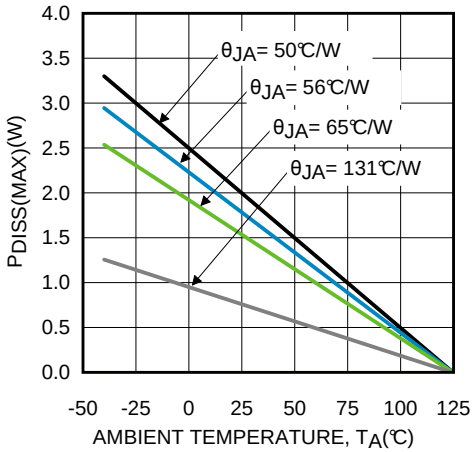


Figure 36. Maximum Dissipation vs. Ambient Temperature

Figure 37 shows the allowable power dissipation factors for a typical multi-layer PC board at ambient temperatures of +25°C, +50°C, and +70°C for the AbsMax junction temperature of 150°C.

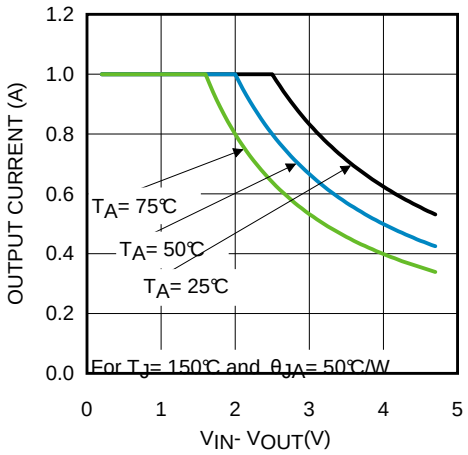


Figure 37. Maximum Output Current vs Input-Output Differential Voltage

The LP38869 HTSSOP package features an exposed thermal pad on its underside. This exposed pad lowers the package's thermal resistance by providing a direct thermal heat path from the die to the PC board. Connect the exposed thermal pad to circuit ground using a large copper pad (1 square inch is the recommended minimum), or use multiple thermal vias to the ground plane of a multi-layer PCB.

For the LP38869MH in the HTSSOP Exposed Pad 16-Lead package, the junction-to-case thermal rating, θ_{JC}, is 16.2°C/W, where the case is the bottom of the package at the center of the Exposed Pad. Typical junction-to-ambient thermal performance for the LP38869MH, using the JESD51 standards, is summarized in the following table.

BOARD TYPE	THERMAL VIAS	θ_{JA}
JEDEC 2-Layer JESD 51-3	None	141°C/W
JEDEC 4-Layer JESD 51-7	0	131°C/W
	1	78°C/W
	2	65°C/W
	3	59°C/W
	4	56°C/W
	6	53°C/W
	9	50°C/W

Noise, PSRR, and Transient Response

The LP38869 is designed to achieve low dropout voltage and low quiescent current in battery-powered systems while still maintaining good noise, transient response, and AC rejection (see PSRR vs. Frequency in the Typical Operating Characteristics). When operating from very noisy sources, supply noise rejection and transient response can be improved by increasing the input and output capacitor values and employing passive post filtering. The LP38869 output noise is typically 50 μV_{RMS}.

Reverse Input-Output Voltage

A reverse voltage condition will exist when the voltage at the output pin is higher than the voltage at the input pin. Typically this will happen when V_{IN} is abruptly taken low and C_{OUT} continues to hold a sufficient charge such that the input to output voltage becomes reversed. Alternately, this could also happen if a secondary supply is connected to the LP38869 output.

While V_{IN} is greater than the UVLO threshold, and the $\overline{SHDN}$ pin is above the $V_{\overline{SHDN}(ON)}$ threshold, the control loop circuitry will attempt to regulate the output voltage. Since the input voltage is less than the output voltage the control circuit will drive the gate of the pass element to the full ON condition when the output voltage begins to fall. In this condition, reverse current will flow from the output pin to the input pin, limited only by the $R_{DS(ON)}$ of the pass element and the output to input voltage differential. This will condition will continue until V_{IN} falls below the UVLO threshold, or the $\overline{SHDN}$ pin voltage falls below the $V_{\overline{SHDN}(OFF)}$ threshold.

The internal PFET pass element in the LP38869 has an inherent parasitic (body) diode. During normal operation, the input voltage is higher than the output voltage and the body diode is reverse biased. However, if the output is turned OFF, either by V_{IN} < UVLO or $V_{\overline{SHDN}} < V_{\overline{SHDN}(OFF)}$, and the output voltage is more than 500 mV (typical) above the input voltage the body diode becomes forward biased and current flows from the output pin to the input pin through the body diode.

The reverse current in the body diode should be limited to less than 1A continuous and less than 5A peak.

REVISION HISTORY

Changes from Revision A (April 2013) to Revision B	Page
• Changed layout of National Data Sheet to TI format	17

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP38869MH/NOPB	ACTIVE	HTSSOP	PWP	16	92	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LP38869 MH	Samples
LP38869MHE/NOPB	ACTIVE	HTSSOP	PWP	16	250	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LP38869 MH	Samples
LP38869MHX/NOPB	ACTIVE	HTSSOP	PWP	16	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LP38869 MH	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

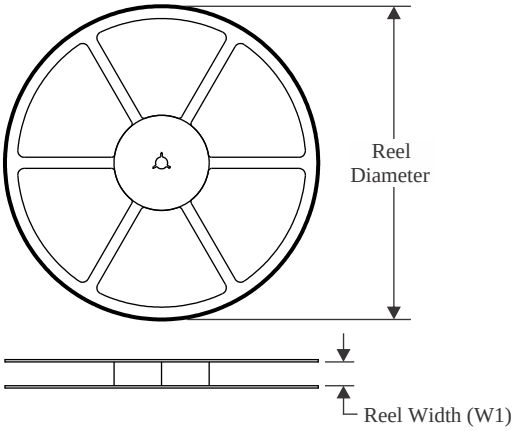
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

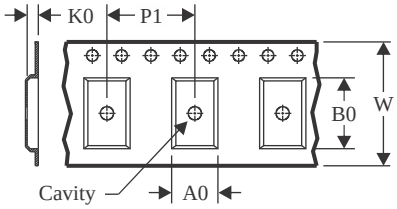
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

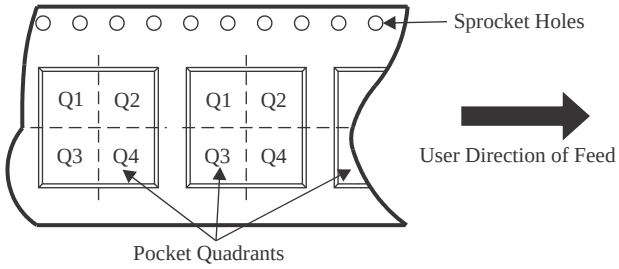


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

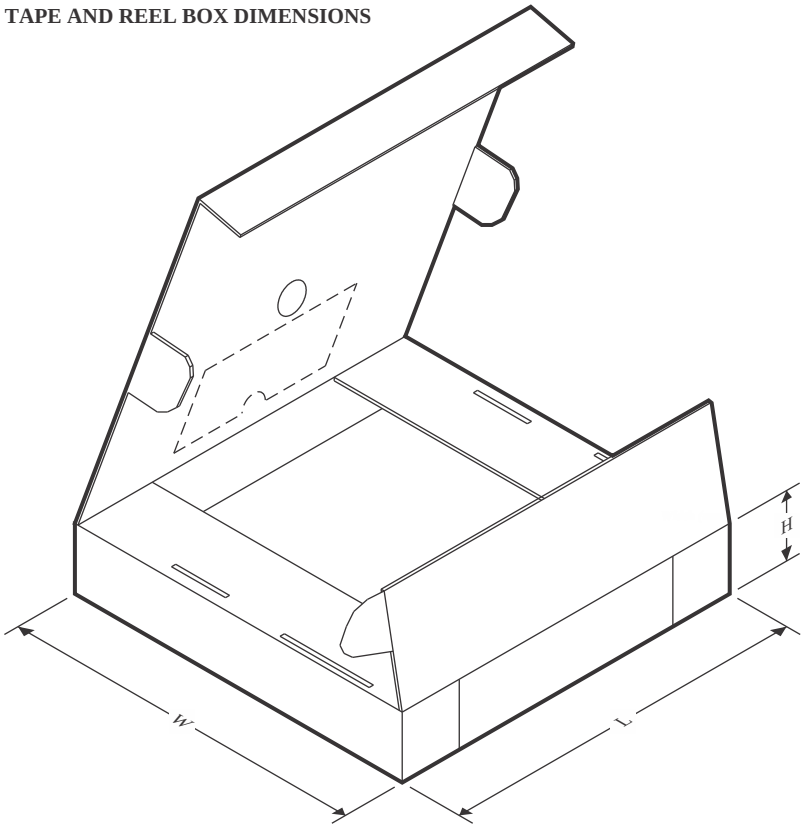
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP38869MHE/NOPB	HTSSOP	PWP	16	250	178.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LP38869MHX/NOPB	HTSSOP	PWP	16	2500	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

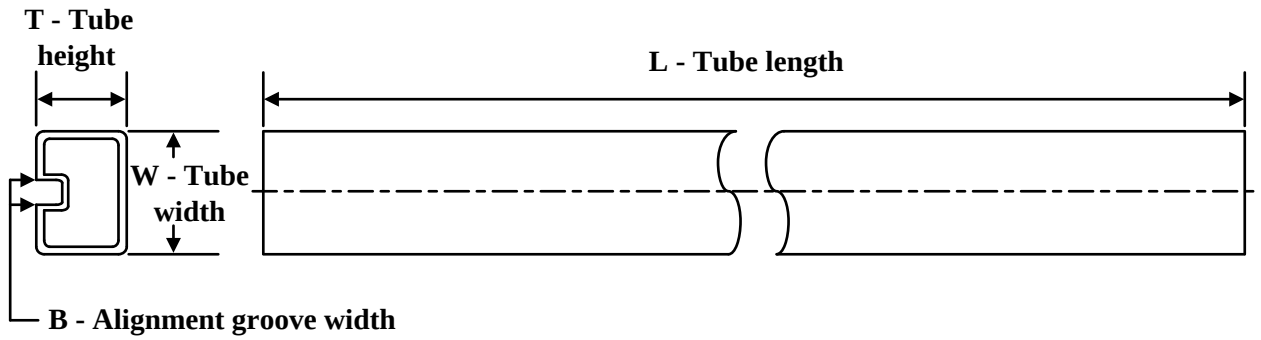
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

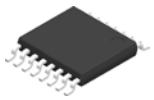
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP38869MHE/NOPB	HTSSOP	PWP	16	250	208.0	191.0	35.0
LP38869MHX/NOPB	HTSSOP	PWP	16	2500	367.0	367.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LP38869MH/NOPB	PWP	HTSSOP	16	92	495	8	2514.6	4.06

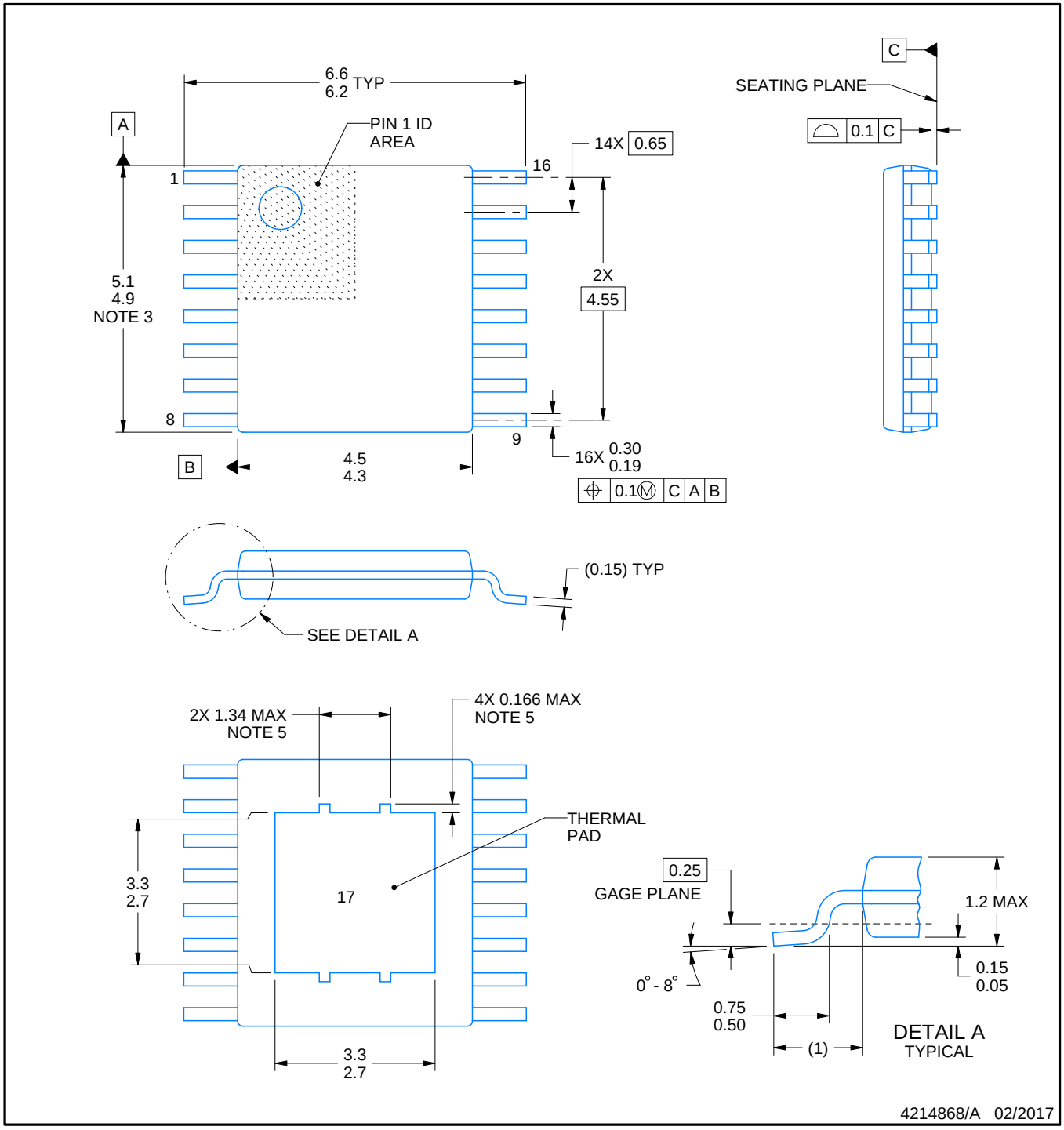


PACKAGE OUTLINE

PWP0016A

PowerPAD ™ HTSSOP - 1.2 mm max height

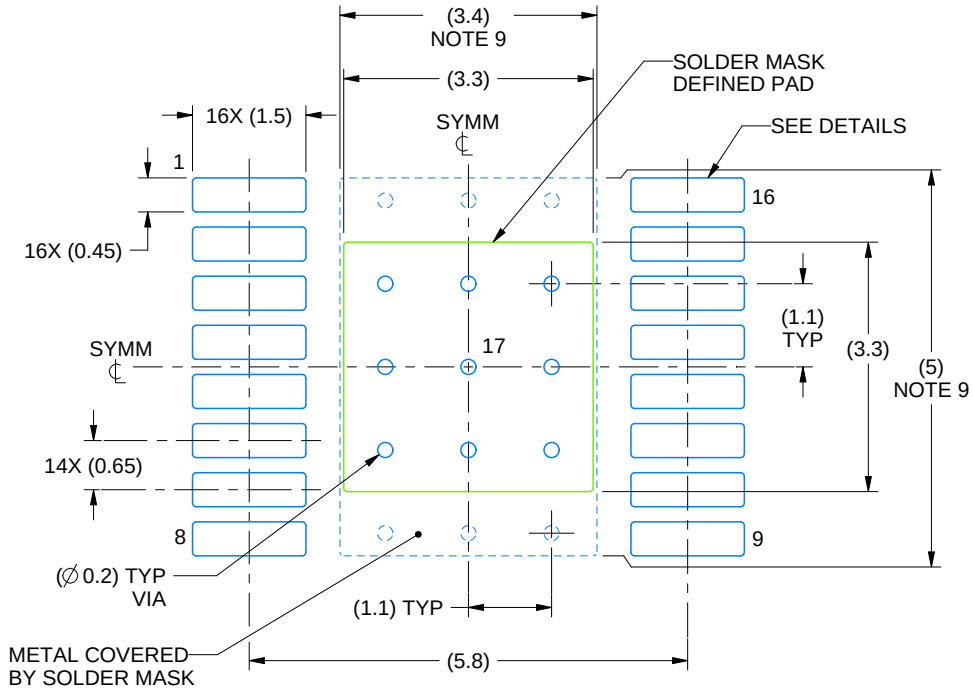
PLASTIC SMALL OUTLINE



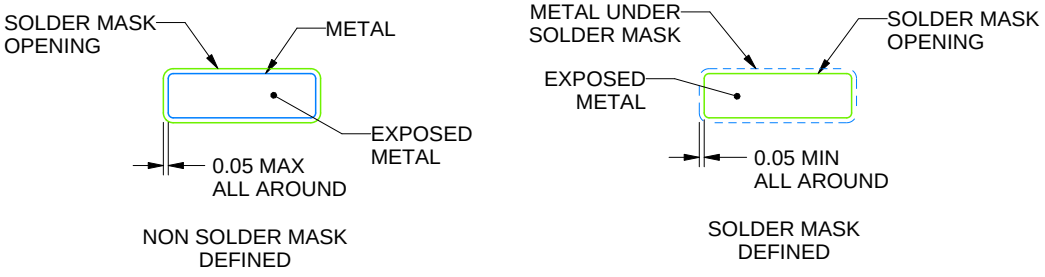
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:10X



SOLDER MASK DETAILS
PADS 1-16

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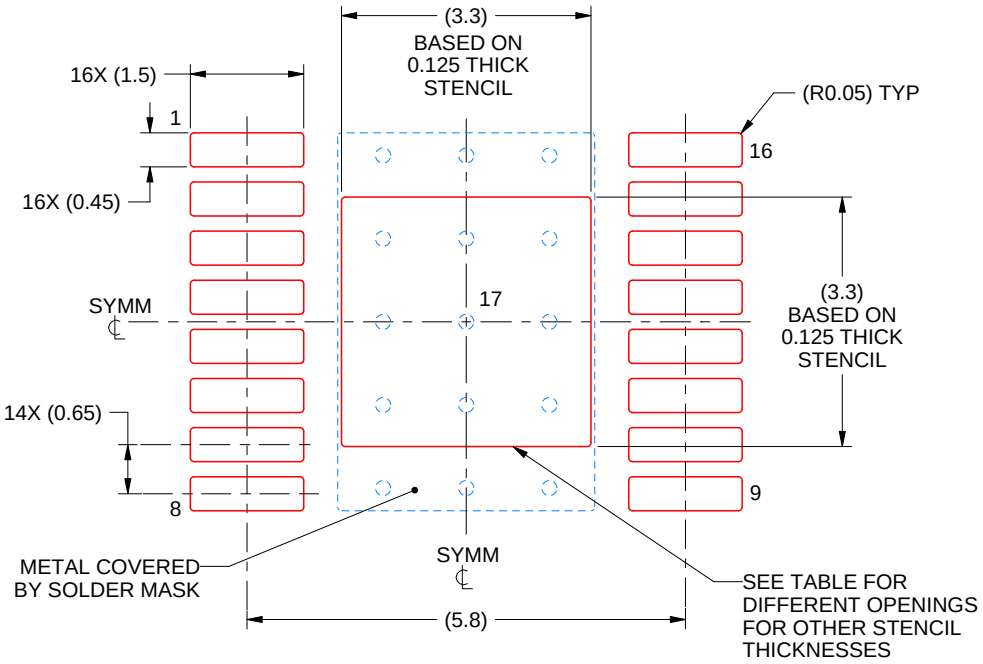
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.69 X 3.69
0.125	3.3 X 3.3 (SHOWN)
0.15	3.01 X 3.01
0.175	2.79 X 2.79

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NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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