www.ti.com

SBOS228E – FEBRUARY 2002 – REVISED DECEMBER 2008

Triple, Wideband, Fixed Gain Video BUFFER AMPLIFIER With Disable

FEATURES

- **FLEXIBLE SUPPLY RANGE:**
  +5V to +12V Single Supply
  ±2.5V to ±6V Dual Supplies
- **INTERNALLY FIXED GAIN: +2 or ±1**
- **HIGH BANDWIDTH (G = +2): 225MHz**
- **LOW SUPPLY CURRENT: 5.1mA/ch**
- **LOW DISABLED CURRENT: 150µA/ch**
- **HIGH OUTPUT CURRENT: 190mA**
- **OUTPUT VOLTAGE SWING: ±4.0V**
- **IMPROVED HIGH-FREQUENCY PINOUT**

APPLICATIONS

- **RGB VIDEO LINE DRIVERS**
- **MULTIPLE LINE VIDEO DAs**
- **PORTABLE INSTRUMENTS**
- **ADC BUFFERS**
- **ACTIVE FILTERS**
- **WIDEBAND DIFFERENTIAL RECEIVERS**
- **IMPROVED UPGRADE TO OPA3682**

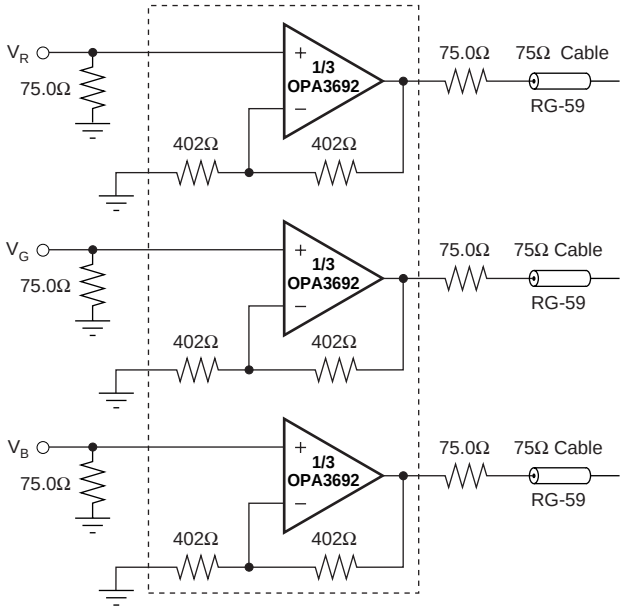
OPA3692 RELATED PRODUCTS

	SINGLES	DUALS	TRIPLES
Voltage-Feedback	OPA690	OPA2690	OPA3690
Current-Feedback	OPA691	OPA2691	OPA3691
Fixed Gain	OPA692	—	OPA3682

DESCRIPTION

The OPA3692 provides an easy-to-use, broadband fixed gain, triple buffer amplifier. Depending on the external connections, the internal resistor network may be used to provide either a fixed gain of +2 video buffer, or a gain of +1 or –1 voltage buffer. Operating on a very low 5.1mA/ch supply current, the OPA3692 offers a slew rate and output power normally associated with a much higher supply current. A new output stage architecture delivers high output current with minimal headroom and crossover distortion. This gives exceptional single-supply operation. Using a single +5V supply, the OPA3692 can deliver a 1V to 4V output swing with over 120mA drive current and > 200MHz bandwidth. This combination of features makes the OPA3692 an ideal RGB line driver or single-supply, triple Analog-to-Digital Converter (ADC) input driver.

The low 5.1mA/ch supply current of the OPA3692 is precisely trimmed at +25°C. This trim, along with low drift over temperature, ensures lower maximum supply current than competing products that report only a room temperature nominal supply current. System power can be further reduced by using the optional disable control pin. Leaving this disable pin open, or holding it HIGH, gives normal operation. If pulled LOW, the OPA3692 supply current drops to less than 150µA/ch while the output goes into a high-impedance state. This feature may be used for power savings.



RGB Line Driver

ABSOLUTE MAXIMUM RATINGS[1]

Power Supply	$\pm 6.5V_{DC}$
Internal Power Dissipation[2]	See Thermal Information
Differential Input Voltage[3]	±1.2V
Input Voltage Range	$\pm V_S$
Storage Temperature Range: D, DBQ	–65°C to +125°C
Lead Temperature (soldering, 10s)	+300°C
Junction Temperature (T_J)	+175°C
ESD Resistance: HBM	2000V
CDM	1500V
MM	200V

NOTES: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. (2) Packages must be derated based on specified θ_{JA}. Maximum T_J must be observed. (3) Noninverting input to internal inverting node.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

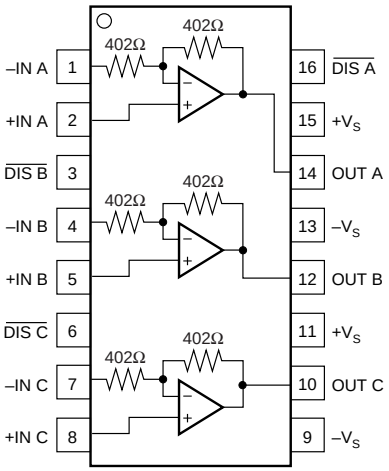
PACKAGE/ORDERING INFORMATION[1]

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
OPA3692	SO-16	D	–40°C to +85°C	OPA3692	OPA3692ID	Rails, 48
"	"	"	"	"	OPA3692IDR	Tape and Reel, 2500
OPA3692	SSOP-16	DBQ	–40°C to +85°C	OPA3692	OPA3692IDBQT	Tape and Reel, 250
"	"	"	"	"	OPA3692IDBQR	Tape and Reel, 2500

NOTE: (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

PIN CONFIGURATION

Top View **OPA3692** **SSOP, SO**



ELECTRICAL CHARACTERISTICS: $V_S = \pm 5V$

Boldface limits are tested at **+25°C.**

G = +2 (–IN grounded) and $R_L = 100\Omega$ (see Figure 1 for AC performance only), unless otherwise noted.

PARAMETER	CONDITIONS	OPA3692ID, OPA3692IDBQ						
		TYP	MIN/MAX OVER TEMPERATURE[1]					
		+25°C	+25°C	0°C to 70°C	–40°C to +85°C	UNITS	MIN/ MAX	TEST LEVEL[2]
AC PERFORMANCE (see Figure 1)								
Small-Signal Bandwidth ($V_O < 0.5V_{PP}$)	G = +1	280				MHz	typ	C
	G = +2	225	185	180	170	MHz	min	B
	G = –1	220				MHz	typ	C
Bandwidth for 0.1dB Gain Flatness	G = +2, $V_O < 0.5V_{PP}$	120	40	35	30	MHz	min	B
Peaking at a Gain of +1	V_O < 0.5Vp-p	0.2	1	1.5	2	dB	max	B
Large-Signal Bandwidth	G = +2, $V_O = 5V_{PP}$	220				MHz	typ	C
Slew Rate	G = +2, 4V Step	2000	1400	1375	1350	V/µs	min	B
Rise-and-Fall Time	G = +2, V_O = 0.5V Step	1.6				ns	typ	C
	G = +2, V_O = 5V Step	1.9				ns	typ	C

ELECTRICAL CHARACTERISTICS: $V_S = \pm 5V$ (Cont.)

Boldface limits are tested at **+25°C.**

G = +2 (–IN grounded) and $R_L = 100\Omega$ (see Figure 1 for AC performance only), unless otherwise noted.

PARAMETER	CONDITIONS	OPA3692ID, OPA3692IDBQ						TEST LEVEL(2)
		TYP	MIN/MAX OVER TEMPERATURE(1)					
		+25°C	+25°C	0°C to 70°C	–40°C to +85°C	UNITS	MIN/ MAX	
AC PERFORMANCE (Cont.)								
Settling Time to 0.02%	G = +2, V_O = 2V Step	12				ns	typ	C
0.1%	G = +2, V_O = 2V Step	8				ns	typ	C
Harmonic Distortion	G = +2, f = 5MHz, $V_O = 2V_{PP}$							
2nd-Harmonic	$R_L = 100\Omega$	–69	–62	–59	–57	dBc	max	B
	$R_L \geq 500\Omega$	–79	–70	–67	–65	dBc	max	B
3rd-Harmonic	$R_L = 100\Omega$	–76	–72	–70	–68	dBc	max	B
	$R_L \geq 500\Omega$	–94	–87	–82	–78	dBc	max	B
Input Voltage Noise	f > 1MHz	1.7	2.5	2.9	3.1	nV/$\sqrt{Hz}$	max	B
Noninverting Input Current Noise	f > 1MHz	12	14	15	15	pA/$\sqrt{Hz}$	max	B
Inverting Input Current Noise (Internal)	f > 1MHz	15	17	18	19	pA/$\sqrt{Hz}$	max	B
Differential Gain	NTSC, $R_L = 150\Omega$	0.07				%	typ	C
	NTSC, $R_L = 37.5\Omega$	0.17				%	typ	C
Differential Phase	NTSC, $R_L = 150\Omega$	0.02				deg	typ	C
	NTSC, $R_L = 37.5\Omega$	0.07				deg	typ	C
Channel-to-Channel Crosstalk	f = 5MHz, Input Referred, All Hostile	–82				dBc	typ	C
DC PERFORMANCE(3)								
Gain Error	G = +1	±0.2				%	typ	C
	G = +2	±0.3	**±1.5**	±1.6	±1.7	%	max	A
	G = –1	±0.2	±1.5	±1.6	±1.7	%	max	B
Internal R_F and R_G								
Maximum		402	**457**	462	464	Ω	max	A
Minimum		402	**347**	342	340	Ω	min	A
Average Drift			0.13	0.13	0.13	%/°C	max	B
Input Offset Voltage	V_{CM} = 0V	±0.8	**±3**	±3.7	±4.3	mV	max	A
Average Offset Voltage Drift	V_{CM} = 0V			±12	±20	µV/°C	max	B
Noninverting Input Bias Current	V_{CM} = 0V	+15	**+35**	+43	+45	µA	max	A
Average Noninverting Input Bias Current Drift	V_{CM} = 0V			–300	–300	nA/°C	max	B
Inverting Input Bias Current	V_{CM} = 0V	±5	**±25**	±30	±40	µA	max	A
Average Inverting Input Bias Current Drift	V_{CM} = 0V			±90	±200	nA°C	max	B
INPUT								
Common-Mode Input Range		±3.5	±3.4	±3.3	±3.2	V	min	B
Noninverting Input Impedance		100 || 2				kΩ || pF	typ	C
OUTPUT								
Voltage Output Swing	No Load	±4.0	**±3.8**	±3.7	±3.6	V	min	A
	100Ω Load	±3.9	**±3.7**	±3.6	±3.3	V	min	A
Current Output, Sourcing		+190	**+160**	+140	+100	mA	min	A
Sinking		–190	**–160**	–140	–100	mA	min	A
Short-Circuit Current		±250				mA	typ	C
Closed-Loop Output Impedance	G = +2, f = 100kHz	0.12				Ω	typ	C
DISABLE/POWER DOWN ($\overline{DIS}$ Pin)								
Power-Down Supply Current (+V_S)	$V_{\overline{DIS}}$ = 0, All Channels	–450	**–900**	–1050	–1200	µA	max	A
Disable Time	$V_{IN} = +1V_{DC}$	1				µs	typ	C
Enable Time	$V_{IN} = +1V_{DC}$	25				ns	typ	C
Off Isolation	G = +2, 5MHz	74				dB	typ	C
Output Capacitance in Disable		4				pF	typ	C
Turn-On Glitch	G = +2, $R_L = 150\Omega$, V_{IN} = 0V	±50				mV	typ	C
Turn-Off Glitch	G = +2, $R_L = 150\Omega$, V_{IN} = 0V	±20				mV	typ	C
Enable Voltage		3.3	**3.5**	3.6	3.7	V	min	A
Disable Voltage		1.8	**1.7**	1.6	1.5	V	max	A
Control Pin Input Bias Current	$V_{\overline{DIS}}$ = 0, Each Channel	75	**130**	150	160	µA	max	A
POWER SUPPLY								
Specified Operating Voltage		±5				V	typ	C
Maximum Operating Voltage Range			**±6**	±6	±6	V	max	A
Maximum Quiescent Current (3 Channels)	$V_S = \pm 5V$	15.3	**15.9**	16.8	17.4	mA	max	A
Minimum Quiescent Current (3 Channels)	$V_S = \pm 5V$	15.3	**14.7**	13.2	12.75	mA	min	A
Power-Supply Rejection Ratio (–PSRR)	Input Referred	58	**52**	50	49	dB	min	A
TEMPERATURE RANGE								
Specification: D, DBQ		–40 to +85				°C	typ	C
Thermal Resistance, θ_{JA}								
D SO-16		100				°C/W	typ	C
DBQ SSOP-16		100				°C/W	typ	C

NOTES: (1) Junction temperature = ambient temperature for low temperature limit and +25°C specifications. Junction temperature = ambient temperature +15°C at high temperature limit specifications. (2) Test Levels: (A) 100% tested at +25°C. Over-temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information. (3) Current is considered positive out-of-node. V_{CM} is the input common-mode voltage.

ELECTRICAL CHARACTERISTICS: V_S = +5V

Boldface limits are tested at **+25°C.**

G = +2 (–IN grounded though 0.1µF) and R_L = 100Ω to V_S/2 (see Figure 2 for AC performance only), unless otherwise noted.

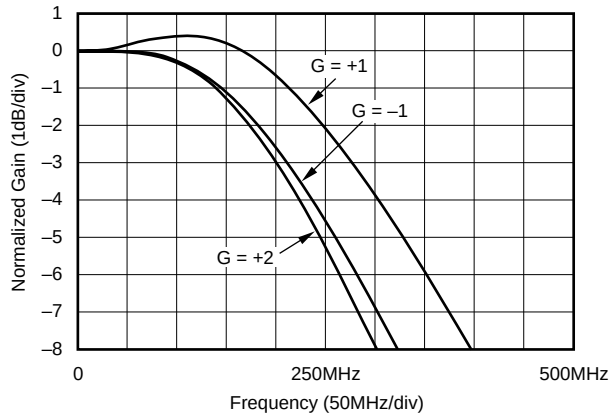
PARAMETER	CONDITIONS	OPA3692ID, OPA3692IDBQ						TEST LEVEL(2)
		TYP	MIN/MAX OVER TEMPERATURE(1)					
		+25°C	+25°C	0°C to 70°C	–40°C to +85°C	UNITS	MIN/ MAX	
AC PERFORMANCE (see Figure 2)								
Small-Signal Bandwidth (V_O < 0.5V_{PP})	G = +1	240				MHz	typ	C
	G = +2	190	168	160	140	MHz	min	B
	G = –1	195				MHz	typ	C
Bandwidth for 0.1dB Gain Flatness	G = +2, V_O < 0.5V_{PP}	90	40	30	25	MHz	min	B
Peaking at a Gain of +1	V_O < 0.5V_{PP}	0.2	1	2.5	3	dB	max	B
Large-Signal Bandwidth	G = +2, V_O = 2V_{PP}	210				MHz	typ	C
Slew Rate	G = +2, 2V Step	830	600	575	550	V/µs	min	B
Rise-and-Fall Time	G = +2, V_O = 0.5V Step	2.0				ns	typ	C
	G = +2, V_O = 2V Step	2.3				ns	typ	C
Settling Time to 0.02%	G = +2, V_O = 2V Step	14				ns	typ	C
0.1%	G = +2, V_O = 2V Step	10				ns	typ	C
Harmonic Distortion	G = +2, f = 5MHz, V_O = 2V_{PP}							
2nd-Harmonic	R_L = 100Ω to V_S/2	–66	–58	–57	–56	dBc	max	B
	R_L ≥ 500Ω to V_S/2	–73	–65	–63	–62	dBc	max	B
3rd-Harmonic	R_L = 100Ω to V_S/2	–72	–68	–67	–65	dBc	max	B
	R_L ≥ 500Ω to V_S/2	–77	–72	–70	–69	dBc	max	B
Input Voltage Noise	f > 1MHz	1.7	2.5	2.9	3.1	nV/√Hz	max	B
Noninverting Input Current Noise	f > 1MHz	12	14	15	15	pA/√Hz	max	B
Inverting Input Current Noise	f > 1MHz	15	17	18	19	pA/√Hz	max	B
DC PERFORMANCE(3)								
Gain Error	G = +1	±0.2				%	typ	C
	G = +2	±0.3	**±1.5**	±1.6	±1.7	%	max	A
	G = –1	±0.2	±1.5	±1.6	±1.7	%	max	B
Internal R_F and R_G								
Minimum		402	457	462	464	Ω	min	B
Maximum		402	347	342	340	Ω	max	B
Average Drift			0.13	0.13	0.13	%/°C	max	B
Input Offset Voltage	V_{CM} = 2.5V	±0.8	**±3.5**	±4.1	±4.8	mV	max	A
Average Offset Voltage Drift	V_{CM} = 2.5V			±12	±20	µV/°C	max	B
Noninverting Input Bias Current	V_{CM} = 2.5V	+20	**+40**	+46	+56	µA	max	A
Average Noninverting Input Bias Current Drift	V_{CM} = 2.5V			–250	–250	nA/°C	max	B
Inverting Input Bias Current	V_{CM} = 2.5V	±5	**±20**	±25	±35	µA	max	A
Average Inverting Input Bias Current Drift	V_{CM} = 2.5V			±112	±200	nA°C	max	B
INPUT								
Least Positive Input Voltage		1.5	1.6	1.7	1.8	V	max	B
Most Positive Input Voltage		3.5	3.4	3.3	3.2	V	min	B
Noninverting Input Impedance		100 || 2				kΩ || pF	typ	C
OUTPUT								
Most Positive Output Voltage	No Load	4.0	**3.8**	3.7	3.5	V	min	A
	R_L = 100Ω	3.9	**3.7**	3.6	3.4	V	min	A
Least Positive Output Voltage	No Load	1.0	**1.2**	1.3	1.5	V	max	A
	R_L = 100Ω	1.1	**1.3**	1.4	1.6	V	max	A
Current Output, Sourcing		+160	**+120**	+100	+80	mA	min	A
Sinking		–160	**–120**	–100	–80	mA	min	A
Short-Circuit Current		±250				mA	typ	C
Output Impedance	G = +2, f = 100kHz	0.12				Ω	typ	C
DISABLE/POWER DOWN ($\overline{DIS}$ Pin)								
Power-Down Supply Current (+V_S)	$V_{\overline{DIS}}$ = 0, All Channels	–450	**–900**	–1050	–1200	µA	max	A
Off Isolation	G = +2, 5MHz	65				dB	typ	C
Output Capacitance in Disable		4				pF	typ	C
Turn-On Glitch	G = +2, R_L = 150Ω, V_{IN} = 2.5V	±50				mV	typ	B
Turn-Off Glitch	G = +2, R_L = 150Ω, V_{IN} = 2.5V	±20				mV	typ	B
Enable Voltage		3.3	**3.5**	3.6	3.7	V	min	A
Disable Voltage		1.8	**1.7**	1.6	1.5	V	max	A
Control Pin Input Bias Current ($\overline{DIS}$)	$V_{\overline{DIS}}$ = 0, Each Channel	75	130	150	160	µA	typ	C
POWER SUPPLY								
Specified Single-Supply Operating Voltage		5				V	typ	C
Maximum Single-Supply Operating Voltage			**12**	12	12	V	max	A
Maximum Quiescent Current (3 Channels)	V_S = +5V	13.5	**14.4**	15.3	15.9	mA	max	A
Minimum Quiescent Current (3 Channels)	V_S = +5V	13.5	**12.3**	11.4	11.0	mA	min	A
Power-Supply Rejection Ratio (+PSRR)	Input Referred	62				dB	typ	C
TEMPERATURE RANGE								
Specification: D, DBQ		–40 to +85				°C	typ	C
Thermal Resistance, θ_{JA}								
D SO-16		100				°C/W	typ	C
DBQ SSOP-16		100				°C/W	typ	C

NOTES: (1) Junction temperature = ambient temperature for low temperature limit and +25°C specifications. Junction temperature = ambient temperature +15°C at high temperature limit specifications. (2) Test Levels: (A) 100% tested at +25°C. Over-temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information. (3) Current is considered positive out-of-node. V_{CM} is the input common-mode voltage.

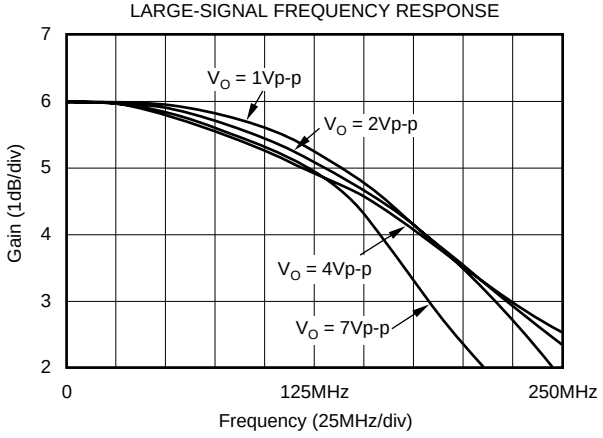
TYPICAL CHARACTERISTICS: $V_S = \pm 5V$

T_A = +25°C, G = +2 (–In grounded), and R_L = 100Ω, (see Figure 1 for AC performance only), unless otherwise noted.

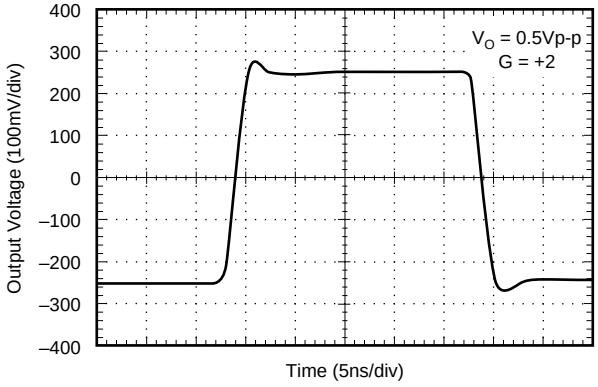
SMALL-SIGNAL FREQUENCY RESPONSE



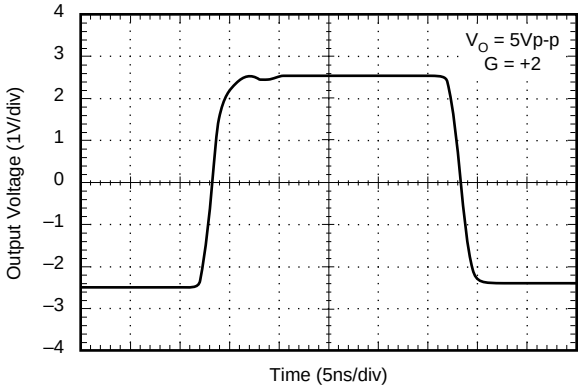
LARGE-SIGNAL FREQUENCY RESPONSE



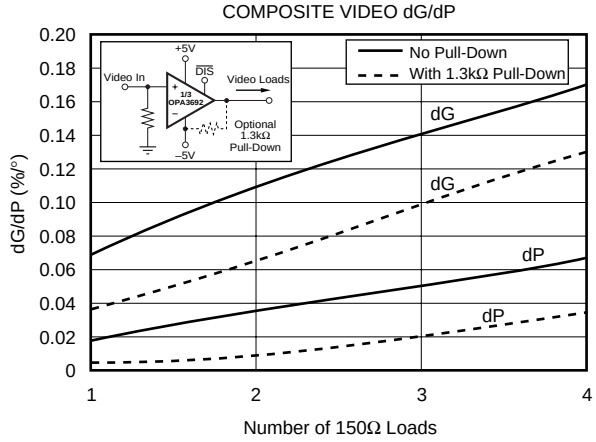
SMALL-SIGNAL PULSE RESPONSE



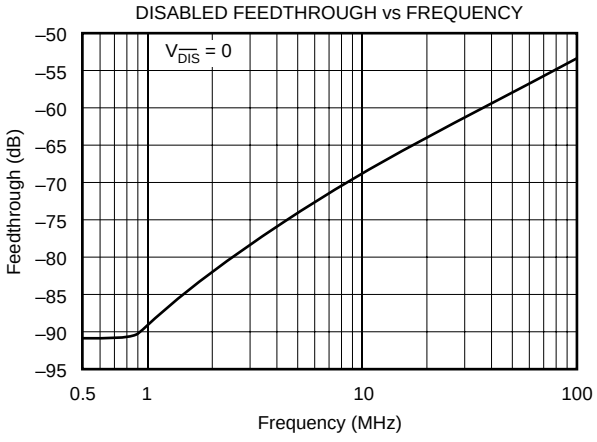
LARGE-SIGNAL PULSE RESPONSE



COMPOSITE VIDEO dG/dP



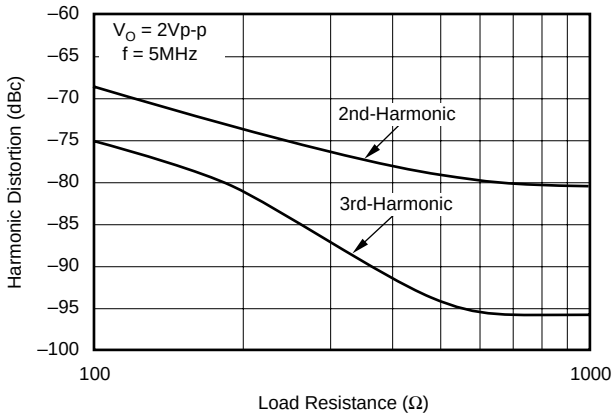
DISABLED FEEDTHROUGH vs FREQUENCY



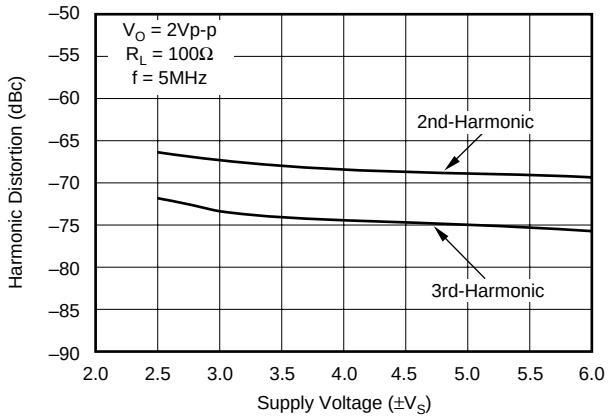
TYPICAL CHARACTERISTICS: $V_S = \pm 5V$ (Cont.)

T_A = +25°C, G = +2 (–In grounded), and R_L = 100Ω, (see Figure 1 for AC performance only), unless otherwise noted.

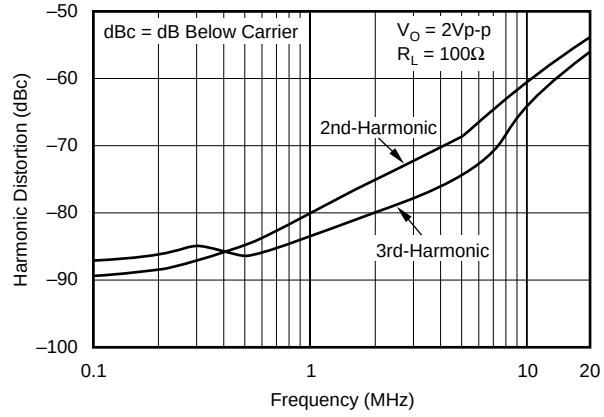
HARMONIC DISTORTION vs LOAD RESISTANCE



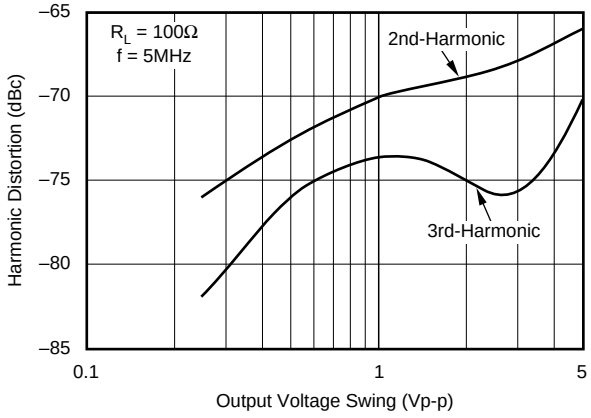
HARMONIC DISTORTION vs SUPPLY VOLTAGE



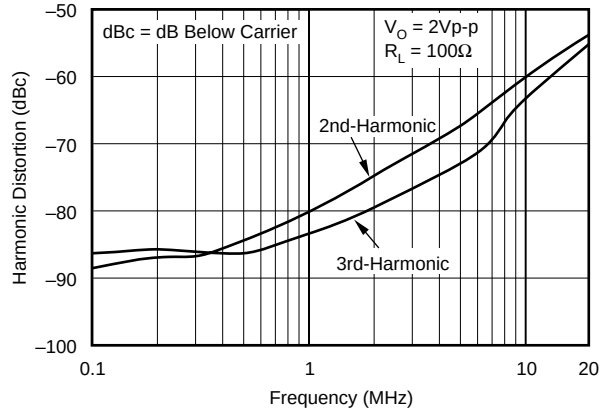
HARMONIC DISTORTION vs FREQUENCY (G = +2)



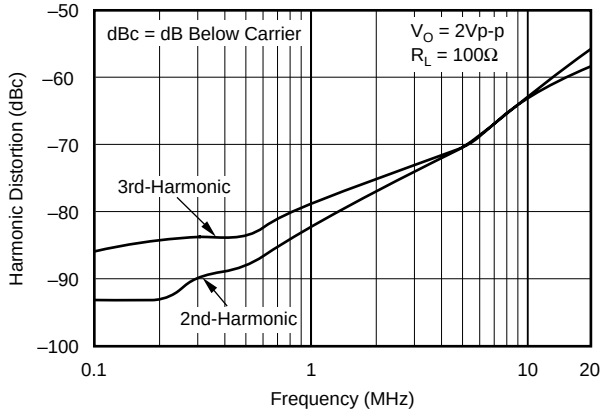
HARMONIC DISTORTION vs OUTPUT VOLTAGE



HARMONIC DISTORTION vs FREQUENCY (G = –1)



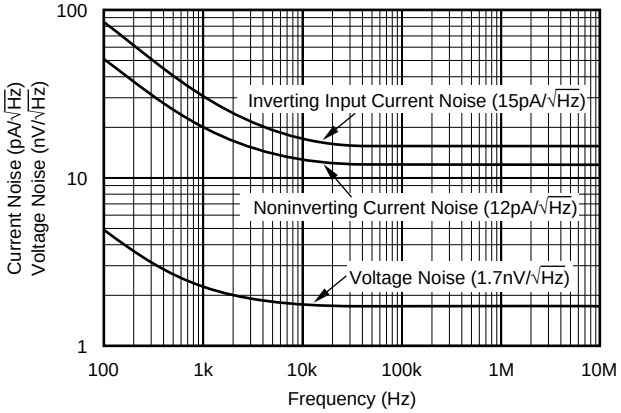
HARMONIC DISTORTION vs FREQUENCY (G = +1)



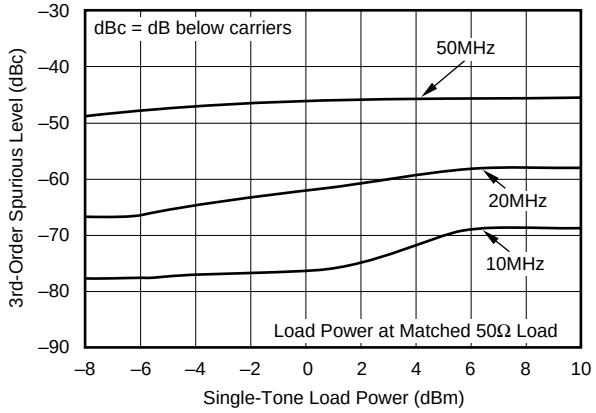
TYPICAL CHARACTERISTICS: $V_S = \pm 5V$ (Cont.)

T_A = +25°C, G = +2 (–In grounded), and R_L = 100Ω, (see Figure 1 for AC performance only), unless otherwise noted.

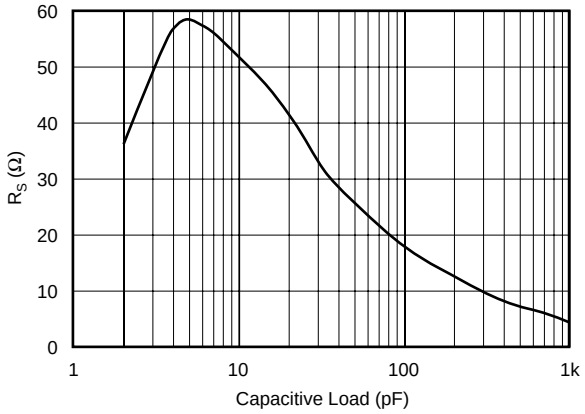
INPUT VOLTAGE AND CURRENT NOISE DENSITY



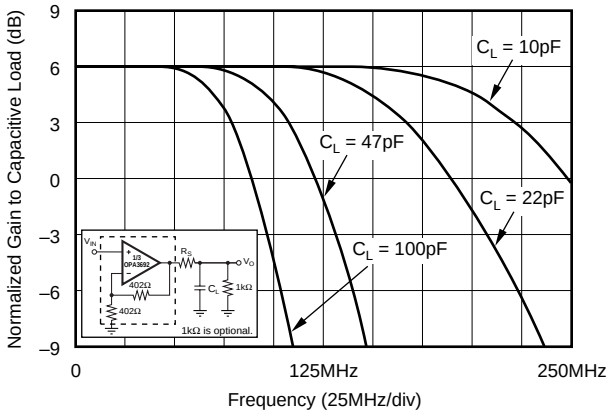
2-TONE, 3RD-ORDER
INTERMODULATION SPURIOUS



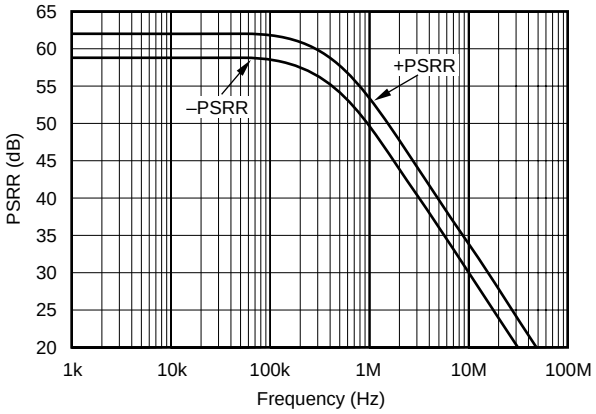
RECOMMENDED R_S vs CAPACITIVE LOAD



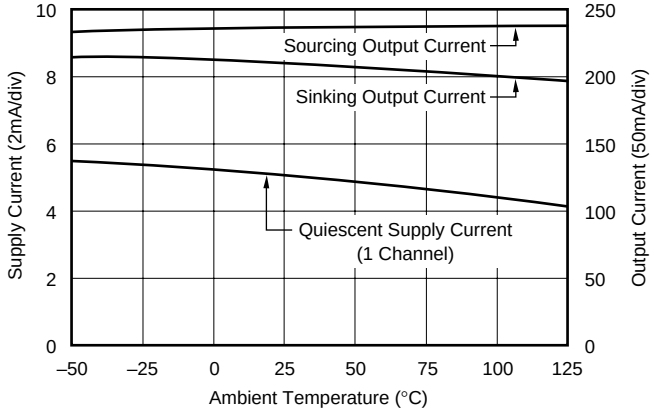
FREQUENCY RESPONSE vs CAPACITIVE LOAD



POWER-SUPPLY REJECTION RATIO vs FREQUENCY



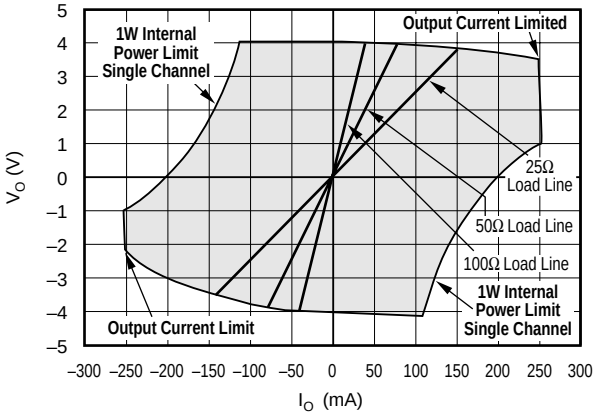
SUPPLY AND OUTPUT CURRENT vs TEMPERATURE



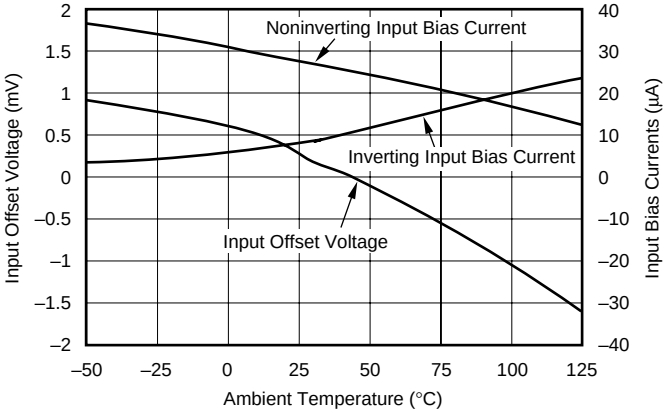
TYPICAL CHARACTERISTICS: $V_S = \pm 5V$ (Cont.)

T_A = +25°C, G = +2 (–In grounded), and R_L = 100Ω, (see Figure 1 for AC performance only), unless otherwise noted.

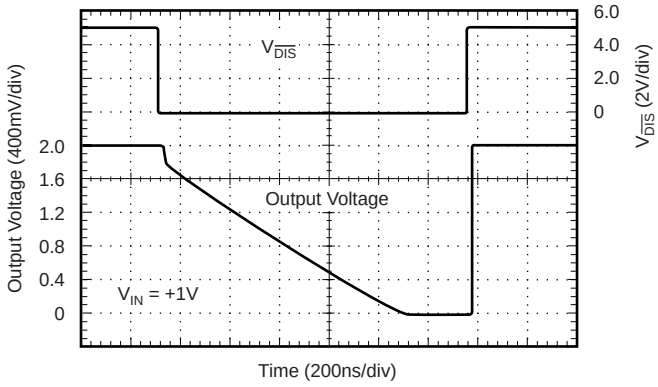
OUTPUT VOLTAGE AND CURRENT LIMITATIONS



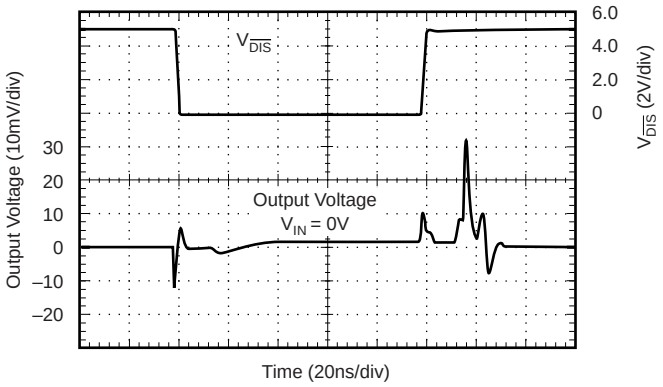
TYPICAL DC DRIFT OVER TEMPERATURE



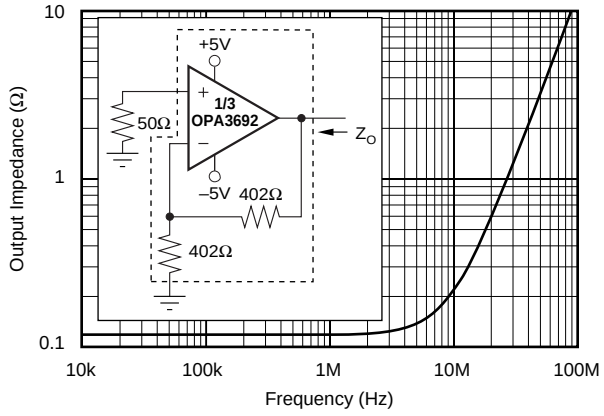
LARGE-SIGNAL DISABLE/ENABLE RESPONSE



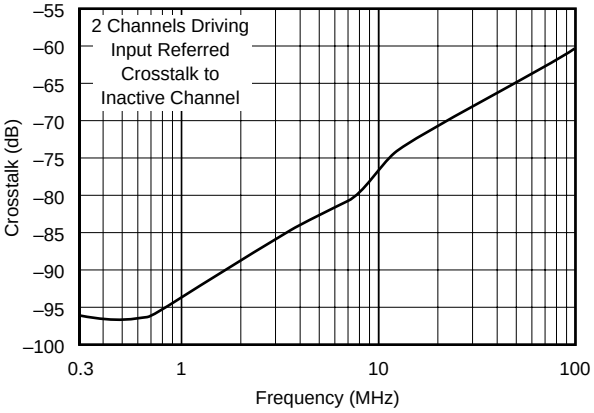
DISABLE/ENABLE GLITCH



CLOSED-LOOP OUTPUT IMPEDANCE vs FREQUENCY



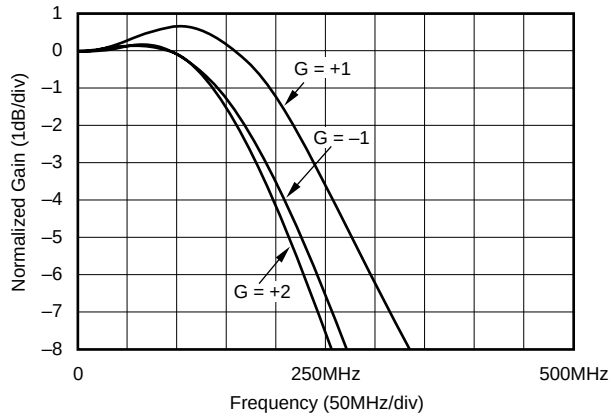
ALL HOSTILE CROSSTALK



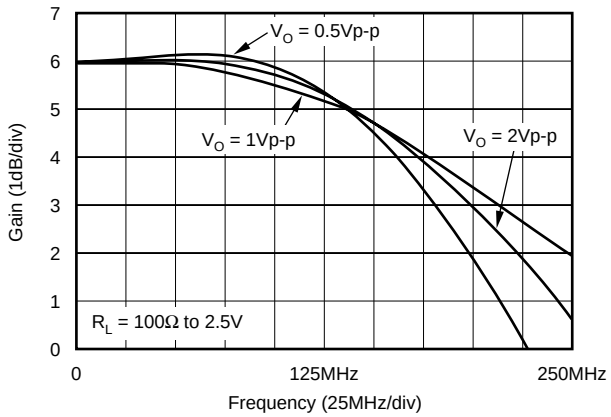
TYPICAL CHARACTERISTICS: V_S = +5V

T_A = +25°C, G = +2 (–In grounded), and R_L = 100Ω, (see Figure 1 for AC performance only), unless otherwise noted.

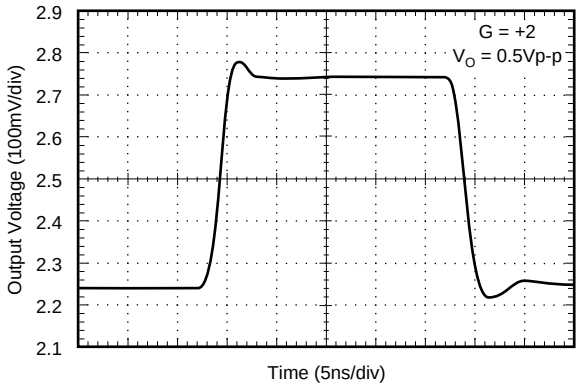
SMALL-SIGNAL FREQUENCY RESPONSE



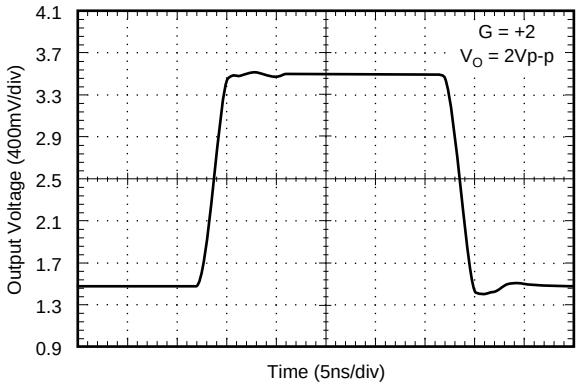
LARGE-SIGNAL FREQUENCY RESPONSE



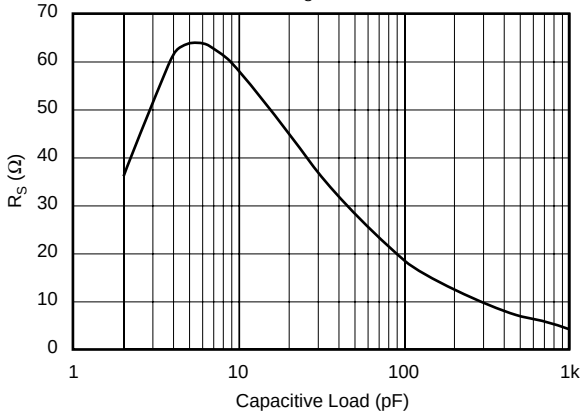
SMALL-SIGNAL PULSE RESPONSE



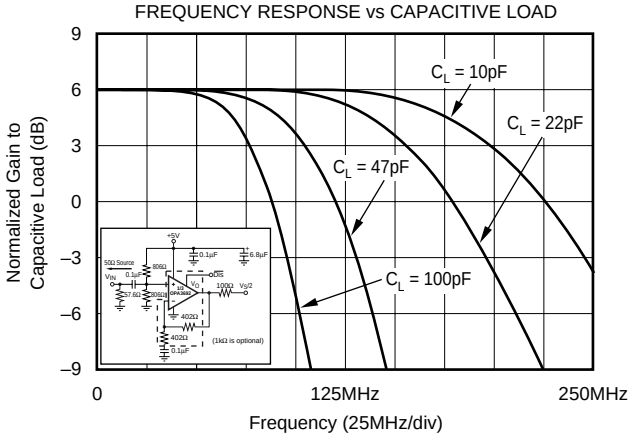
LARGE-SIGNAL PULSE RESPONSE



RECOMMENDED R_S vs CAPACITIVE LOAD



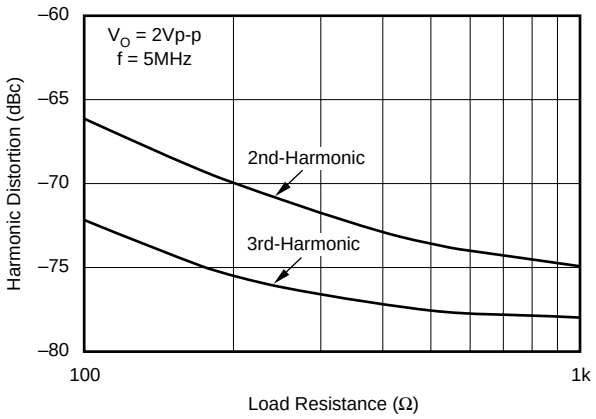
FREQUENCY RESPONSE vs CAPACITIVE LOAD



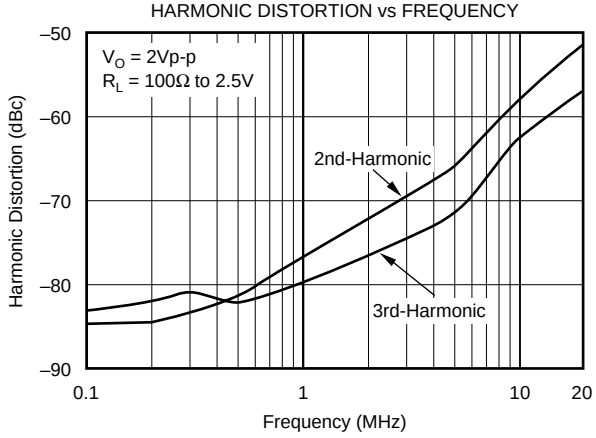
TYPICAL CHARACTERISTICS: V_S = +5V (Cont.)

T_A = +25°C, G = +2 (–In grounded), and R_L = 100Ω, (see Figure 1 for AC performance only), unless otherwise noted.

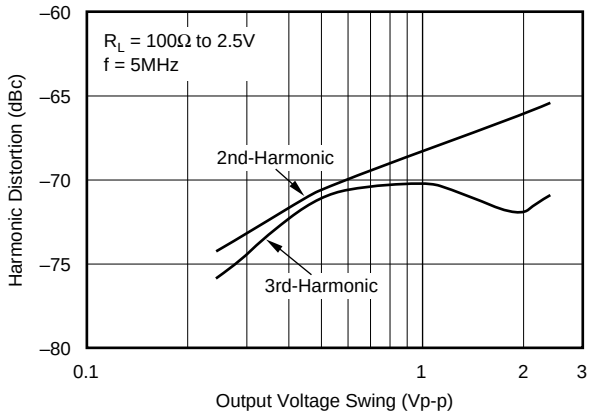
HARMONIC DISTORTION vs LOAD RESISTANCE



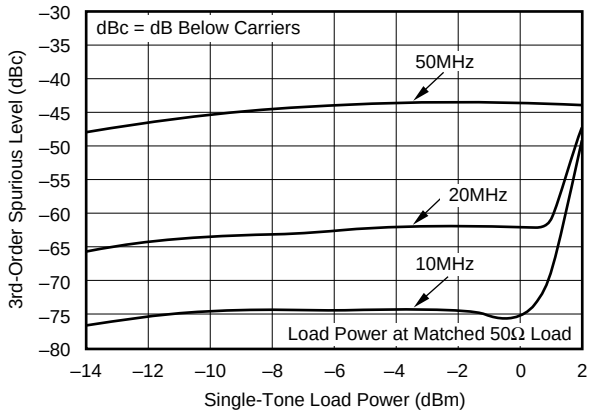
HARMONIC DISTORTION vs FREQUENCY



HARMONIC DISTORTION vs OUTPUT VOLTAGE



2-TONE, 3RD-ORDER
INTERMODULATION SPURIOUS



APPLICATIONS INFORMATION

WIDEBAND BUFFER OPERATION

The OPA3692 gives the exceptional AC performance of a wideband, current-feedback op amp with a highly linear, high-power output stage. It features internal R_F and R_G resistors that make it easy to select a gain of +2, +1, or –1 without external resistors. Requiring only 5.1mA/ch quiescent current, the OPA3692 swings to within 1V of either supply rail and delivers in excess of 160mA at room temperature. This low output headroom requirement, along with supply voltage independent biasing, gives remarkable +5V single-supply operation. The OPA3692 will deliver greater than 200MHz bandwidth driving a 2Vp-p output into 100Ω on a +5V single supply. Previous boosted output stage amplifiers have typically suffered from very poor crossover distortion as the output current goes through zero. The OPA3692 achieves a comparable power gain with much better linearity.

Figure 1 shows the DC-coupled, gain of +2, dual power-supply circuit configuration used as the basis of the ±5V Electrical and Typical Characteristics. For test purposes, the input impedance is set to 50Ω with a resistor to ground and the output impedance is set to 50Ω with a series output resistor. Voltage swings reported in the specifications are taken directly at the input and output pins while load powers (dBm) are defined at a matched 50Ω load. For the circuit of Figure 1, the total effective load will be 100Ω || 804Ω = 89Ω. The disable control line ($\overline{DIS}$) is typically left open to ensure normal amplifier operation. In addition to the usual power-supply decoupling capacitors to ground, a 0.1µF capacitor can be included between the two power-supply pins. This optional capacitor typically improves the 2nd-harmonic distortion performance by 3dB to 6dB.

Figure 2 shows the AC-coupled, gain of +2, single-supply circuit configuration used as the basis of the +5V Electrical and Typical Characteristics. Though not a rail-to-rail design, the OPA3692 requires minimal input and output voltage headroom compared to other very wideband, current-feedback op amps. It will deliver a 3Vp-p output swing on a single +5V supply with greater than 150MHz bandwidth. The key requirement of broadband single-supply operation is to maintain input and output signal swings within the usable voltage ranges at both the input and the output. The circuit in Figure 2 establishes an input midpoint bias using a simple resistive divider from the +5V supply (two 806Ω resistors). The input signal is then AC-coupled into this midpoint voltage bias. The input voltage can swing to within 1.5V of either supply pin, giving a 2Vp-p input signal range centered between the supply pins. The input impedance matching resistor (57.6Ω) used for testing is adjusted to give a 50Ω input match when the parallel combination of the biasing divider network is included. The gain resistor (R_G) is AC-coupled, giving the circuit a DC gain of +1, which puts the input DC bias voltage (2.5V) on the output as well. Again, on a single +5V supply, the output voltage can swing to within 1V of either supply pin while delivering more than 120mA output current. A demanding 100Ω load to a midpoint bias is used in this characterization circuit. The new output stage used in the OPA3692 can deliver large bipolar output currents into this midpoint load with minimal crossover distortion, as shown by the +5V supply, 3rd-harmonic distortion plots. Although Figure 2 shows a single +5V operation, this same circuit is suitable for applications up to a single +12V supply.

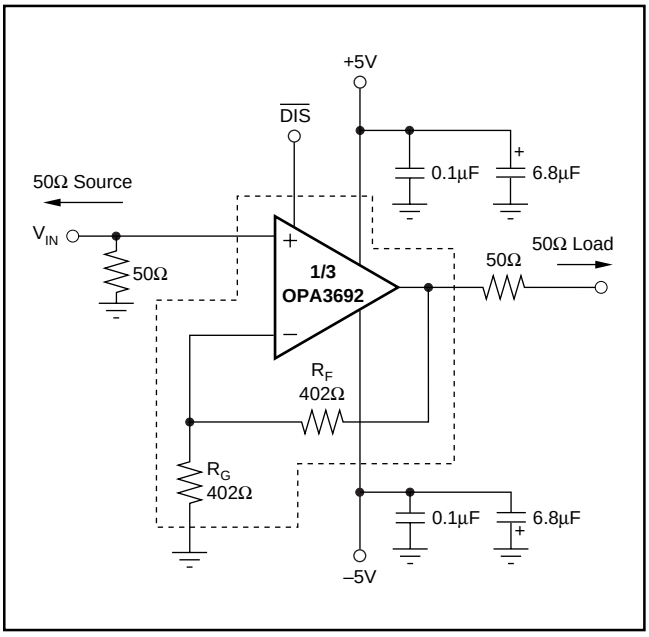


FIGURE 1. DC-Coupled, G = +2, Bipolar Supply, Specification and Test Circuit.

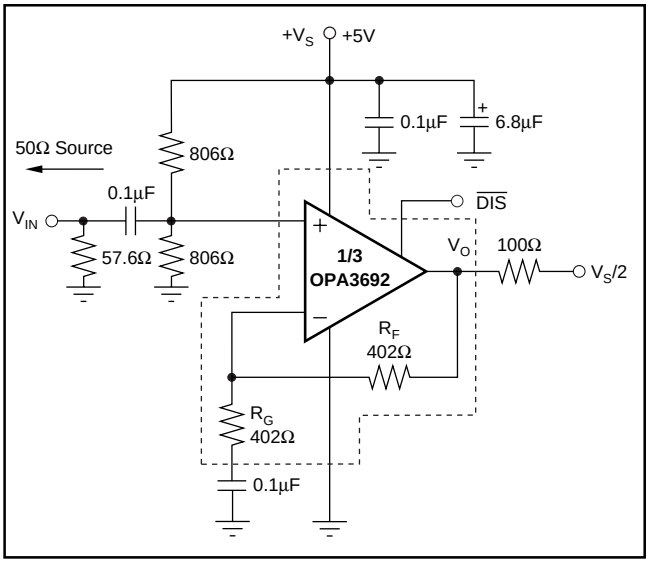


FIGURE 2. AC-Coupled, G = +2, Single-Supply Specification and Test Circuit.

VIDEO RGB AMPLIFIER

The front page shows an RGB amplifier based on the OPA3692. The package pinout supports a signal flow-through printed circuit board (PCB). The internal resistors simplify the PCB even more, while maintaining good gain accuracy. For systems that need to conserve power, the total supply current for the disabled OPA3692 is only 450µA.

This triple op amp could also be used to drive triple video ADCs to digitize component video.

HIGH-SPEED INSTRUMENTATION AMPLIFIER

Figure 3 shows an instrumentation amplifier based on the OPA3692. The offset matching between inputs makes this an attractive input stage for this application. The differential-to-single-ended gain for this circuit is 2.0V/V. The inputs are high impedance, with only 1pF to ground at each input. The loads on the OPA3692 outputs are equal for the best harmonic distortion possible.

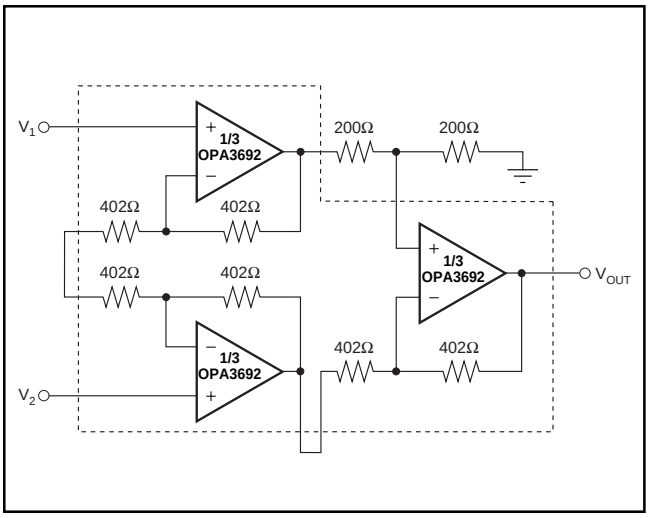


FIGURE 3. High-Speed Instrumentation Amplifier.

As shown in Figure 4, the OPA3692 used as an instrumentation amplifier has a 240MHz, –3dB bandwidth. This plot has been made for a 1Vp-p output signal using a low-impedance differential input source.

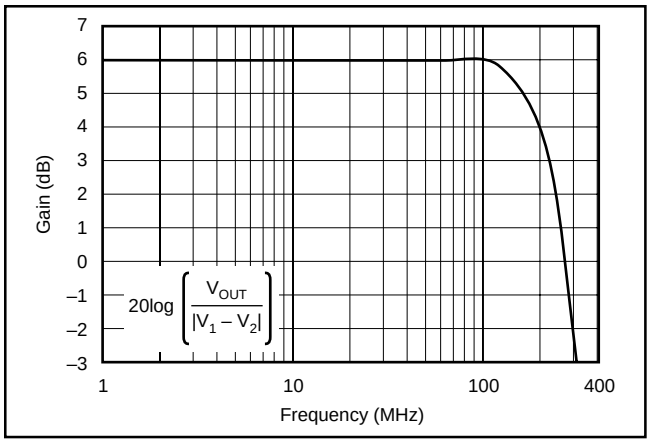


FIGURE 4. High-Speed Instrumentation Amplifier Response.

MULTIPLEXED CONVERTER DRIVER

The converter driver in Figure 5 multiplexes among the three input signals. The OPA3692s enable and disable times support multiplexing among video signals. The make-before-break disable characteristic of the OPA3692 ensures that the output is always under control. To avoid large switching glitches, switch during the sync or retrace portions of the video signal—the two inputs should be almost equal at these times. The output is always under control, so the switching glitches for two 0V inputs are < 20mV. With standard video signals levels at the inputs, the maximum differential voltage across the disabled inputs will not exceed the ±1.2V maximum rating.

The output resistors isolate the outputs from each other when switching between channels. The feedback network of the disabled channels forms part of the load seen by the enabled amplifier, attenuating the signal slightly.

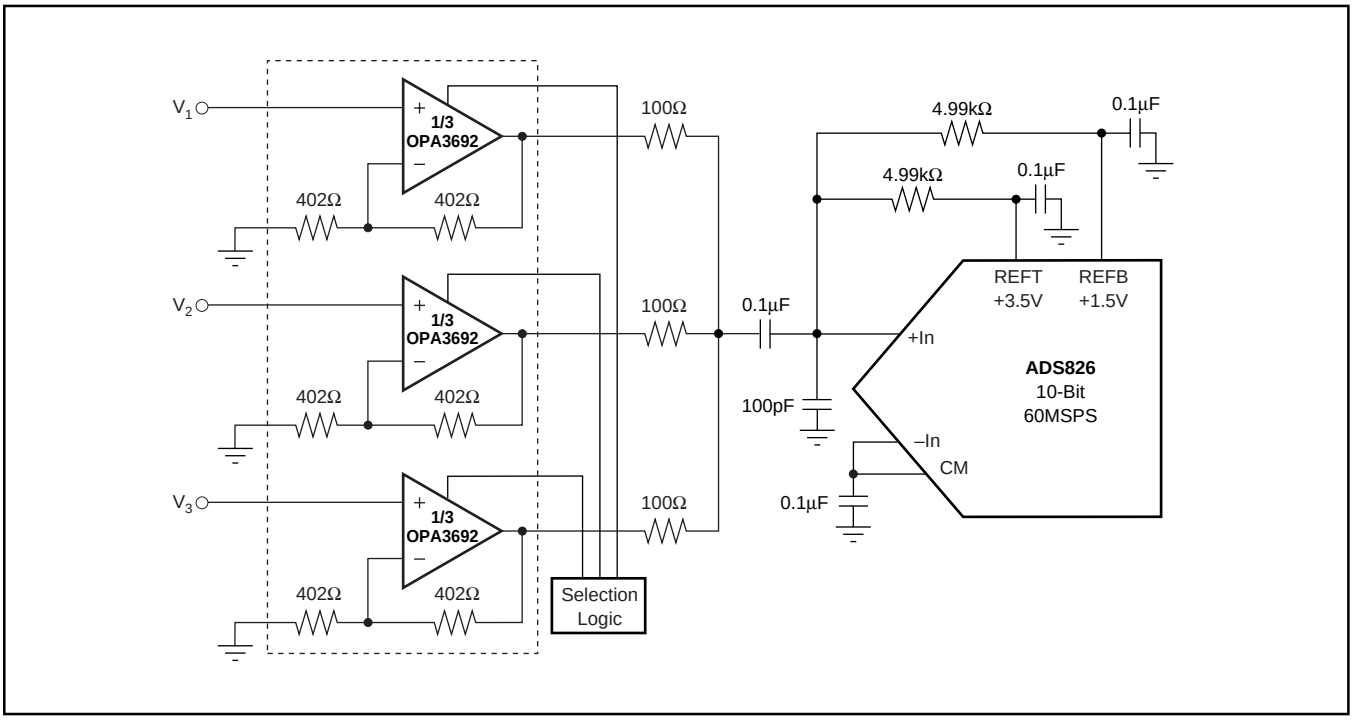


FIGURE 5. Multiplexed Converter Driver.

LOW-PASS FILTER

The circuit in Figure 6 realizes a 7th-order Butterworth low-pass filter with a –3dB bandwidth of 20MHz. This filter is based on the KRC active filter topology, which uses an amplifier with the fixed gain ≥ 1. The OPA3692 makes a good amplifier for this type of filter. The component values have been adjusted to compensate for the parasitic effects of the op amp.

DESIGN-IN TOOLS

DEMONSTRATION FIXTURES

Two PCBs are available to assist in the initial evaluation of circuit performance using the OPA3692 in its two package options. Both of these are offered free of charge as unpopulated PCBs, delivered with a user's guide. The summary information for these fixtures is shown in Table I.

PRODUCT	PACKAGE	ORDERING NUMBER	LITERATURE NUMBER
OPA3692IDBQ	SSOP-16	DEM-OPA-SSOP-3B	SBOU006
OPA3692ID	SO-16	DEM-OPA-SO-3A	SBOU007

TABLE I. OPA3692 Demonstration Boards.

The demonstration fixtures can be requested at the Texas Instruments web site at (www.ti.com) through the OPA3692 product folder.

MACROMODELS AND APPLICATIONS SUPPORT

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. This is particularly true for video and RF amplifier circuits where parasitic capacitance and inductance can have a major effect on circuit performance. A SPICE model for the OPA692 is available through the Texas Instruments web site at www.ti.com. Use three of these models to simulate the OPA3692. These models do a good job of predicting small-signal AC and transient performance under a wide variety of operating conditions. They do not do as well in predicting the harmonic distortion or dG/dP characteristics. These models do not attempt to distinguish between the package types in their small-signal AC performance.

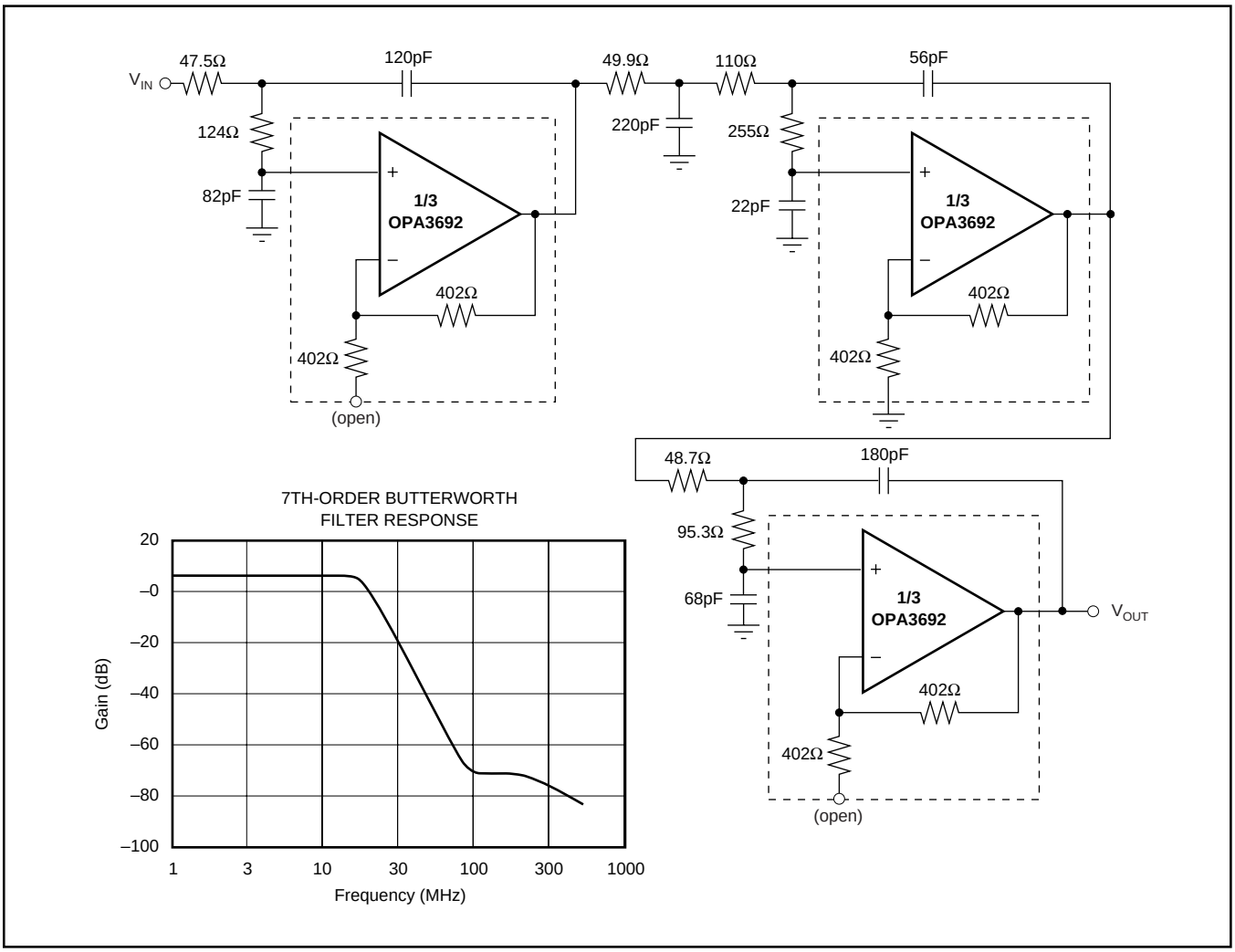


FIGURE 6. 7th-Order Butterworth Filter.

OPERATING SUGGESTIONS

GAIN SETTING

Setting the gain with the OPA3692 is very easy. For a gain of +2, ground the –IN pin and drive the +IN pin with the signal. For a gain of +1, leave the –IN pin open and drive the +IN pin with the signal. For a gain of –1, ground the +IN pin and drive the –IN pin with the signal. As the internal resistor values (not their ratios) change significantly over temperature and process, external resistors should not be used to modify the gain.

OUTPUT CURRENT AND VOLTAGE

The OPA3692 provides output voltage and current capabilities that are unsurpassed in a low-cost monolithic op amp. Under no-load conditions at 25°C, the output voltage typically swings closer than 1V to either supply rail; the tested swing limit is within 1.2V of either rail. Into a 15Ω load (the minimum tested load), it is tested to deliver more than ±160mA.

The specifications described previously, though familiar in the industry, consider voltage and current limits separately. In many applications, it is the voltage • current, or V-I product, which is more relevant to circuit operation. Refer to the *Output Voltage and Current Limitations* plot in the Typical Characteristics. The X- and Y-axes of this graph show the zero-voltage output current limit and the zero-current output voltage limit, respectively. The four quadrants give a more detailed view of the OPA3692 output drive capabilities, noting that the graph is bounded by a safe operating area of 1W maximum internal power dissipation. Superimposing resistor load lines onto the plot shows that the OPA3692 can drive ±2.5V into 25Ω or ±3.5V into 50Ω without exceeding the output capabilities or the 1W dissipation limit. A 100Ω load line (the standard test circuit load) shows the full ±3.9V output swing capability, as shown in the Electrical Characteristics.

The minimum specified output voltage and current over-temperature are set by worst-case simulations at the cold temperature extreme. Only at cold start-up does the output current and voltage decrease to the numbers shown in the Electrical Characteristic tables. As the output transistors deliver power, their junction temperatures increase, decreasing their V_{BE}s (increasing the available output voltage swing) and increasing their current gains (increasing the available output current). In steady-state operation, the available output voltage and current is always greater than that shown in the over-temperature specifications because the output stage junction temperatures are higher than the minimum specified operating ambient.

To protect the output stage from accidental shorts to ground and the power supplies, output short-circuit protection is included in the OPA3692. This circuit acts to limit the maximum source or sink current to approximately 250mA.

DRIVING CAPACITIVE LOADS

One of the most demanding, but yet very common load conditions for an op amp is capacitive loading. Often, the capacitive load is the input of an ADC—including additional external capacitance that may be recommended to improve ADC linearity. A high-speed amplifier like the OPA3692 can be very susceptible to decreased stability and closed-loop response peaking when a capacitive load is placed directly on the output pin. When the amplifier open-loop output resistance is considered, this capacitive load introduces an additional pole in the signal path that can decrease the phase margin. Several external solutions to this problem have been suggested. When the primary considerations are frequency response flatness, pulse response fidelity, and/or distortion, the simplest and most effective solution is to isolate the capacitive load from the feedback loop by inserting a series isolation resistor between the amplifier output and the capacitive load. This does not eliminate the pole from the loop response, but rather shifts it and adds a zero at a higher frequency. The additional zero acts to cancel the phase lag from the capacitive load pole, thus increasing the phase margin and improving stability.

The Typical Characteristics show the recommended R_S versus capacitive load and the resulting frequency response at the load. Parasitic capacitive loads greater than 2pF can begin to degrade the performance of the OPA3692. Long PCB traces, unmatched cables, and connections to multiple devices can easily cause this value to be exceeded. Always consider this effect carefully, and add the recommended series resistor as close as possible to the OPA3692 output pin (see the Board Layout Guidelines section).

DISTORTION PERFORMANCE

The OPA3692 provides good distortion performance into a 100Ω load on ±5V supplies. Relative to alternative solutions, it provides exceptional performance into lighter loads and/or operating on a single +5V supply. Generally, until the fundamental signal reaches very high frequency or power levels, the 2nd-harmonic dominates the distortion with a negligible 3rd-harmonic component. Focusing then on the 2nd-harmonic, increasing the load impedance improves distortion directly. Remember that the total load includes the feedback network in the noninverting configuration (see Figure 1); this is the sum $R_F + R_G$, whereas in the inverting configuration, it is just R_F. Also, providing an additional supply decoupling capacitor (0.1µF) between the supply pins (for bipolar operation) improves the 2nd-order distortion slightly (3dB to 6dB).

In most op amps, increasing the output voltage swing increases harmonic distortion directly. The Typical Characteristics show the 2nd-harmonic increasing at a little less than the expected 2X rate while the 3rd-harmonic increases at a little less than the expected 3X rate. Where the test power doubles, the 2nd-harmonic increases only by less than the expected 6dB, whereas the 3rd-

harmonic increases by less than the expected 12dB. This also shows up in the 2-tone, 3rd-order intermodulation spurious (IM3) response curves. The 3rd-order spurious levels are extremely low at low output power levels. The output stage continues to hold them low even as the fundamental power reaches very high levels. As the Typical Characteristics show, the spurious intermodulation powers do not increase as predicted by a traditional intercept model. As the fundamental power level increases, the dynamic range does not decrease significantly. For two tones centered at 20MHz, with 10dBm/tone into a matched 50Ω load (that is, 2Vp-p for each tone at the load, which requires 8Vp-p for the overall 2-tone envelope at the output pin), the Typical Characteristics show a 58dBc difference between the test-tone power and the 3rd-order intermodulation spurious levels. This exceptional performance improves further when operating at lower frequencies.

NOISE PERFORMANCE

The OPA3692 offers an excellent balance between voltage and current noise terms to achieve low output noise. The inverting current noise (15pA/$\sqrt{Hz}$) is significantly lower than earlier solutions while the input voltage noise (1.7nV/$\sqrt{Hz}$) is lower than most unity-gain stable, wideband, voltage-feedback op amps. This low input voltage noise was achieved at the price of higher noninverting input current noise (12pA/$\sqrt{Hz}$). As long as the AC source impedance looking out of the noninverting node is less than 100Ω, this current noise will not contribute significantly to the total output noise. The op amp input voltage noise and the two input current noise terms combine to give low output noise under a wide variety of operating conditions. Figure 7 shows the op amp noise analysis model with all the noise terms included. In this model, all noise terms are taken to be noise voltage or current density terms in either nV/$\sqrt{Hz}$ or pA/$\sqrt{Hz}$.

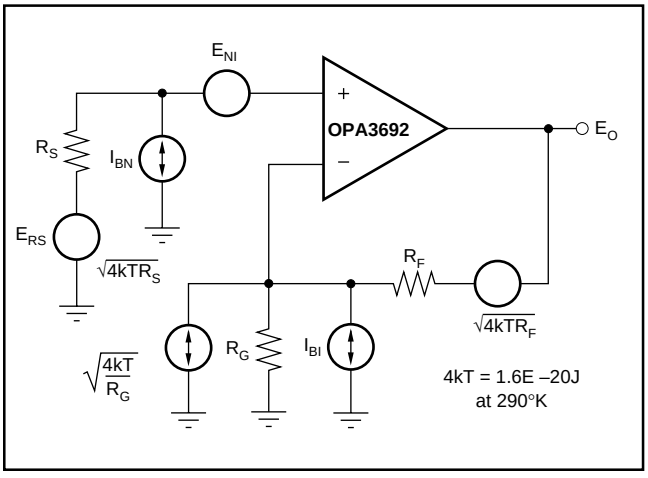


FIGURE 7. Noise Model.

The total output spot noise voltage can be computed as the square root of the sum of all squared output noise voltage contributors. Equation 1 shows the general form for the output noise voltage using the terms shown in Figure 7.

(1)

$$E_O = \sqrt{\left(E_{NI}^2 + \left(I_{BN}R_S\right)^2 + 4kTR_S\right)NG^2 + \left(I_{BI}R_F\right)^2 + 4kTR_FNG}$$

Dividing this expression by the noise gain (NG = (1+R_F/R_G)) gives the equivalent input-referred spot noise voltage at the noninverting input as shown in Equation 2.

(2)

$$E_N = \sqrt{E_{NI}^2 + \left(I_{BN}R_S\right)^2 + 4kTR_S + \left(\frac{I_{BI}R_F}{NG}\right)^2 + \frac{4kTR_F}{NG}}$$

Evaluating these two equations for the OPA3692 circuit and component values shown in Figure 1 gives a total output spot noise voltage of 8nV/$\sqrt{Hz}$ and a total equivalent input spot noise voltage of 4nV/$\sqrt{Hz}$. This total input-referred spot noise voltage is higher than the 1.7nV/$\sqrt{Hz}$ specification for the op amp voltage noise alone. This reflects the noise added to the output by the inverting current noise times the feedback resistor. This inverting node current noise is modeled as internal to the OPA3692 with R_F set internally as well.

DC ACCURACY

The OPA3692 provides exceptional bandwidth in high gains, giving fast pulse settling but only moderate DC accuracy. The Electrical Characteristics show an input offset voltage comparable to high-speed voltage-feedback amplifiers. However, the two input bias currents are somewhat higher and are unmatched. Bias current cancellation techniques do not reduce the output DC offset for OPA3692. As the two input bias currents are unrelated in both magnitude and polarity, matching the source impedance looking out of each input to reduce their error contribution to the output is ineffective. Evaluating the configuration of Figure 1, using worst-case +25°C input offset voltage and the two input bias currents, gives a worst-case output offset range equal to:

$$\pm(NG \bullet V_{OS(MAX)}) + (I_{BN} \bullet R_S/2 \bullet NG) \pm (I_{BI} \bullet R_F)$$

where NG = noninverting signal gain

$$= \pm(2 \bullet 3mV) + (35\mu A \bullet 25\Omega \bullet 2) \pm (402\Omega \bullet 25\mu A)$$

$$= \pm 6mV + 1.75mV \pm 10.05mV$$

$$= -14.3mV \rightarrow +17.8mV$$

Minimizing the resistance seen by the noninverting input will give the best DC offset performance.

DISABLE OPERATION

The OPA3692 provides an optional disable feature that can be used either to reduce system power or to implement a simple channel multiplexing operation. If the $\overline{DIS}$ control pin is left unconnected, the OPA3692 operates normally. To disable, the control pin must be asserted LOW. Figure 8 shows a simplified internal circuit for the disable control feature.

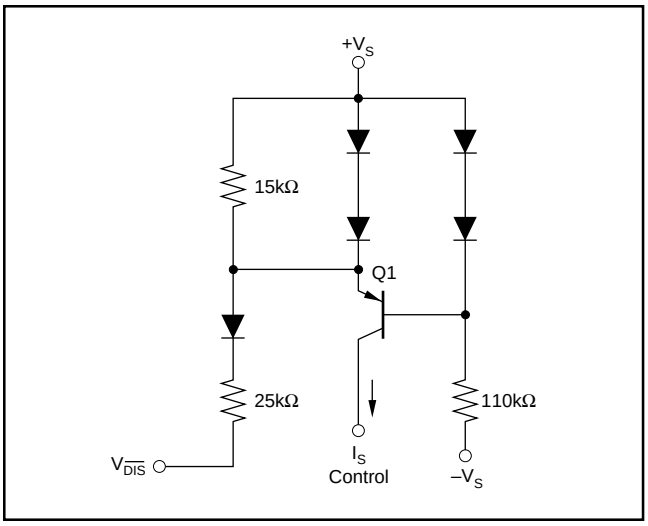


FIGURE 8. Simplified Disable Control Circuit.

In normal operation, base current to Q1 is provided through the 110kΩ resistor while the emitter current through the 15kΩ resistor sets up a voltage drop that is inadequate to turn on the two diodes in the Q1 emitter. As $V_{\overline{DIS}}$ is pulled LOW, additional current is pulled through the 15kΩ resistor, eventually turning on these two diodes (≈ 75μA). At this point, any additional current pulled out of $V_{\overline{DIS}}$ goes through those diodes holding the emitter-base voltage of Q1 at approximately 0V. This shuts off the collector current out of Q1, turning the amplifier off. The supply current in the disable mode is only what is required to operate the circuit of Figure 8. Additional circuitry ensures that turn-on time occurs faster than turn-off time (make-before-break).

When disabled, the output and input nodes go to a high-impedance state. If the OPA3692 is operating in a gain of +1, this shows a very high impedance (2pF || 1MΩ) at the output and exceptional signal isolation. If operating at a gain of +2, the total feedback network resistance ($R_F + R_G$) will appear as the impedance looking back into the output, but the circuit will still show very high forward and reverse isolation. If configured as an inverting amplifier, the input and output will be connected through the feedback network resistance ($R_F + R_G$) giving relatively poor input to output isolation.

One key parameter in disable operation is the output glitch when switching in and out of the disabled mode. Typical Characteristics show these glitches for the circuit of Figure 1 with the input signal set to 0V. The glitch waveform at the output pin is plotted along with the $\overline{DIS}$ pin voltage.

The transition edge rate (dV/dt) of the $\overline{DIS}$ control line influences this glitch. For the curve, *Disable/Enable Glitch*, shown in the Typical Characteristics, the edge rate was reduced until no further reduction in glitch amplitude was observed. This approximately 1V/ns maximum slew rate can be achieved by adding a simple RC filter into the $V_{\overline{DIS}}$ pin from a higher speed logic line. If extremely fast transition logic is used, a 2kΩ series resistor between the logic gate and the $\overline{DIS}$ input pin provides adequate bandlimiting using just the parasitic input capacitance on the $\overline{DIS}$ pin while still ensuring an adequate logic level swing.

THERMAL ANALYSIS

Due to the high output power capability of the OPA3692, heatsinking or forced airflow may be required under extreme operating conditions. Maximum desired junction temperature will set the maximum allowed internal power dissipation as described following. In no case should the maximum junction temperature be allowed to exceed 175°C.

Operating junction temperature (T_J) is given by $T_A + P_D \bullet \theta_{JA}$. The total internal power dissipation (P_D) is the sum of quiescent power (P_{DQ}) and additional power dissipated in the output stage (P_{DL}) to deliver load power. Quiescent power is simply the specified no-load supply current times the total supply voltage across the part. P_{DL} depends on the required output signal and load but, for a grounded resistive load, be at a maximum when the output is fixed at a voltage equal to 1/2 of either supply voltage (for equal bipolar supplies). Under this condition $P_{DL} = V_S^2/(4 \bullet R_L)$, where R_L includes feedback network loading.

Note that it is the power in the output stage and not in the load that determines internal power dissipation.

As a worst-case example, compute the maximum T_J using an OPA3692 in the circuit of Figure 1 operating at the maximum specified ambient temperature of +85°C with all three outputs driving a grounded 100Ω load to +2.5V:

$P_D = 10V \bullet 17.4mA + 3\ (5^2/(4 \bullet (100\Omega \parallel 804\Omega)) = 384mW$

Maximum $T_J = +85°C + (0.384W \bullet 100°C/W) = 123.4°C$

This worst-case condition is within the maximum junction temperature. Normally, this extreme case is not encountered. Careful attention to internal power dissipation is required.

BOARD LAYOUT GUIDELINES

Achieving optimum performance with a high frequency amplifier like the OPA3692 requires careful attention to board layout parasitics and external component types. Recommendations that will optimize performance include:

a) Minimize parasitic capacitance to any AC ground for all of the signal I/O pins. Parasitic capacitance on the output pin can cause instability: on the noninverting input, it can react with the source impedance to cause unintentional bandlimiting. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes around those pins. Otherwise, ground and power planes should be unbroken elsewhere on the board.

b) Minimize the distance (< 0.25") from the power-supply pins to high frequency 0.1μF decoupling capacitors. At the device pins, the ground and power plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power-supply connections (on pins 9, 11, 13, and 15) should always be decoupled with these capacitors. An optional supply decoupling capacitor across the two power supplies (for bipolar operation) will improve 2nd-harmonic distortion performance. Larger (2.2μF to 6.8μF) decoupling capacitors, effective at lower frequency, should also be used on the main supply pins. These may be placed somewhat farther from the device and may be shared among several devices in the same area of the PCB.

c) Careful selection and placement of external components will preserve the high-frequency performance of the OPA3692. Resistors should be a very low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Metal-film and carbon composition, axially-leaded resistors can also provide good high-frequency performance. Again, keep their leads and PCB trace length as short as possible. Never use wirewound type resistors in a high-frequency application. Other network components, such as noninverting input termination resistors, should also be placed close to the package.

d) Connections to other wideband devices on the board may be made with short direct traces or through onboard transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50mils to 100mils) should be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and set R_S from the plot of recommended R_S versus Capacitive Load. Low parasitic capacitive loads (< 5pF) may not need an R_S because the OPA3692 is nominally compensated to operate with a 2pF parasitic load. If a long trace is required, and the 6dB signal loss intrinsic to a doubly-terminated transmission line is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50Ω environment is normally not necessary on board, and in fact, a higher impedance environment will improve distortion as shown in the Distortion versus Load plots. With a characteristic board trace impedance defined based on board material and trace dimensions, a matching series resistor into the trace from the output of the OPA3692 is used as well as a terminating shunt resistor at the input of the destination device. Remember also that the terminating impedance will be the parallel combination of the shunt resistor and the input impedance of the destination device; this total effective impedance should be set to match the trace impedance. The high output voltage and current capability of the OPA3692 allows multiple destination devices to be handled as separate transmission lines, each with their own series and shunt terminations. If the 6dB attenuation of a doubly-terminated transmission line is unacceptable, a long trace can be series-terminated at the source end only. Treat the trace as a capacitive load in this case and set the series resistor value as shown in the plot of R_S versus Capacitive Load. This will not preserve signal integrity as well as a doubly-terminated line. If the input impedance of the destination device is low, there will be some signal attenuation due to the voltage divider formed by the series output into the terminating impedance.

e) Socketing a high-speed part like the OPA3692 is not recommended. The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network which can make it almost impossible to achieve a smooth, stable frequency response. Best results are obtained by soldering the OPA3692 onto the board.

INPUT AND ESD PROTECTION

The OPA3692 is built using a very high-speed complementary bipolar process. The internal junction breakdown voltages are relatively low for these very small geometry devices. These breakdowns are reflected in the Absolute Maximum Ratings table. All device pins have limited ESD protection using internal diodes to the power supplies as shown in Figure 9.

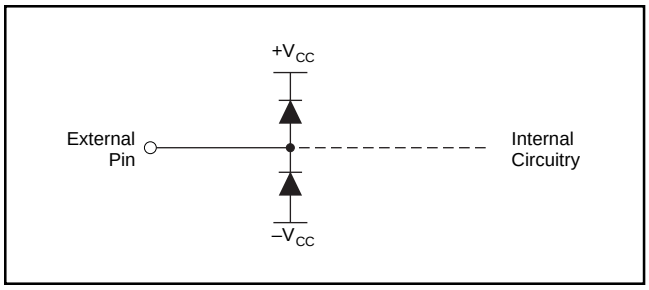


FIGURE 9. Internal ESD Protection.

These diodes provide moderate protection to input overdrive voltages above the supplies as well. The protection diodes can typically support 30mA continuous current. Where higher currents are possible (for example, in systems with ±15V supply parts driving into the OPA3692), current-limiting series resistors should be added into the two inputs. Keep these resistor values as low as possible since high values degrade both noise performance and frequency response.

Revision History

DATE	REVISION	PAGE	SECTION	DESCRIPTION
12/08	E	2	Absolute Maximum Ratings	Changed minimum Storage Temperature Range from –40°C to –65°C.
6/06	D	13	Design-In Tools	Demonstration fixture numbers changed.
		18	Applications Information	Added Revision History table.

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA3692ID	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA3692	Samples
OPA3692IDBQR	ACTIVE	SSOP	DBQ	16	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 3692	Samples
OPA3692IDBQT	ACTIVE	SSOP	DBQ	16	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 3692	Samples
OPA3692IDG4	ACTIVE	SOIC	D	16	40	TBD	Call TI	Call TI	-40 to 85		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
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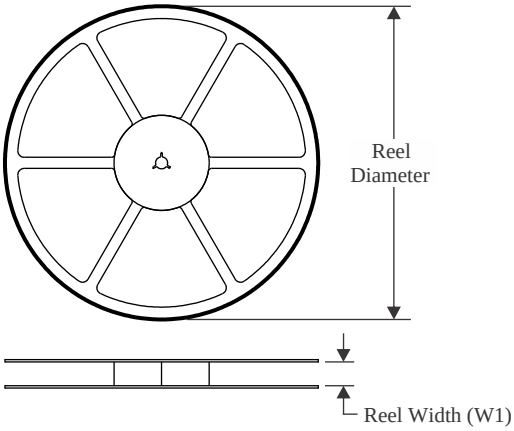
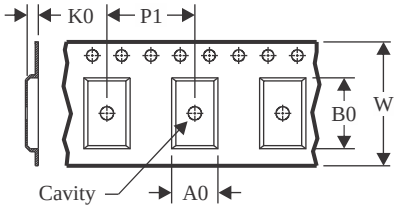
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

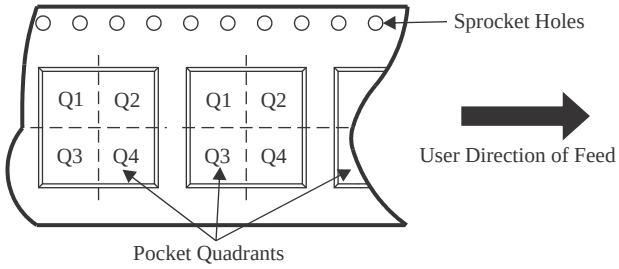


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

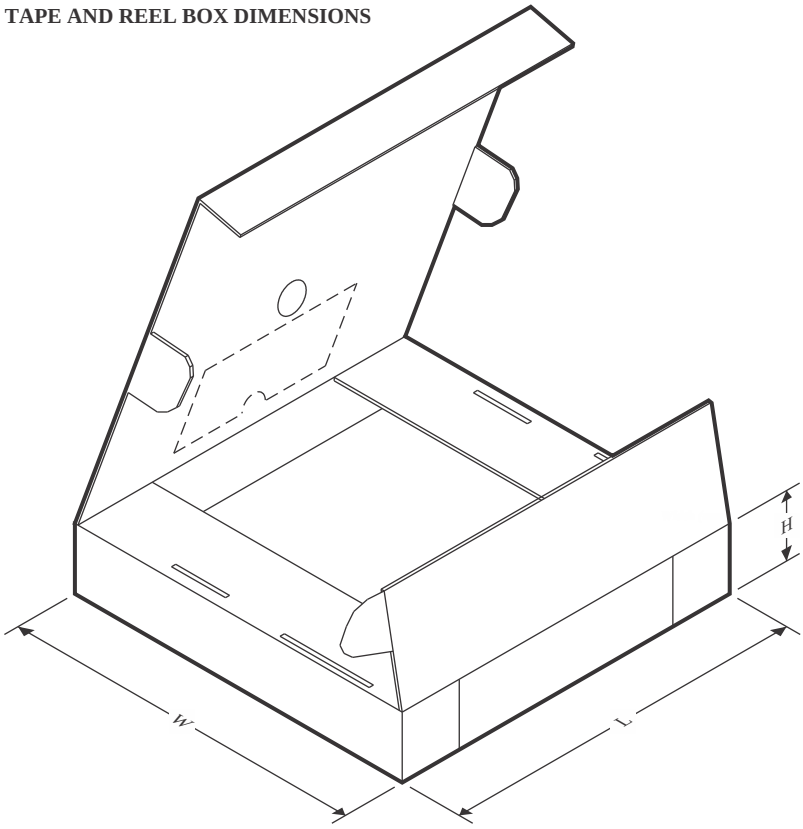
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA3692IDBQR	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA3692IDBQT	SSOP	DBQ	16	250	180.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

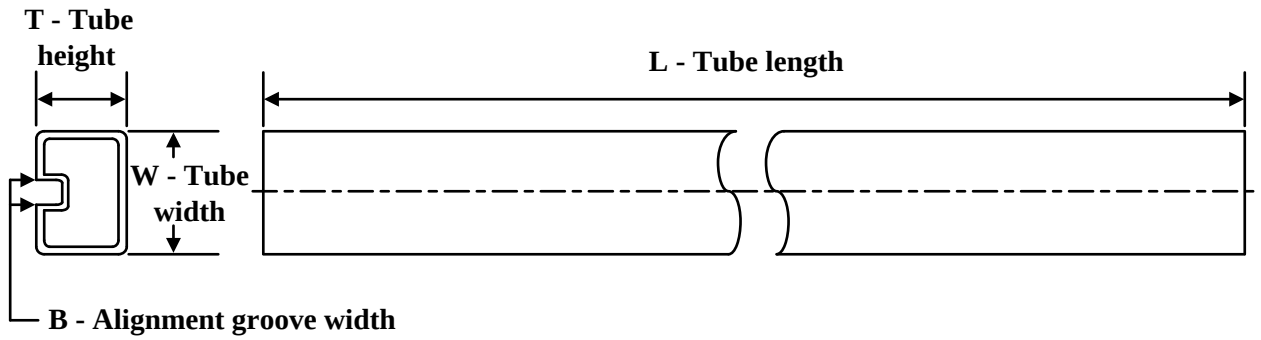
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA3692IDBQR	SSOP	DBQ	16	2500	356.0	356.0	35.0
OPA3692IDBQT	SSOP	DBQ	16	250	210.0	185.0	35.0

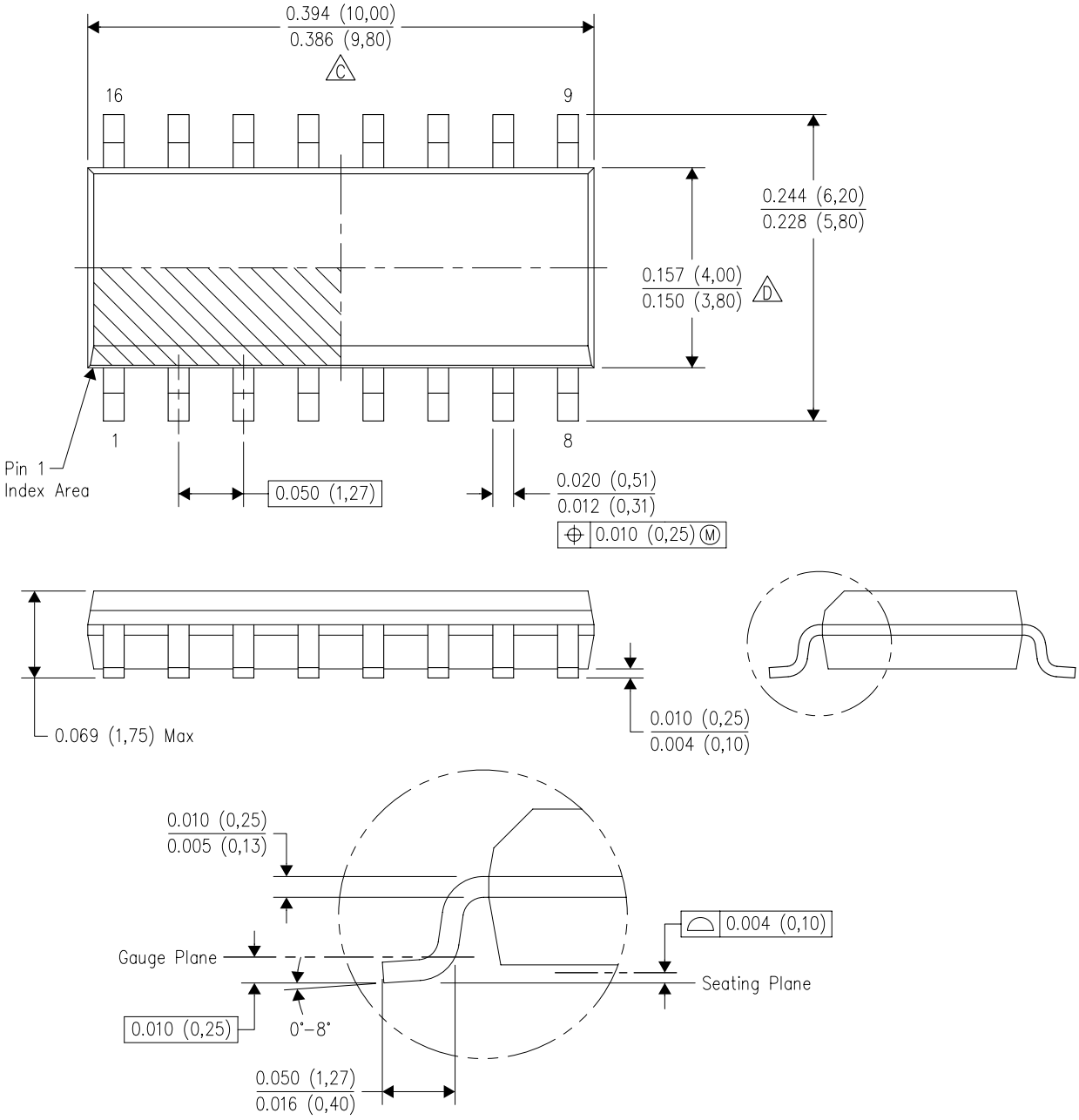
TUBE



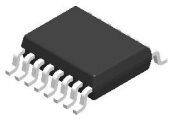
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA3692ID	D	SOIC	16	40	506.6	8	3940	4.32

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

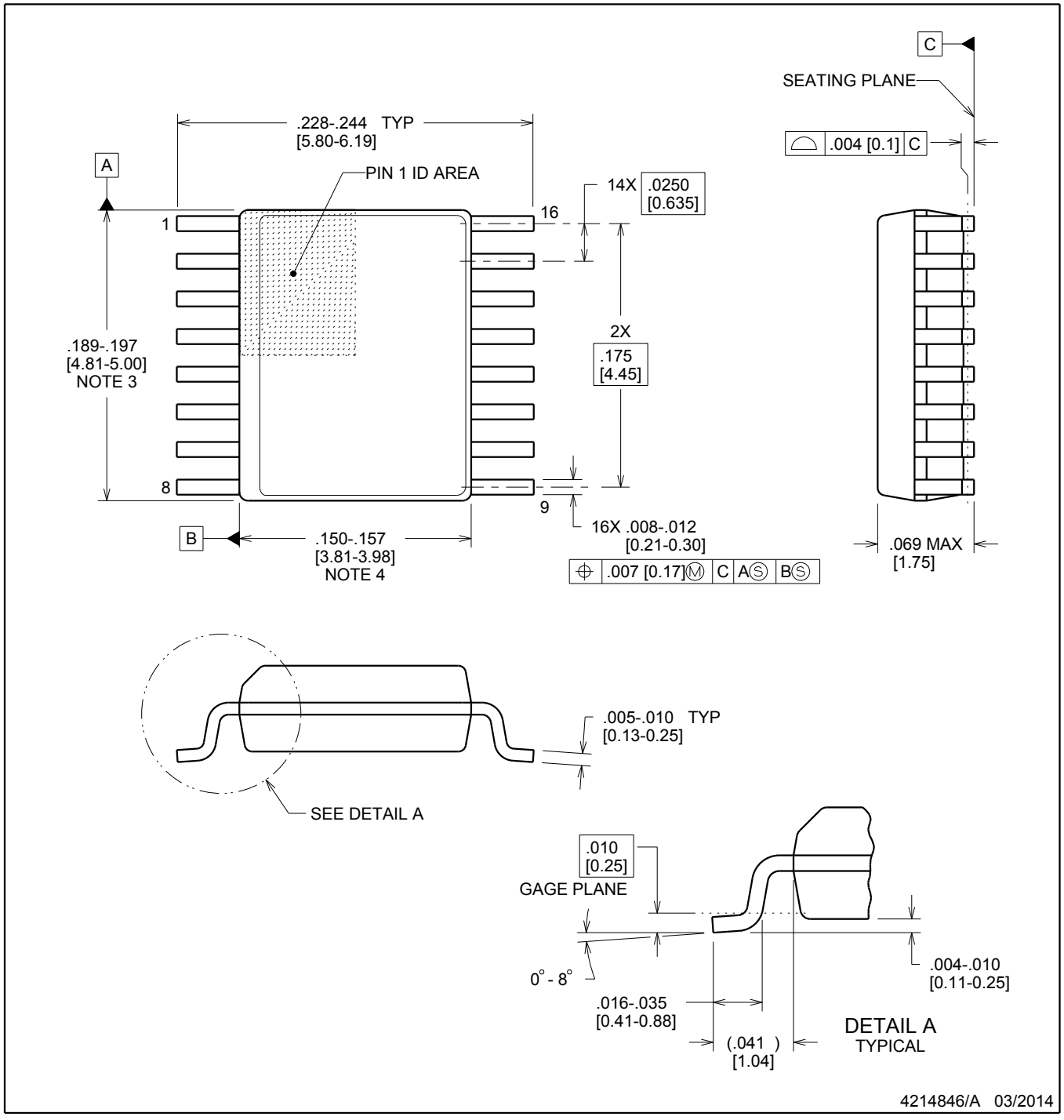


PACKAGE OUTLINE

DBQ0016A

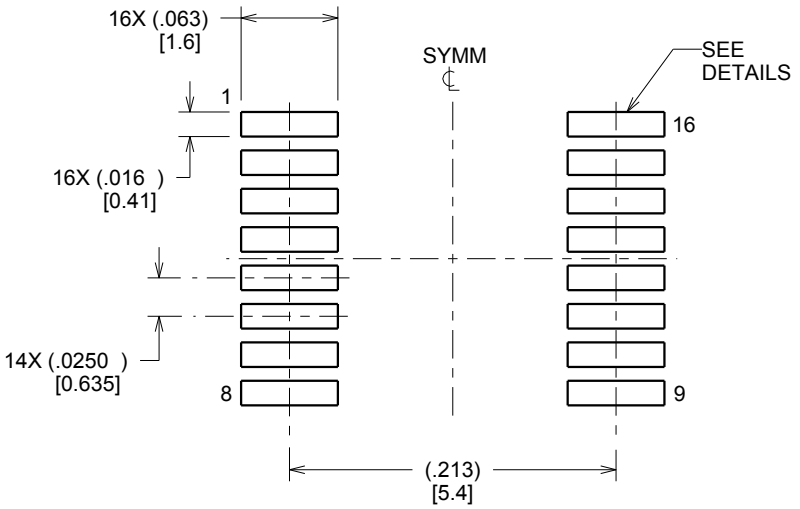
SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE

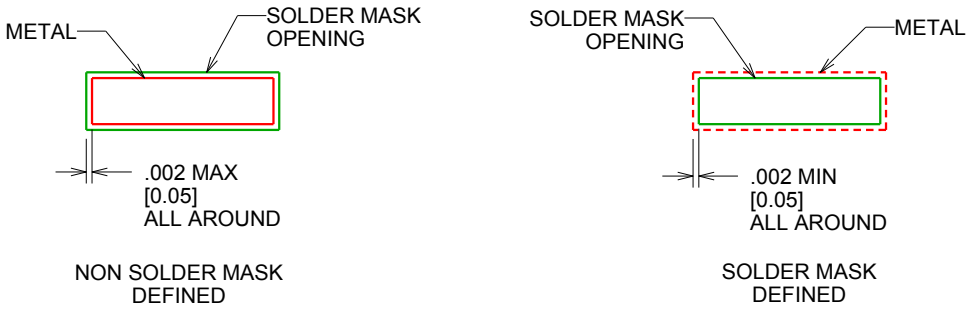


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 inch, per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MO-137, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4214846/A 03/2014

NOTES: (continued)

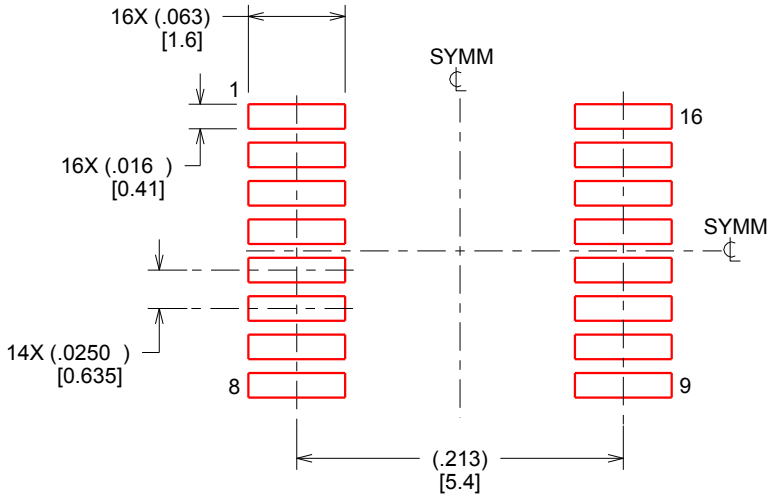
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.127 MM] THICK STENCIL
SCALE:8X

4214846/A 03/2014

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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