# SN74AHC367 Hex Buffers and Line Drivers With 3-State Outputs

## 1 Features

- Operating range 2V to 5.5V $V_{CC}$
- Latch-up performance exceeds 100 mA per JESD 78, class II

## 2 Applications

- Enable or disable a digital signal
- Controlling an indicator LED
- Translation between communication modules and system controllers

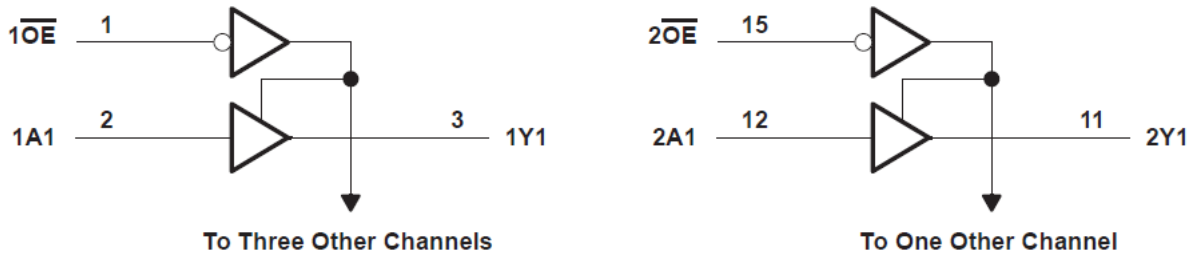
## 3 Description

The 'AHC367 devices are hex buffers and line drivers designed for 2V to 5.5V $V_{CC}$ operation.

**Package Information**

| PART NUMBER | PACKAGE(1) | PACKAGE SIZE(2) | BODY SIZE (3) |
|---|---|---|---|
| SN74AHC367 | D (SOIC, 16) | 9.9mm × 6mm | 9.9mm × 3.9mm |
| | N (PDIP, 16) | 19.3mm x 9.4mm | 19.3mm x 6.35mm |
| | PW (TSSOP, 16) | 5.00mm x 6.4mm | 5.00mm x 4.4mm |

(1) For more information, see Mechanical, Packaging, and Orderable Information.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) The body size (length × width) is a nominal value and does not include pins.




**Logic Diagram (Positive Logic)**

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## 4 Pin Configurations and Functions

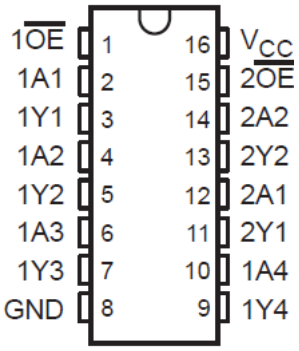



**Figure 4-1. D, DB, DGV, N, or PW Package (Top View)**

**Table 4-1. Pin Functions**

| PIN | | TYPE | DESCRIPTION |
|---|---|---|---|
| NO. | NAME | | |
| 1 | 1 $\overline{OE}$ | I | Output Enable 1 |
| 2 | 1A1 | I | 1A1 Input |
| 3 | 1Y1 | O | 1Y1 Output |
| 4 | 1A2 | I | 1A2 Input |
| 5 | 1Y2 | O | 1Y2 Output |
| 6 | 1A3 | I | 1A3 Input |
| 7 | 1Y3 | O | 1Y3 Output |
| 8 | GND | — | Ground Pin |
| 9 | 1Y4 | O | 1Y4 Output |
| 10 | 1A4 | I | 1A4 Input |
| 11 | 2Y1 | O | 2Y1 Output |
| 12 | 2A1 | I | 2A1 Input |
| 13 | 2Y2 | O | 2Y2 Output |
| 14 | 2A2 | I | 2A2 Input |
| 15 | 2 $\overline{OE}$ | I | Output Enable 2 |
| 16 | $V_{CC}$ | — | Power Pin |

# 5 Specifications

## 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage range | | –0.5 | 7 | V |
| $V_I$ (2) | Input voltage range | | –0.5 | 7 | V |
| $V_O$ (2) | Output voltage range | | –0.5 | $V_{CC}$ + 0.5 | V |
| $I_{IK}$ | Input clamp current | ($V_I$ < 0) | | –20 | mA |
| $I_{OK}$ | Output clamp current | ($V_O$ < 0) | | ±20 | mA |
| $I_O$ | Continuous output current | ($V_O$ = 0 to $V_{CC}$) | | ±25 | mA |
| | Continuous current through $V_{CC}$ or GND | | | ±75 | mA |
| $T_{stg}$ | Storage temperature range | | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

## 5.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-Body Model (A114-A), per ANSI/ESDA/JEDEC JS-001(1) | ±2000 | V |
| | | Charged-Device Model (C101), per JESD22-C101(2) | ±1000 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 2 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 2 V | 1.5 | | V |
| | | $V_{CC}$ = 3 V | 2.1 | | |
| | | $V_{CC}$ = 5.5 V | 3.85 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 2 V | | 0.5 | V |
| | | $V_{CC}$ = 3 V | | 0.9 | |
| | | $V_{CC}$ = 5.5 V | | 1.65 | |
| $V_I$ | Input voltage | | 0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 2 V | | –50 | μA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | –4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | –8 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 2 V | | 50 | μA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | 4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 8 | |
| Δt/Δv | Input transition rise or fall rate | $V_{CC}$ = 3.3 V ± 0.3 V | | 100 | ns/V |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 20 | |
| $T_A$ | Operating free-air temperature | | –40 | 85 | °C |

(1) All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*.

## 5.4 Thermal Information

| THERMAL METRIC[1] | | SN74AHC367 | | | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | D (SOIC) | DB (SSOP) | DGV (TVSOP) | N (PDIP) | PW (TSSOP) | |
| | | 16 PINS | 16 PINS | 16 PINS | 16 PINS | 16 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 73 | 82 | 120 | 67 | 135.9 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

## 5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | $V_{CC}$ | $T_A$ = 25°C | | | SN74AHC367 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | |
| $V_{OH}$ | $I_{OH}$ = –50 µA | | 2 V | 1.9 | 2 | | 1.9 | | V |
| | | | 3 V | 2.9 | 3 | | 2.9 | | |
| | | | 4.5 V | 4.4 | 4.5 | | 4.4 | | |
| | $I_{OH}$ = –4 mA | | 3 V | 2.58 | | | 2.48 | | |
| | $I_{OH}$ = –8 mA | | 4.5 V | 3.94 | | | 3.8 | | |
| $V_{OL}$ | $I_{OL}$ = 50 µA | | 2 V | | | 0.1 | | 0.1 | V |
| | | | 3 V | | | 0.1 | | 0.1 | |
| | | | 4.5 V | | | 0.1 | | 0.1 | |
| | $I_{OL}$ = 4 mA | | 3 V | | | 0.36 | | 0.44 | |
| | $I_{OL}$ = 8 mA | | 4.5 V | | | 0.36 | | 0.44 | |
| $I_I$ | $V_I$= 5.5 V or GND | | 0 V to 5.5 V | | | ± 0.1 | | ± 1 | µA |
| $I_{OZ}$ | $V_I$ = $V_{CC}$ or GND, $V_O$ = $V_{CC}$ or GND, $\overline{OE}$ = $V_{IH}$ | | 5.5 V | | | ± 0.25 | | ± 2.5 | µA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or GND, | $I_O$ = 0 | 5.5 V | | | 4 | | 40 | µA |
| $C_i$ | $V_I$ = $V_{CC}$ or GND | | 5 V | | 3 | 10 | | 10 | pF |
| $C_O$ | $V_O$ = $V_{CC}$ or GND | | 5 V | | 5.1 | | | | pF |

## 5.6 Switching Characteristics, $V_{CC}$ = 3.3 V ± 0.3 V

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | SN74AHC367 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | |
| $t_{PLH}$ | A | Y | $C_L$ = 15 pF | | 4.7[1] | 8.3[1] | 1 | 10 | ns |
| $t_{PHL}$ | | | | | 4.7[1] | 8.3[1] | 1 | 10 | |
| $t_{PZH}$ | $\overline{OE}$ | Y | $C_L$ = 15 pF | | 5.1[1] | 10.5[1] | 1 | 12.5 | ns |
| $t_{PZL}$ | | | | | 5.1[1] | 10.5[1] | 1 | 12.5 | |
| $t_{PHZ}$ | $\overline{OE}$ | Y | $C_L$ = 15 pF | | 4[1] | 10.5[1] | 1 | 12.5 | ns |
| $t_{PLZ}$ | | | | | 4.91 | 10.51 | 1 | 12.5 | |
| $t_{PLH}$ | A | Y | $C_L$ = 50 pF | | 6.1 | 11.8 | 1 | 13.5 | ns |
| $t_{PHL}$ | | | | | 6.2 | 11.8 | 1 | 13.5 | |
| $t_{PZH}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | 6.4 | 14 | 1 | 16 | ns |
| $t_{PZL}$ | | | | | 6.8 | 14 | 1 | 16 | |
| $t_{PHZ}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | 6.2 | 13.6 | 1 | 15.5 | ns |
| $t_{PLZ}$ | | | | | 7.3 | 13.6 | 1 | 15.5 | |

1. On products compliant to MIL-PRF-38535, this parameter is not production tested.

## 5.7 Switching Characteristics, $V_{CC}$ = 5 V ± 0.5 V

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | SN74AHC367 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | |
| $t_{PLH}$ | A | Y | $C_L$ = 15 pF | | 3.4[1] | 5.9[1] | 1 | 7 | ns |
| $t_{PHL}$ | | | | | 3.6[1] | 5.9[1] | 1 | 7 | |
| $t_{PZH}$ | $\overline{OE}$ | Y | $C_L$ = 15 pF | | 3.6[1] | 7.2[1] | 1 | 8.5 | ns |
| $t_{PZL}$ | | | | | 3.8[1] | 7.2[1] | 1 | 8.5 | |
| $t_{PHZ}$ | $\overline{OE}$ | Y | $C_L$ = 15 pF | | 2.61 | 7.21 | 0 | 8.5 | ns |
| $t_{PLZ}$ | | | | | 2.6[1] | 7.2[1] | 0 | 8.5 | |
| $t_{PLH}$ | A | Y | $C_L$ = 50 pF | | 4.3 | 7.9 | 1 | 9 | ns |
| $t_{PHL}$ | | | | | 4.5 | 7.9 | 1 | 9 | |
| $t_{PZH}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | 4.6 | 9.2 | 1 | 10.5 | ns |
| $t_{PZL}$ | | | | | 4.9 | 9.2 | 1 | 10.5 | |
| $t_{PHZ}$ | $\overline{OE}$ | Y | $C_L$ = 50 pF | | 3.4 | 9.2 | 0 | 10.5 | ns |
| $t_{PLZ}$ | | | | | 4.5 | 9.2 | 0 | 10.5 | |

1. On products compliant to MIL-PRF-38535, this parameter is not production tested.

## 5.8 Noise Characteristics

$V_{CC}$ = 3.3 V, $C_L$ = 50 pF, $T_A$ = 25°C

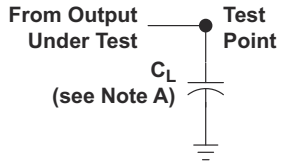
| PARAMETER | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | 0.9 | | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | | –0.8 | | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | | 4.2 | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 3.5 | | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | | 1.5 | V |

## 5.9 Operating Characteristics

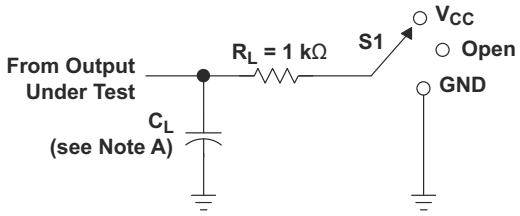
$T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, | f = 1 MHz | 22.4 | pF |

## 6 Parameter Measurement Information

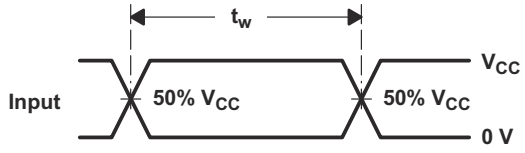



LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

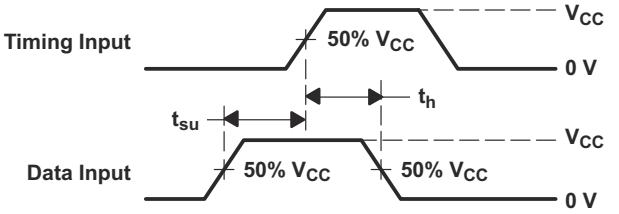



LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS

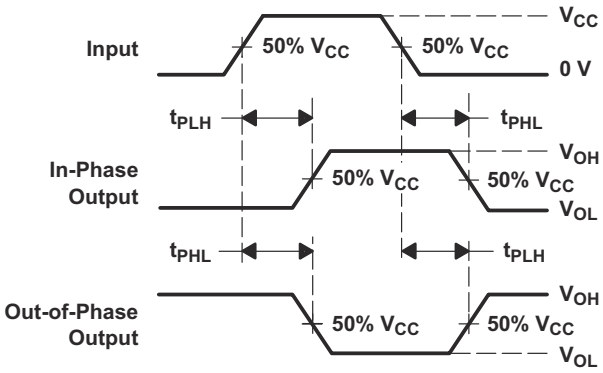
| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |
| Open Drain | $V_{CC}$ |



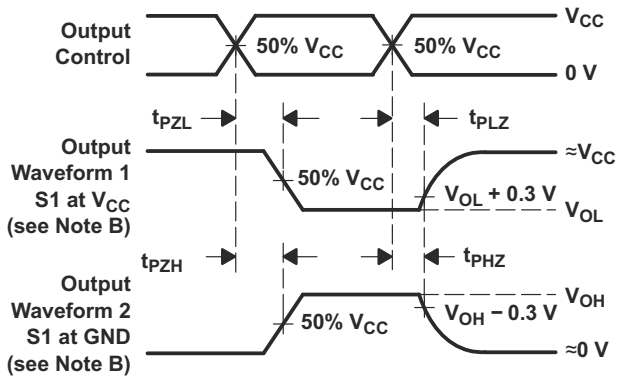

VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 3 ns, $t_f$ ≤ 3 ns.
D. The outputs are measured one at a time, with one input transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PHL}$ and $t_{PLH}$ are the same as $t_{pd}$.
H. All parameters and waveforms are not applicable to all devices.

**Figure 6-1. Load Circuit and Voltage Waveforms**

# 7 Detailed Description

## 7.1 Overview

These devices are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The ’AHC367 devices are organized as dual 4-line and 2-line buffers/drivers with active-low output-enable (1$\overline{OE}$ and 2$\overline{OE}$) inputs. When $\overline{OE}$ is low, the device passes noninverted data from the A inputs to the Y outputs. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to $V_{CC}$ through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

## 7.2 Functional Block Diagram

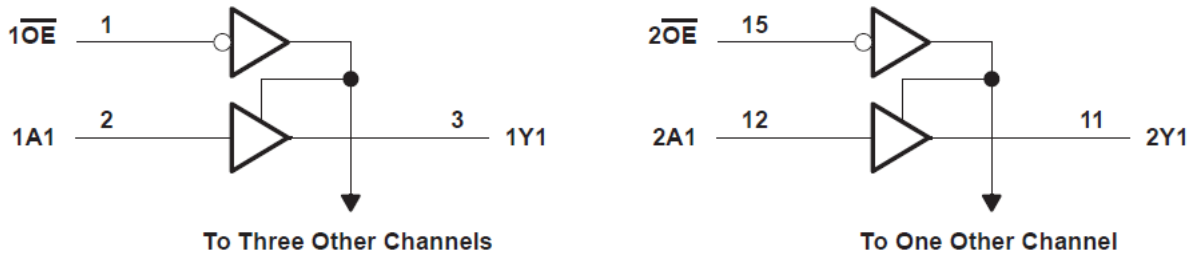



**Figure 7-1. Logic Diagram (Positive Logic)**

## 7.3 Device Functional Modes

**Table 7-1. Function Table (Each Buffer/ Driver)**

| INPUTS | | OUTPUT |
|---|---|---|
| $\overline{OE}$ | A | Y |
| L | H | H |
| L | L | L |
| H | X | Z |

# 8 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 8.1 Application Information

In this application, three 2-input AND gates are combined to produce a 4-input AND gate function as shown in Block Diagram. The fourth gate can be used for another application in the system, or the inputs can be grounded and the channel left unused.

The SN74AHC367 is used to directly control the $\overline{\text{RESET}}$ pin of a motor controller. The controller requires four input signals to all be HIGH before being enabled, and should be disabled in the event that any one signal goes LOW. The 4-input AND gate function combines the four individual reset signals into a single active-low reset signal.

## 8.2 Typical Application

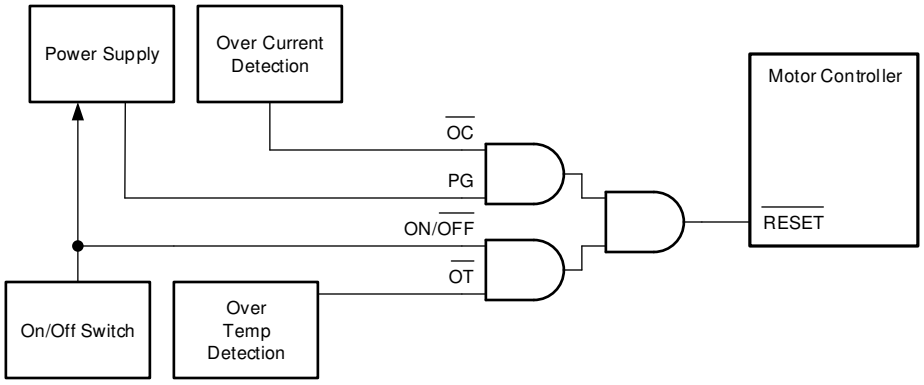



**Figure 8-1. Typical Application Block Diagram**

## 8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each $V_{CC}$ terminal should have a good bypass capacitor to prevent power disturbance. A 0.1-µF capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in the following layout example.

## 8.4 Layout

### *8.4.1 Layout Guidelines*

When using multiple-input and multiple-channel logic devices, inputs must never be left floating. In many cases, functions or parts of functions of digital logic devices are unused (for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used). Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or $V_{CC}$, whichever makes more sense for the logic function or is more convenient.

### 8.4.2 Layout Example

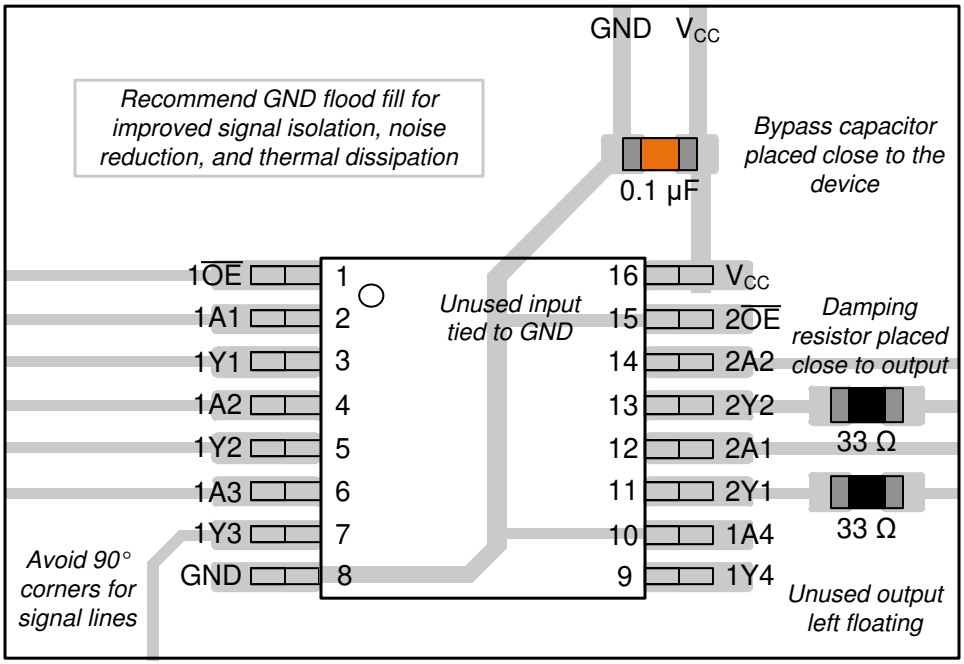



**Figure 8-2. Example Layout for the SN74AHC367**

# 9 Device and Documentation Support

## 9.1 Documentation Support (Analog)

### *9.1.1 Related Documentation*

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 9-1. Related Links**

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|---|---|---|---|---|---|
| SN74AHC367 | Click here | Click here | Click here | Click here | Click here |

## 9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

## 9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 9.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

# 10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision F (November 2023) to Revision G (July 2024) | Page |
|---|---|
| • Updated RθJA value: PW = 108 to 135.9, all values in °C/W | 5 |

| Changes from Revision E (February 2002) to Revision F (November 2023) | Page |
|---|---|
| • Added *Applications* section, *Package Information* table, *Pin Functions* table, *ESD Ratings* table, *Thermal Information* table, *Device Functional Modes, Application and Implementation* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section | 1 |

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74AHC367D | OBSOLETE | SOIC | D | 16 | | TBD | Call TI | Call TI | -40 to 85 | AHC367 | |
| SN74AHC367DR | ACTIVE | SOIC | D | 16 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | AHC367 | Samples |
| SN74AHC367N | ACTIVE | PDIP | N | 16 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | -40 to 85 | SN74AHC367N | Samples |
| SN74AHC367PWR | ACTIVE | TSSOP | PW | 16 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HA367 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

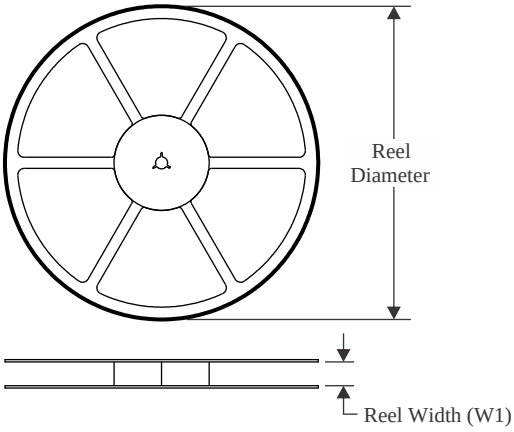
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

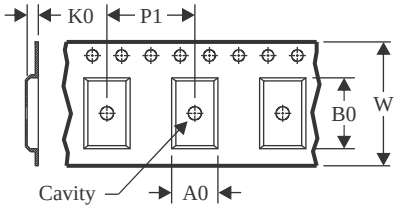
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

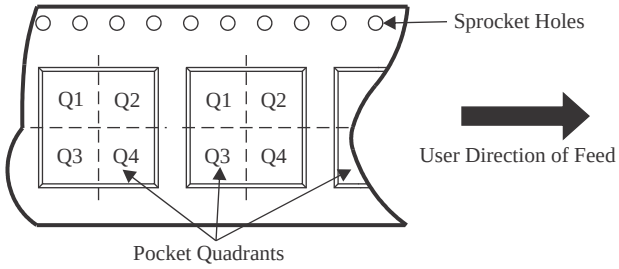



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

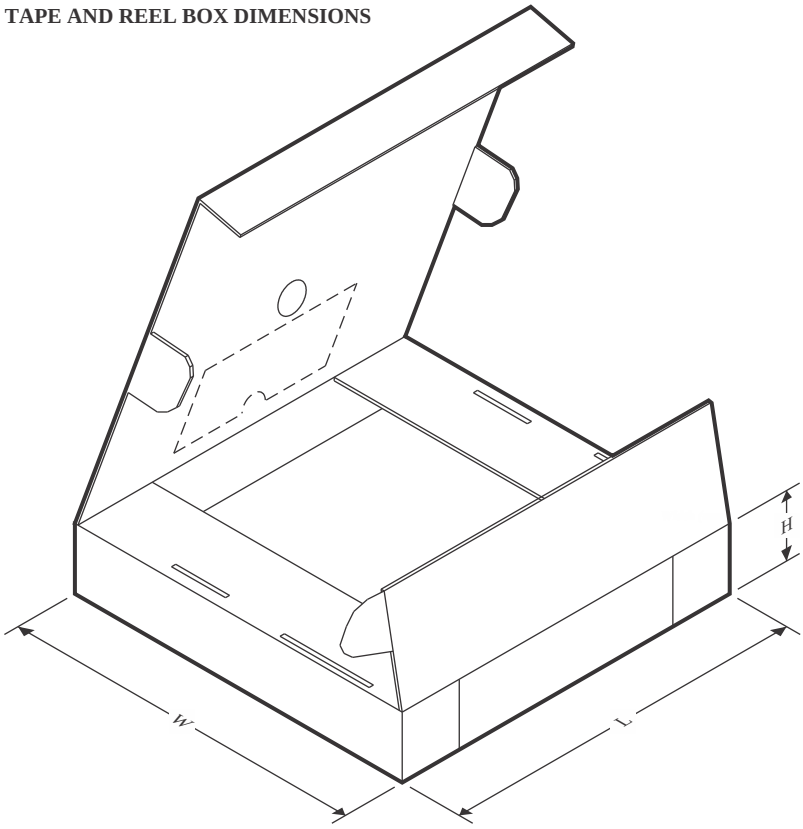
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74AHC367DR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74AHC367PWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74AHC367PWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

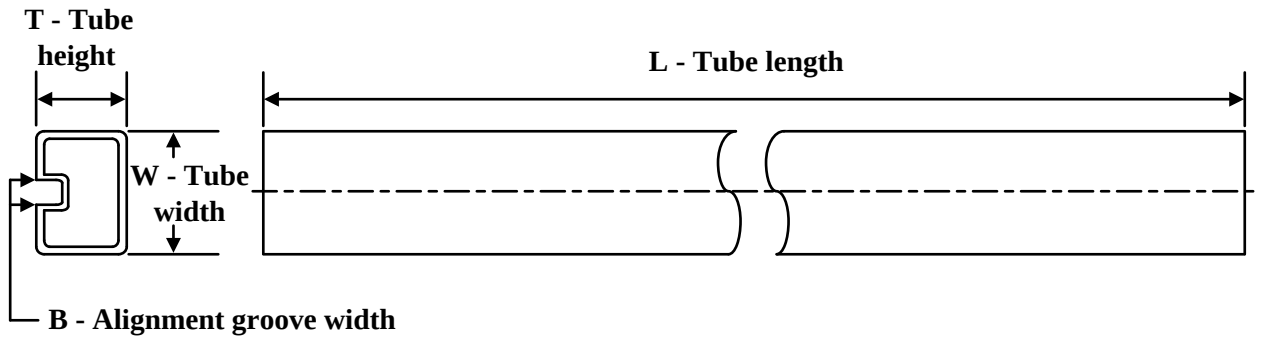
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74AHC367DR | SOIC | D | 16 | 2500 | 340.5 | 336.1 | 32.0 |
| SN74AHC367PWR | TSSOP | PW | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74AHC367PWR | TSSOP | PW | 16 | 2000 | 353.0 | 353.0 | 32.0 |

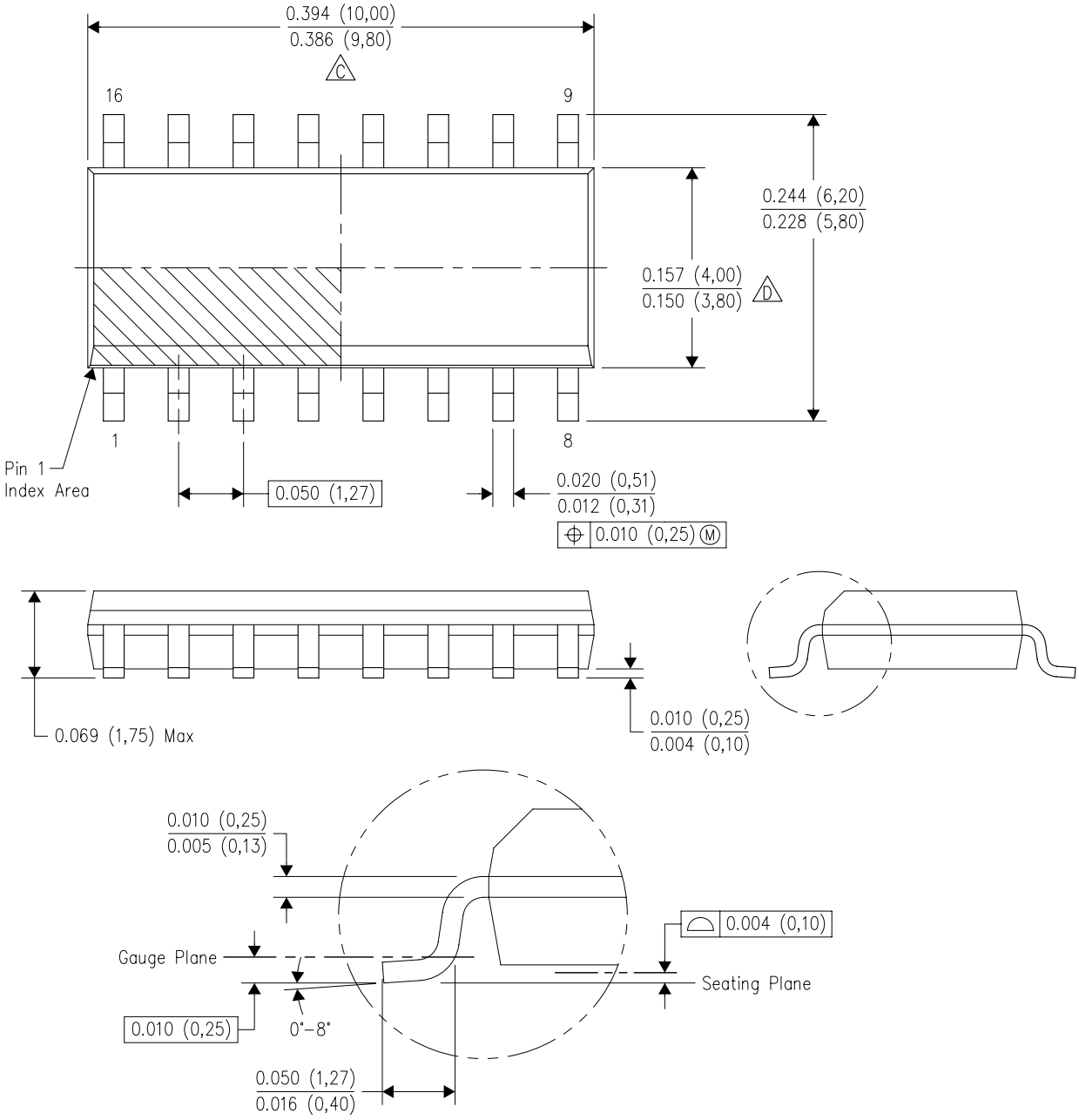
## TUBE




*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| SN74AHC367N | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74AHC367N | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



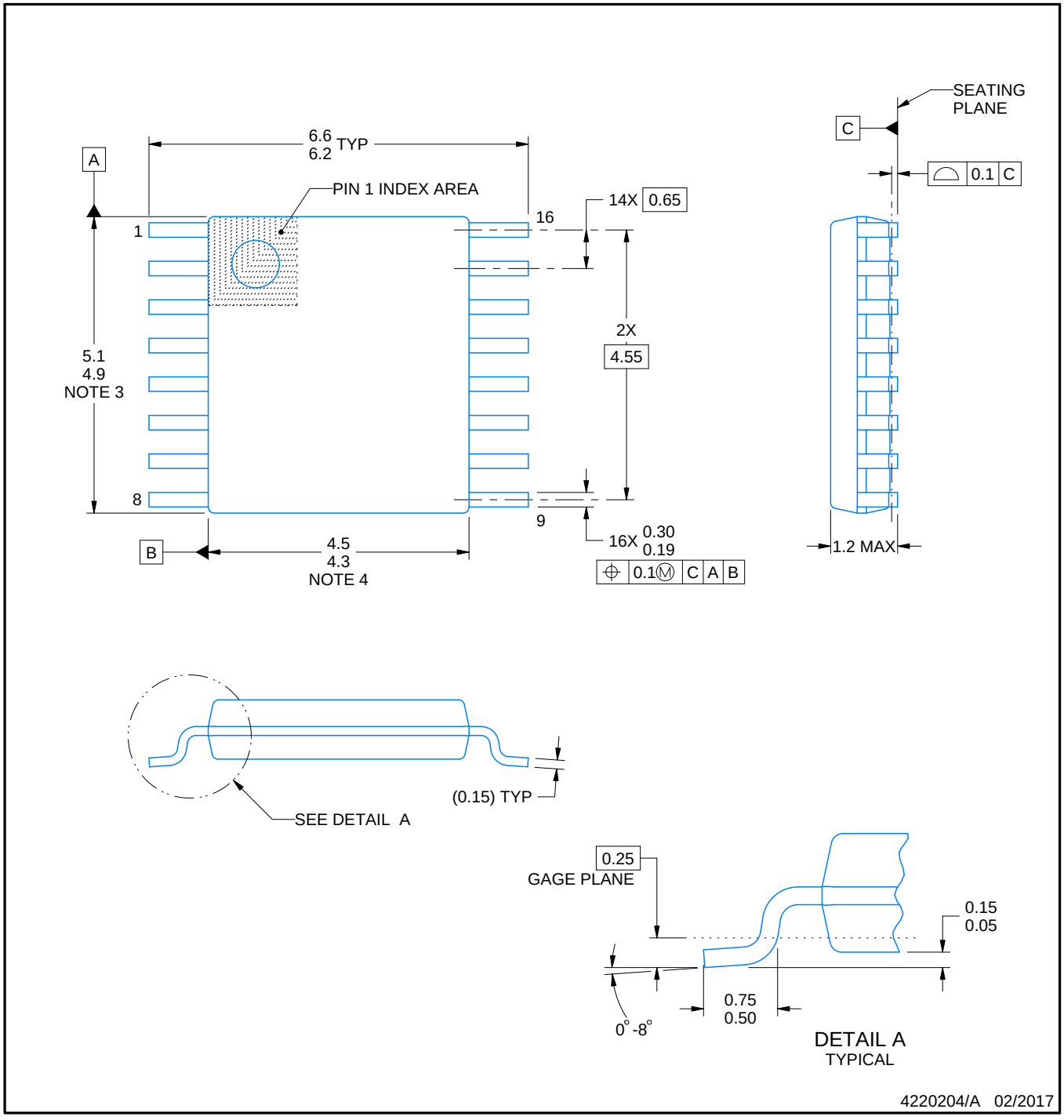

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

# PACKAGE OUTLINE

## PW0016A

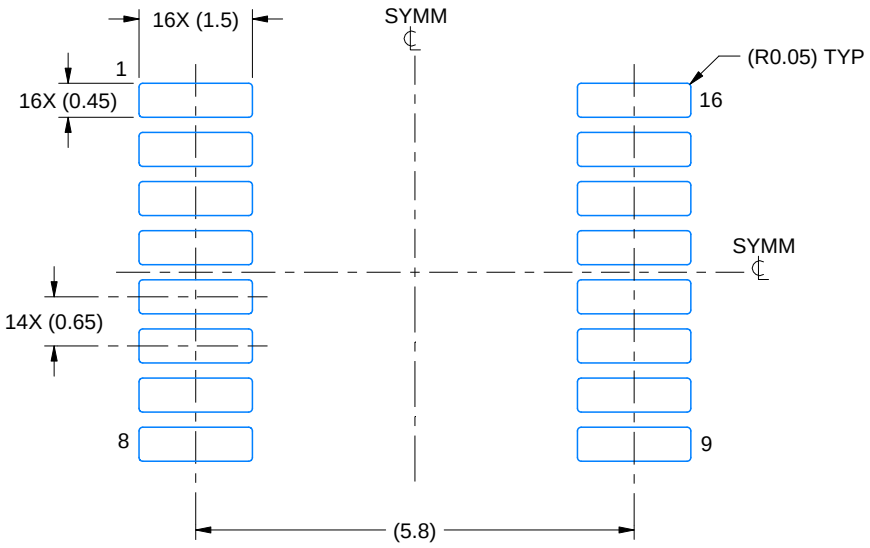
## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

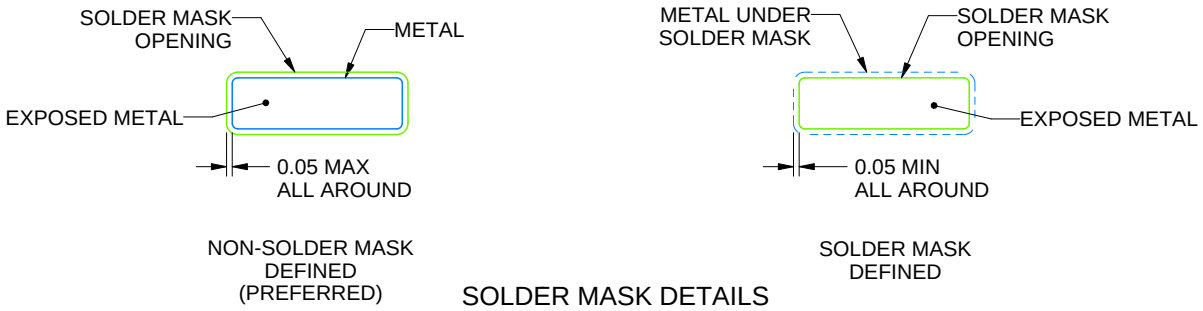



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

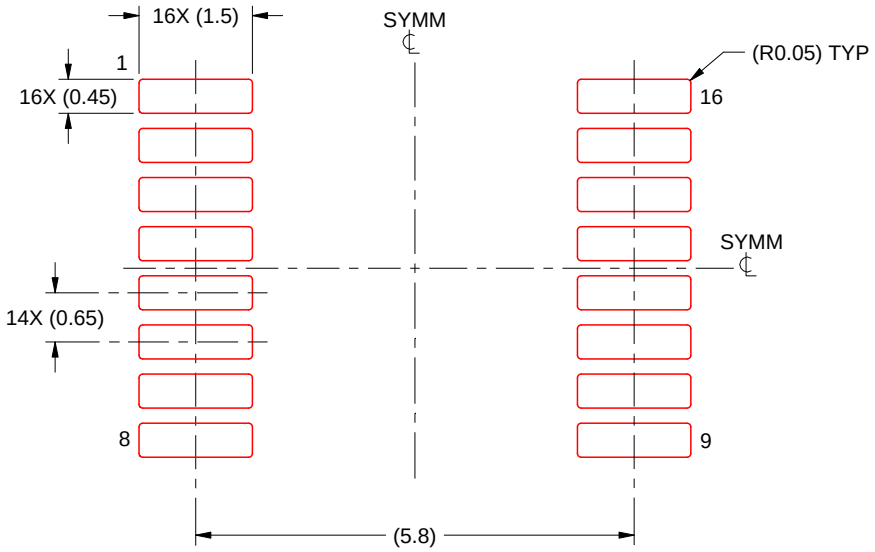



SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

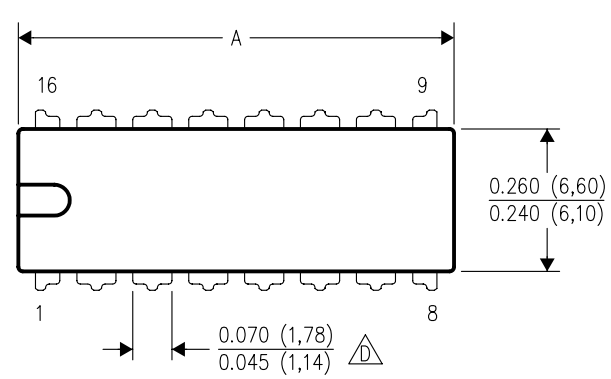
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

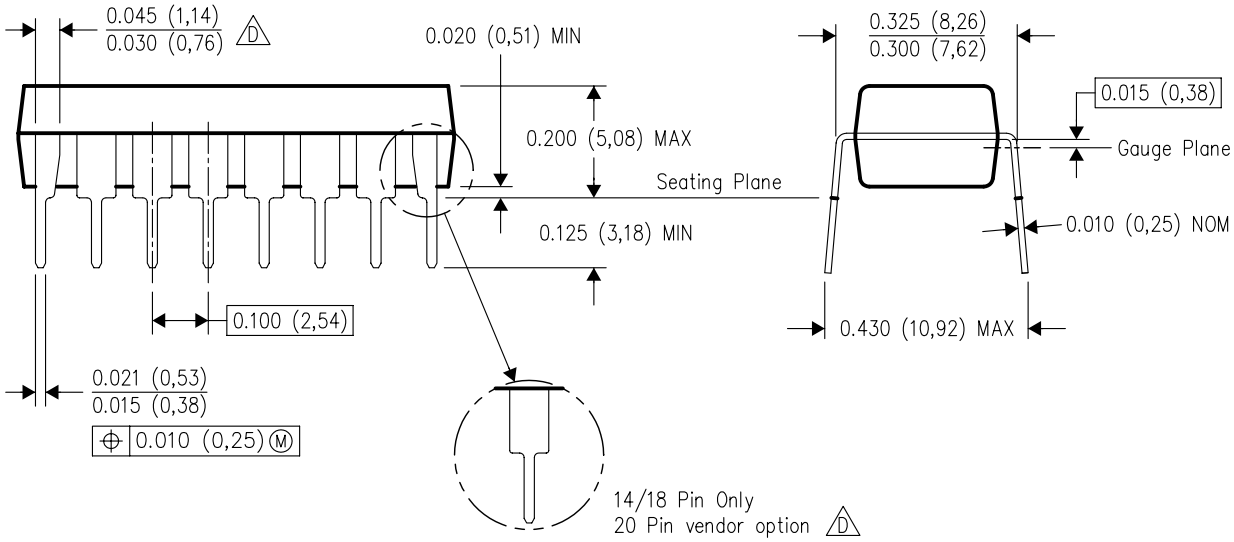
## N (R–PDIP–T**)

## PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |




4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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