

- Operates at 3-V to 3.6-V V_{CC}
- Load Clock and Unload Clock Can Be Asynchronous or Coincident
- Low-Power Advanced CMOS Technology
- Full, Empty, and Half-Full Flags
- Programmable Almost-Full/Almost-Empty Flag
- Fast Access Times of 18 ns With a 50-pF Load and All Data Outputs Switching Simultaneously
- Data Rates From 0 to 40 MHz
- 3-State Outputs
- Pin Compatible With SN74ACT7804
- Packaged in Shrink Small-Outline 300-mil Package (DL) Using 25-mil Center-to-Center Spacing

description

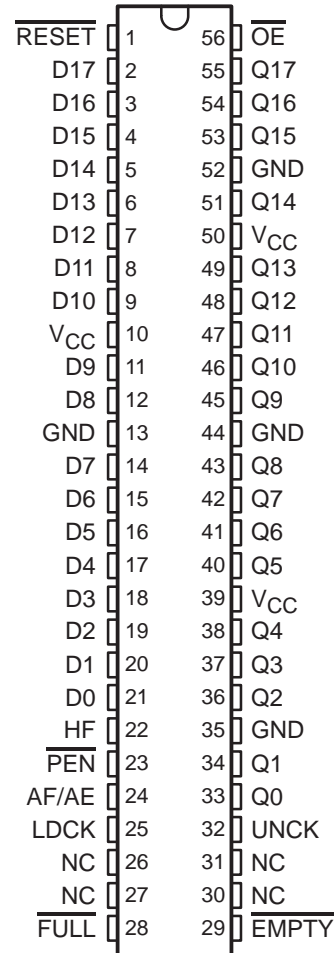
A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. The SN74ALVC7804 is an 18-bit FIFO with high speed and fast access times. Data is processed at rates up to 40 MHz with access times of 18 ns in a bit-parallel format. The SN74ALVC7804 is designed for 3-V to 3.6-V V_{CC} operation.

Data is written into memory on a low-to-high transition of the load clock (LDCK) and is read out on a low-to-high transition of the unload clock (UNCK). The memory is full when the number of words clocked in exceeds the number of words clocked out by 512. When the memory is full, LDCK has no effect on the data residing in memory. When the memory is empty, UNCK has no effect.

Status of the FIFO memory is monitored by the full (\overline{FULL}), empty (\overline{EMPTY}), half-full (HF), and almost-full/almost-empty (AF/AE) flags. The \overline{FULL} output is low when the memory is full and high when the memory is not full. The \overline{EMPTY} output is low when the memory is empty and high when it is not empty. The HF output is high whenever the FIFO contains 256 or more words and is low when it contains 255 or less words. The AF/AE status flag is a programmable flag. The first one or two low-to-high transitions of LDCK after reset are used to program the almost-empty offset value (X) and the almost-full offset value (Y), if program enable (\overline{PEN}) is low. The AF/AE flag is high when the FIFO contains X or less words or (512 minus Y) or more words. The AF/AE flag is low when the FIFO contains between (X plus 1) and (511 minus Y) words.

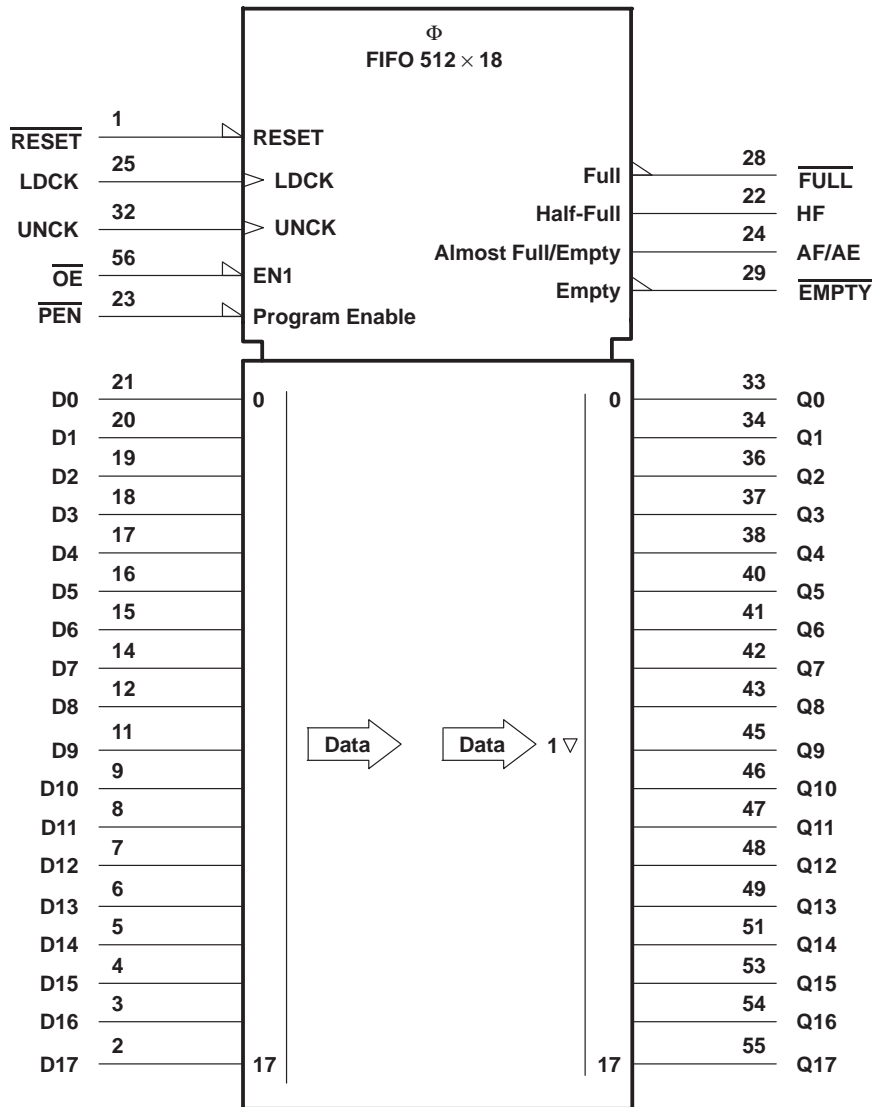
A low level on the reset (\overline{RESET}) resets the internal stack pointers and sets \overline{FULL} high, AF/AE high, HF low, and \overline{EMPTY} low. The Q outputs are not reset to any specific logic level. The FIFO must be reset upon power up. The first word loaded into empty memory causes \overline{EMPTY} to go high and the data to appear on the Q outputs. The data outputs are in the high-impedance state when the output-enable (\overline{OE}) is high.

DL PACKAGE
(TOP VIEW)



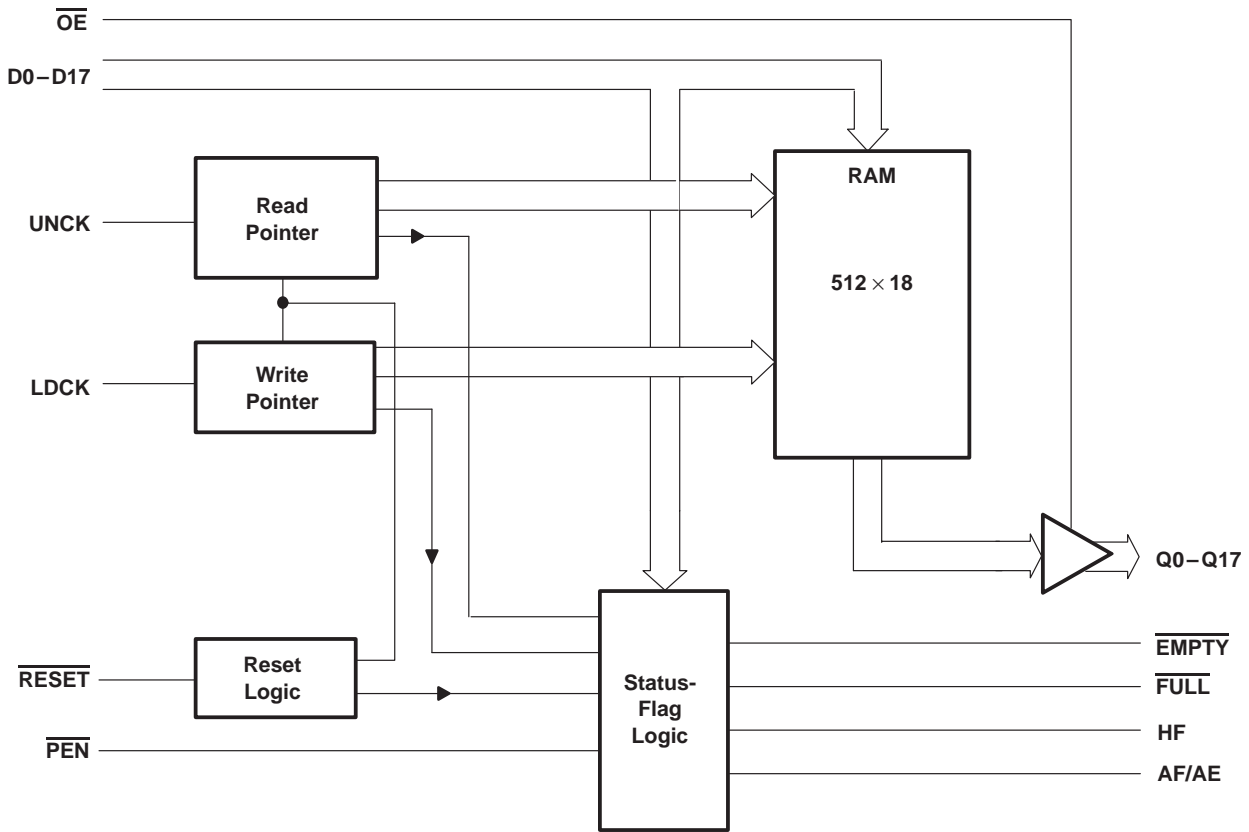
SN74ALVC7804
512 × 18
FIRST-IN, FIRST-OUT MEMORY
 SCAS432 – JANUARY 1995

logic symbol†



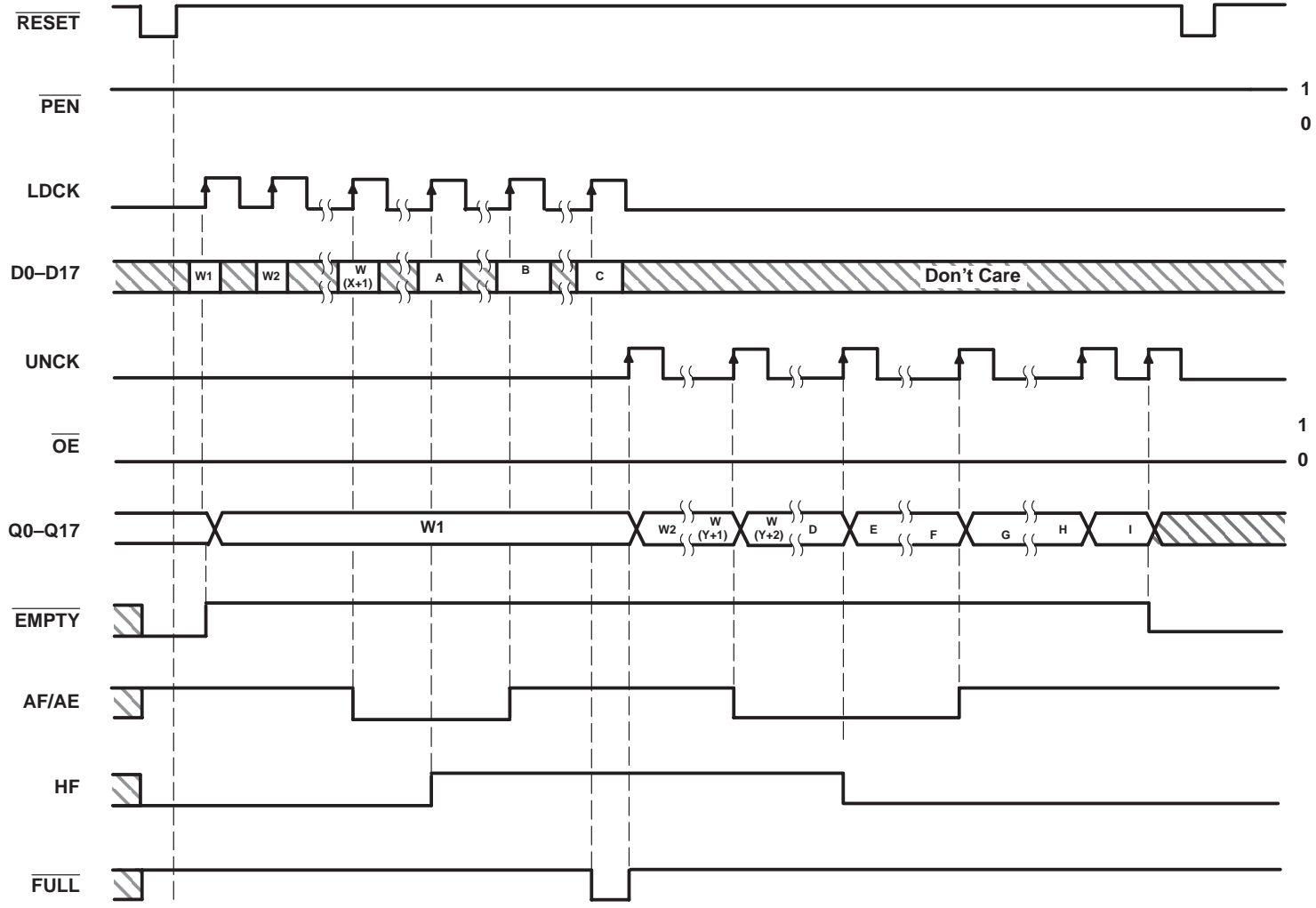
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AF/AE	24	O	Almost full/almost empty flag. Depth offset values can be programmed for AF/AE, or the default value of 64 can be used for both the almost empty offset (X) and the almost full offset (Y). AF/AE is high when memory contains X or less words or (512 - Y) or more words. AF/AE is high after reset.
D0-D17	21-14, 12-11, 9-2	I	18-bit data input port
$\overline{\text{EMPTY}}$	29	O	Empty flag. $\overline{\text{EMPTY}}$ is low when the FIFO is empty. A FIFO reset also causes $\overline{\text{EMPTY}}$ to go low.
$\overline{\text{FULL}}$	28	O	Full flag. $\overline{\text{FULL}}$ is low when the FIFO is full. A FIFO reset causes $\overline{\text{FULL}}$ to go high.
HF	22	O	Half-full flag. HF is high when the FIFO memory contains 256 or more words. HF is low after reset.
LDCK	25	I	Load clock. Data is written to the FIFO on the rising edge of LDCK when $\overline{\text{FULL}}$ is high.
$\overline{\text{OE}}$	56	I	Output enable. When $\overline{\text{OE}}$ is high, the data outputs are in the high-impedance state.
$\overline{\text{PEN}}$	23	I	Program enable. After reset and before the first word is written to the FIFO, the binary value on D0-D7 is latched as an AF/AE offset value when $\overline{\text{PEN}}$ is low and WRTCLK is high.
Q0-Q17	33-34, 36-38, 40-43, 45-49, 51, 53-55	O	18-bit data output port
$\overline{\text{RESET}}$	1	I	Reset. A low level on $\overline{\text{RESET}}$ resets the FIFO and drives AF/AE and $\overline{\text{FULL}}$ high and HF and $\overline{\text{EMPTY}}$ low.
UNCK	32	I	Unload clock. Data is read from the FIFO on the rising edge of UNCK when $\overline{\text{EMPTY}}$ is high.



Define the AF/AE Flag
 Using the Default Value of X and Y

Figure 1. Write, Read, and Flag Timing Reference

DATA WORD NUMBERS FOR FLAG TRANSITIONS

DEVICE	TRANSITION WORD								
	A	B	C	D	E	F	G	H	I
SN74ALVC7804	W256	W(512-Y)	W512	W257	W258	W(512-X)	W(513-X)	W511	W512

offset values for AF/AE

The AF/AE flag has two programmable limits: the almost-empty offset value (X) and the almost-full offset value (Y). They can be programmed after the FIFO is reset and before the first word is written to memory. The AF/AE flag is high when the FIFO contains X or less words or (512 minus Y) or more words.

To program the offset values, $\overline{\text{PEN}}$ can be brought low after reset. On the following low-to-high transition of LDCK, the binary value on D0–D7 is stored as the almost empty offset value (X) and the almost full offset value (Y). Holding $\overline{\text{PEN}}$ low for another low-to-high transition of LDCK reprograms Y to the binary value on D0–D7 at the time of the second LDCK low-to-high transition. Writes to the FIFO memory are disabled while the offsets are programmed. A maximum value of 255 can be programmed for either X or Y (see Figure 2). To use the default values of X = Y = 64, $\overline{\text{PEN}}$ must be held high.

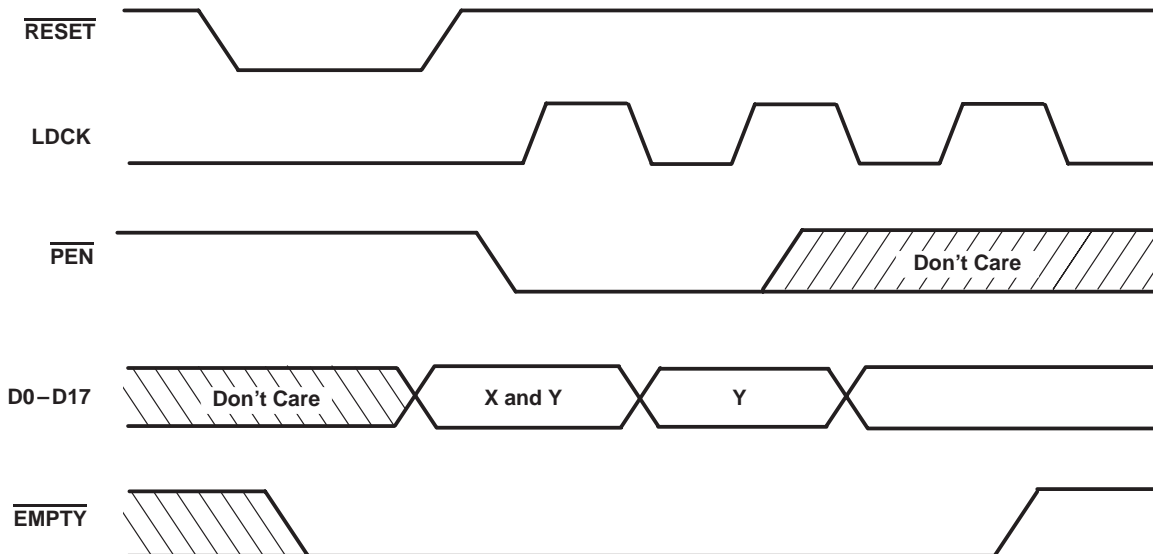


Figure 2. Programming X and Y Separately

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	–0.5 V to 4.6 V
Output voltage range, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Voltage applied to a disabled 3-state output	3.6 V
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings can be exceeded if the input and output clamp current ratings are observed.
2. This value is limited to 4.6 V maximum.

recommended operating conditions

		'ALVC7804-25 $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		'ALVC7804-40 $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		UNIT
		MIN	MAX	MIN	MAX	
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage	0.8		0.8		V
V_I		0	V_{CC}	0	V_{CC}	V
V_O		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current, Q outputs, Flags	$V_{CC} = 3 \text{ V}$		–8	–8	mA
I_{OL}	Low-level output current, Q outputs, Flags	$V_{CC} = 3 \text{ V}$		16	16	mA
f_{clock}	Clock frequency	40		25		MHz
t_w	Pulse duration	D0–D17 high or low		8	12	ns
		LDCK high or low		8	12	
		UNCK high or low		8	12	
		$\overline{\text{PEN}}$ low		8	12	
		RESET low		10	12	
t_{su}	Setup time	D0–D17 before LDCK↑		5	5	ns
		LDCK inactive before $\overline{\text{RESET}}$ high		6	6	
		$\overline{\text{PEN}}$ before LDCK↑		8	8	
t_h	Hold time	D0–D17 after LDCK↑		0	0	ns
		$\overline{\text{PEN}}$ high after LDCK low		0	0	
		$\overline{\text{PEN}}$ low after LDCK↑		3	3	
		LDCK inactive after $\overline{\text{RESET}}$ high		6	6	
T_A	Operating free-air temperature	0	70	0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
VOH	Flags, Q outputs	VCC = MIN to MAX,	I _{OH} = – 100 μA	VCC–0.2		2.4	V
		VCC = 3 V,	I _{OH} = – 8 mA				
VOL	Flags, Q outputs	VCC = MIN to MAX,	I _{OL} = 100 μA			0.2	V
	Flags	VCC = 3 V,	I _{OL} = 8 mA			0.4	
	Q outputs	VCC = 3 V,	I _{OL} = 16 mA			0.55	
I _I		VCC = 3.6 V,	V _I = VCC or GND			±5	μA
I _{OZ}		VCC = 3.6 V,	V _O = VCC or GND			±10	μA
I _{CC}		VCC = 3.6 V,	V _I = VCC or GND and I _O = 0			40	μA
ΔI _{CC} §		VCC = 3.6 V, Other inputs at VCC or GND	One input at VCC–0.6 V,			500	μA
C _i		VCC = 3.3 V,	V _I = VCC or GND			3	pF
C _o		VCC = 3.3 V,	V _O = VCC or GND			6	pF

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at VCC = 3.3 V, TA = 25°C.

§ This is the supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or VCC.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, CL = 50 pF (unless otherwise noted) (see Figure 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	'ALVC7804-25 VCC = 3.3 V ± 0.3 V		'ALVC7804-40 VCC = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	
f _{max}	LDCK or UNCK		40		25		MHz
t _{pd}	LDCK↑	Any Q	9	22	9	24	ns
t _{pd}	UNCK↑		6	18	6	20	
t _{PLH}	LDCK↑	EMPTY	6	17	6	19	ns
t _{PHL}	UNCK↑		6	17	6	19	
t _{PHL}	RESET low		4	18	4	20	
t _{PHL}	LDCK↑	FULL	6	17	6	19	ns
t _{PLH}	UNCK↑		6	17	6	19	
t _{PLH}	RESET low		4	20	4	22	
t _{pd}	LDCK↑	AF/AE	7	20	7	22	ns
t _{pd}	UNCK↑		7	20	7	22	
t _{PLH}	RESET low		2	12	2	14	
t _{PLH}	LDCK↑	HF	5	20	5	22	ns
t _{PHL}	UNCK↑		7	20	7	22	
t _{PHL}	RESET low		3	14	3	16	
t _{en}	OE	Any Q	2	10	2	11	ns
t _{dis}			2	11	2	12	

operating characteristics, VCC = 3.3 V, TA = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C _{pd}	Power dissipation capacitance per FIFO channel	Outputs enabled CL = 50 pF, f = 5 MHz	53	pF

APPLICATION INFORMATION

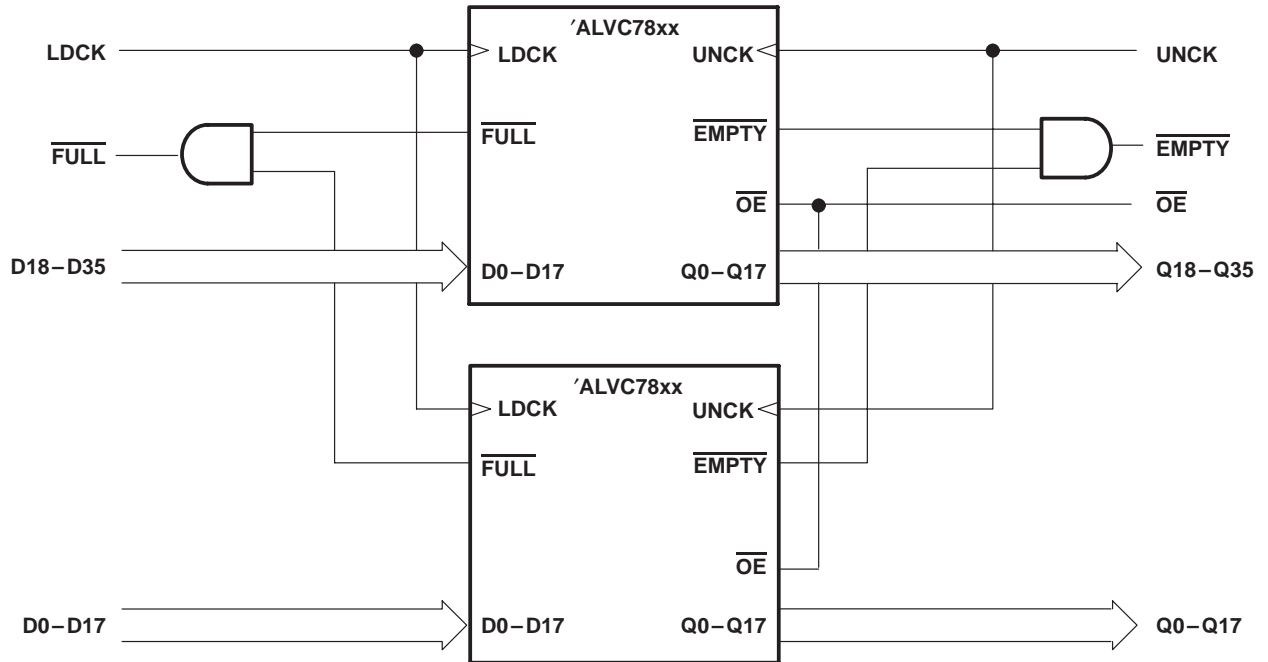


Figure 3. Word-Width Expansion: 512 × 36 Bit

TYPICAL CHARACTERISTICS

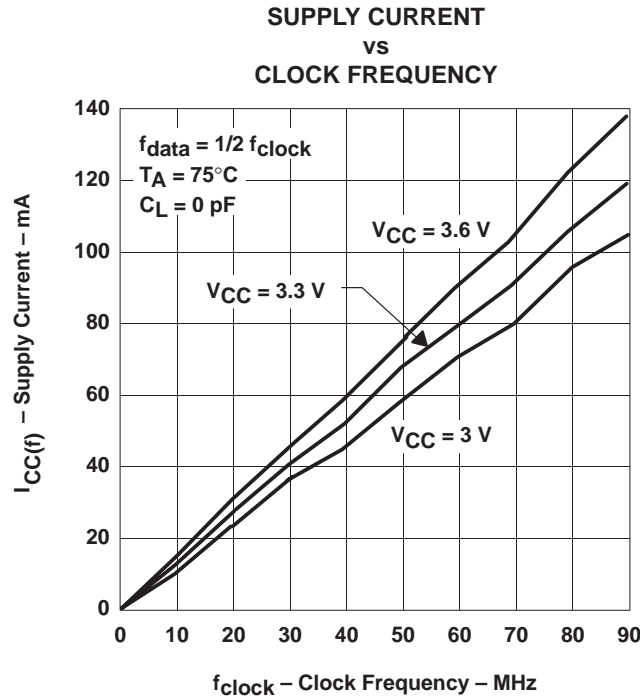


Figure 4

calculating power dissipation

With $I_{CC}(f)$ taken from Figure 4, the dynamic power (P_d), based on all data outputs changing states on each read, can be calculated by using:

$$P_d = V_{CC} \times [I_{CC}(f) + (N \times \Delta I_{CC} \times dc)] + \Sigma(C_L \times V_{CC}^2 \times f_o)$$

A more accurate total power (P_T) can be calculated if quiescent power (P_q) is also taken into consideration. Quiescent power (P_q) can be calculated using:

$$P_q = V_{CC} \times [I_{CCI} + (N \times \Delta I_{CC} \times dc)]$$

Total power will be:

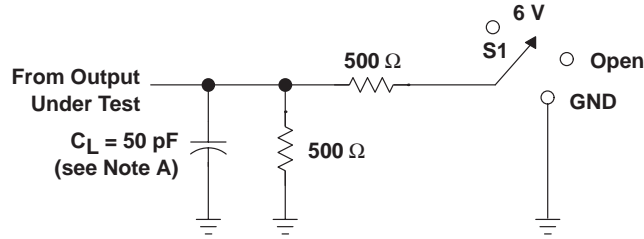
$$P_T = P_d + P_q$$

The above equations provide worst-case power calculations.

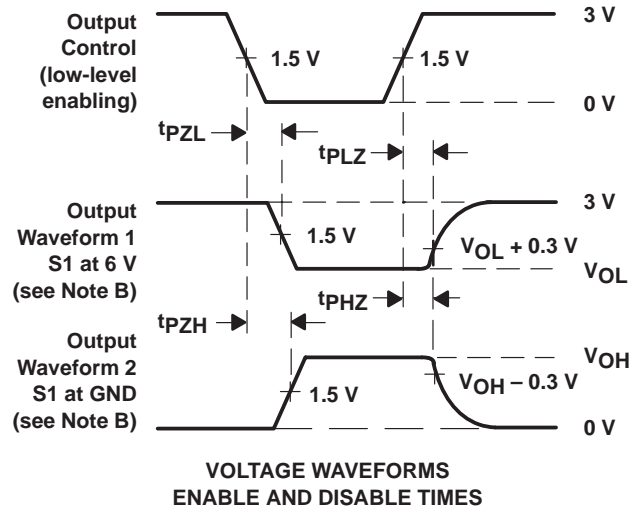
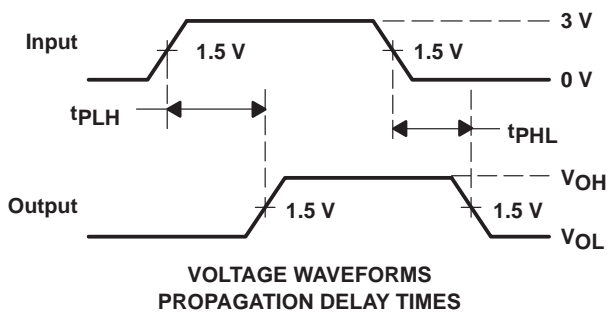
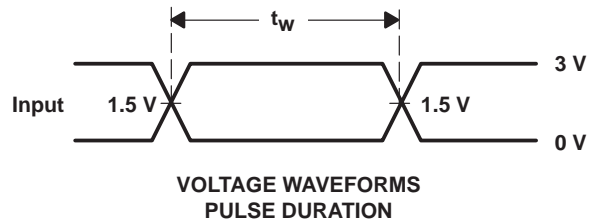
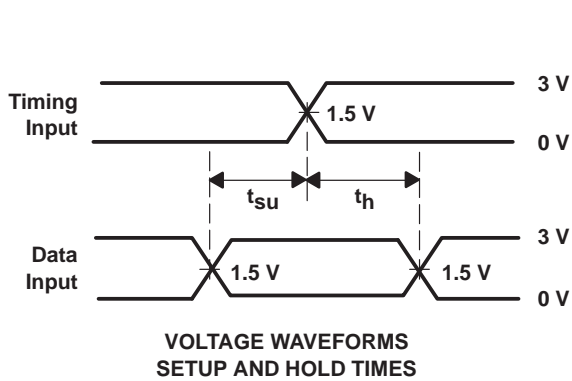
Where:

- N = number of inputs driven by TTL levels
- ΔI_{CC} = increase in power supply current for each input at a TTL high level
- dc = duty cycle of inputs at a TTL high level of 3.4 V
- C_L = output capacitance load
- f_o = switching frequency of an output
- I_{CCI} = idle current, supply current when FIFO is idle $\approx pF \times f_{clock} = 0.2 \times f_{clock}$
 (current is due to free-running clocks)
- pF = power factor (the slope of idle I_{CC} versus frequency)
- $I_{CC}(f)$ = active current, supply current when FIFO is transferring data

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT FOR OUTPUTS



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.

3-STATE OUTPUTS (ANY Q)

PARAMETER		R1, R2	C_L^\dagger	S1
t_{en}	t_{PZH}	500 Ω	50 pF	GND
	t_{PZL}			6 V
t_{dis}	t_{PHZ}	500 Ω	50 pF	GND
	t_{PLZ}			6 V
t_{pd}	t_{PLH}/t_{PHL}	500 Ω	50 pF	Open

† Includes probe and test-fixture capacitance

Figure 5. Standard CMOS Outputs (FULL, EMPTY, HF, AF/AE)

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74ALVC7804-25DL	ACTIVE	SSOP	DL	56	20	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		ALVC7804-25	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74ALVC7804-25DL	DL	SSOP	56	20	473.7	14.24	5110	7.87

MECHANICAL DATA

DL (R-PDSO-G56)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - Falls within JEDEC MO-118

PowerPAD is a trademark of Texas Instruments.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2024, Texas Instruments Incorporated