

# SN54AS1000A, SN74AS1000A QUADRUPLE 2-INPUT POSITIVE-NAND BUFFERS/DRIVERS

SDAS056B – APRIL 1984 – REVISED JANUARY 1995

- Driver Version of 'AS00
- High Capacitive-Drive Capability
- Package Options Include Plastic Small-Outline (D) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

## description

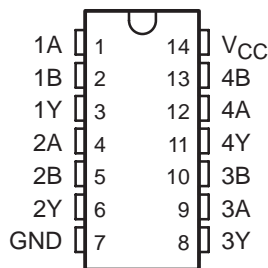
These devices contain four independent 2-input positive-NAND buffers/drivers. They perform the Boolean functions  $Y = \overline{A \cdot B}$  or  $Y = \overline{A + B}$  in positive logic.

The SN54AS1000A is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74AS1000A is characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

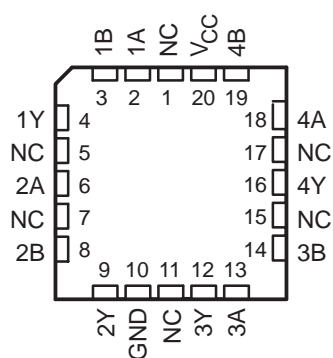
FUNCTION TABLE  
(each gate)

INPUTS		OUTPUT Y
A	B	
H	H	L
L	X	H
X	L	H

SN54AS1000A ... J PACKAGE  
SN74AS1000A ... D OR N PACKAGE  
(TOP VIEW)

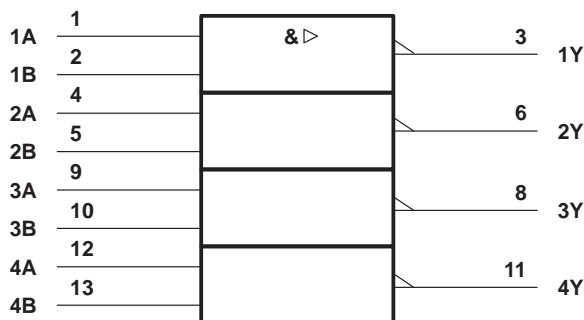


SN54AS1000A ... FK PACKAGE  
(TOP VIEW)

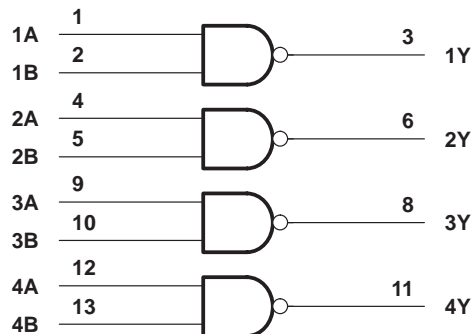


NC – No internal connection

## logic symbol†



## logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for the D, J, and N packages.

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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, $V_{CC}$	7 V
Input voltage, $V_I$	7 V
Operating free-air temperature range, $T_A$ : SN54AS1000A	-55°C to 125°C
SN74AS1000A	0°C to 70°C
Storage temperature range	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## recommended operating conditions‡

		SN54AS1000A			SN74AS1000A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	2			2			V
$V_{IL}$	Low-level input voltage			0.8			0.8	V
$I_{OH}$	High-level output current			-40			-48	mA
$I_{OL}$	Low-level output current			40			48	mA
$T_A$	Operating free-air temperature	-55		125	0		70	°C

‡ These high sink- or source-current devices are not recommended for use above 40 MHz.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54AS1000A			SN74AS1000A			UNIT
		MIN	TYP§	MAX	MIN	TYP§	MAX	
$V_{IK}$	$V_{CC} = 4.5 V$ , $I_I = -18 mA$			-1.2			-1.2	V
$V_{OH}$	$V_{CC} = 4.5 V$ to $5.5 V$ , $I_{OH} = -2 mA$	$V_{CC} - 2$			$V_{CC} - 2$			V
	$V_{CC} = 4.5 V$ , $I_{OH} = -3 mA$	2.4	3.2		2.4	3.2		
	$V_{CC} = 4.5 V$ , $I_{OH} = -40 mA$	2						
$V_{OL}$	$V_{CC} = 4.5 V$ , $I_{OH} = -48 mA$				2			V
	$V_{CC} = 4.5 V$ , $I_{OL} = 40 mA$	0.25			0.5			
	$V_{CC} = 4.5 V$ , $I_{OL} = 48 mA$				0.35			
$I_I$	$V_{CC} = 5.5 V$ , $V_I = 7 V$			0.1			0.1	mA
$I_{IH}$	$V_{CC} = 5.5 V$ , $V_I = 2.7 V$			20			20	μA
$I_{IL}$	$V_{CC} = 5.5 V$ , $V_I = 0.4 V$			-0.5			-0.5	mA
$I_{O}^{\parallel}$	$V_{CC} = 5.5 V$ , $V_O = 2.25 V$	-30		-200	-50		-200	mA
$I_{CCH}$	$V_{CC} = 5.5 V$ , $V_I = 0$		2.2	3.5		2.2	3.5	mA
$I_{CCL}$	$V_{CC} = 5.5 V$ , $V_I = 4.5 V$		12	19		12	19	mA

§ All typical values are at  $V_{CC} = 5 V$ ,  $T_A = 25^\circ C$ .

¶ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current,  $I_{OS}$ .



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## switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$ $C_L = 50 \text{ pF},$ $R_L = 500 \Omega,$ $T_A = \text{MIN to MAX}^\dagger$				UNIT
			SN54AS1000A		SN74AS1000A		
			MIN	MAX	MIN	MAX	
$t_{PLH}$	A or B	Y	1	5	1	4	ns
$t_{PHL}$			1	5	1	4	

<sup>†</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



# SN54AS1000A, SN74AS1000A QUADRUPLE 2-INPUT POSITIVE-NAND BUFFERS/DRIVERS

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## PARAMETER MEASUREMENT INFORMATION SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.  
 D. All input pulses have the following characteristics:  $PRR \leq 1$  MHz,  $t_r = t_f = 2$  ns, duty cycle = 50%.  
 E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9162701M2A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9162701M2A SNJ54AS 1000AFK	Samples
5962-9162701MCA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9162701MC A SNJ54AS1000AJ	Samples
SN74AS1000AD	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	0 to 70	AS1000A	
SN74AS1000ADR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	AS1000A	Samples
SN74AS1000AN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74AS1000AN	Samples
SN74AS1000ANSR	ACTIVE	SOP	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	74AS1000A	Samples
SNJ54AS1000AFK	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9162701M2A SNJ54AS 1000AFK	Samples
SNJ54AS1000AJ	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9162701MC A SNJ54AS1000AJ	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=100ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN54AS1000A, SN74AS1000A :**

- Catalog : [SN74AS1000A](#)
- Military : [SN54AS1000A](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AS1000ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74AS1000ANSR	SOP	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AS1000ADR	SOIC	D	14	2500	356.0	356.0	35.0
SN74AS1000ANSR	SOP	NS	14	2000	356.0	356.0	35.0



**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-9162701M2A	FK	LCCC	20	55	506.98	12.06	2030	NA
SN74AS1000AN	N	PDIP	14	25	506	13.97	11230	4.32
SN74AS1000AN	N	PDIP	14	25	506	13.97	11230	4.32
SNJ54AS1000AFK	FK	LCCC	20	55	506.98	12.06	2030	NA

D0014A



# PACKAGE OUTLINE

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

# EXAMPLE BOARD LAYOUT

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

## GENERIC PACKAGE VIEW

**FK 20**

**LCCC - 2.03 mm max height**

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

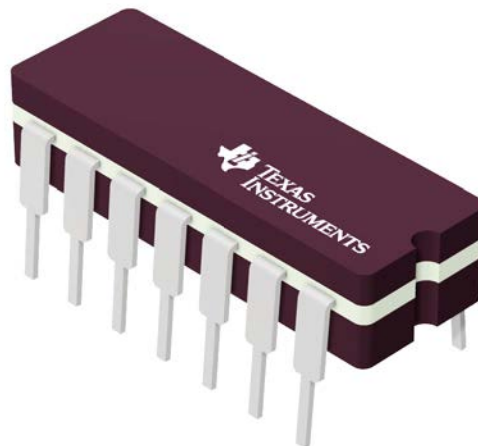
This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4229370VA\

J 14

**GENERIC PACKAGE VIEW**  
**CDIP - 5.08 mm max height**  
CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4040083-5/G

# J0014A



## PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

### NOTES:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.



# EXAMPLE BOARD LAYOUT

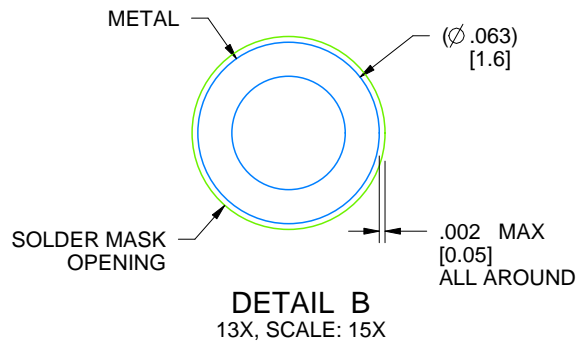
J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE  
NON-SOLDER MASK DEFINED  
SCALE: 5X



4214771/A 05/2017

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

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