

SN74AUC1G19 1-of-2 Decoder/Demultiplexer

1 Features

- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)
- Available in the Texas Instruments NanoFree™ Package
- Optimized for 1.8-V Operation and Is 3.6-V I/O Tolerant to Support Mixed-Mode Signal Operation
- I_{off} Supports Partial-Power-Down Mode Operation
- Sub-1-V Operable
- ± 8 -mA Output Drive at 1.8 V V_{CC}
- Maximum t_{pd} of 3 ns at 1.8 V
- Low Power Consumption, 10- μ A Maximum I_{CC}

2 Applications

- AV Receiver
- Audio Dock: Portable
- Blu-ray Player and Home Theater
- Embedded PC
- MP3 Player/Recorder (Portable Audio)
- Personal Digital Assistant (PDA)
- Power: Telecom/Server AC/DC Supply: Single Controller: Analog and Digital
- Solid State Drive (SSD): Client and Enterprise
- TV: LCD/Digital and High-Definition (HDTV)
- Tablet: Enterprise
- Video Analytics: Server
- Wireless Headset, Keyboard, and Mouse

3 Description

This 1-of-2 decoder/demultiplexer is operational at 0.8-V to 2.7-V V_{CC} , but is designed specifically for 1.65-V to 1.95-V V_{CC} operation.

The SN74AUC1G19 is a 1-of-2 decoder/demultiplexer. This device buffers the data on input A and passes it to the outputs Y_0 (true) and Y_1 (complement) when the enable (\bar{E}) input signal is low.

NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

For more information about AUC Little Logic devices, see [Applications of Texas Instruments AUC Sub-1-V Little Logic Devices](#), SCEA027.

Device Information⁽¹⁾

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|----------------|-------------|-------------------|
| SN74AUC1G19DBV | SOT-23 (6) | 2.90 mm × 1.60 mm |
| SN74AUC1G19DCK | SC70 (6) | 2.00 mm × 1.25 mm |
| SN74AUC1G19DRL | SOT-5X3 (6) | 1.60 mm × 1.20 mm |
| SN74AUC1G19YZP | DSBGA (6) | 1.50 mm × 0.90 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Logic Diagram (Positive Logic)

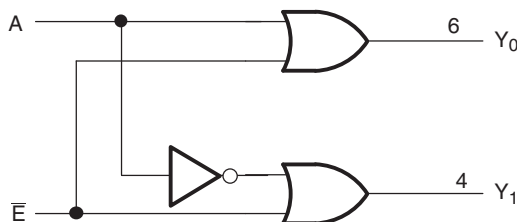


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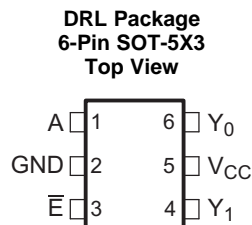
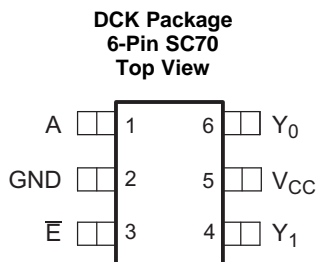
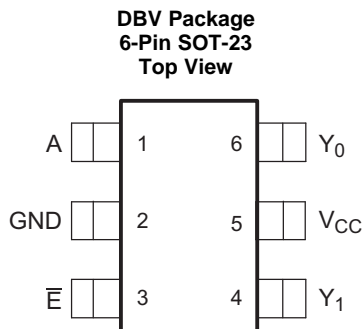
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4 Revision History

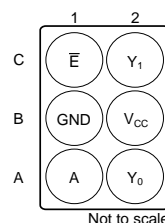
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision D (April 2007) to Revision E | Page |
|---|-------------|
| • Deleted DRY package throughout data sheet..... | 1 |
| • Added <i>Application</i> section, <i>Device Information</i> table, <i>Pin Configuration and Functions</i> section, <i>ESD Ratings</i> table, <i>Thermal Information</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section..... | 1 |
| • Deleted <i>Ordering Information</i> table, see <i>Mechanical, Packaging, and Orderable Information</i> at the end of the data sheet | 1 |

5 Pin Configuration and Functions



**YZP Package
6-Pin DSBGA
Bottom View**



See mechanical drawings for dimensions.

Pin Functions

| NAME | PIN | | I/O | DESCRIPTION |
|-----------------|---------------|-----|-----|------------------------------------|
| | DBV, DCK, DRL | YZP | | |
| A | 1 | A1 | I | A Input |
| \bar{E} | 3 | C1 | I | Active Low Enable |
| GND | 2 | B1 | — | Ground |
| V _{CC} | 5 | B2 | — | Positive Supply |
| Y ₀ | 6 | A2 | O | Y ₀ True Output |
| Y ₁ | 4 | C2 | O | Y ₁ Complemented Output |

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | MIN | MAX | UNIT |
|------------------|---|--------------------|-----------------------|---------|
| V _{CC} | Supply voltage | -0.5 | 3.6 | V |
| V _I | Input voltage ⁽²⁾ | -0.5 | 3.6 | V |
| V _O | Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾ | -0.5 | 3.6 | V |
| V _O | Voltage range applied to any output in the high or low state ^{(2) (3)} | -0.5 | V _{CC} + 0.5 | V |
| I _{IK} | Input clamp current | V _I < 0 | | -50 mA |
| I _{OK} | Output clamp current | V _O < 0 | | -50 mA |
| I _O | Continuous output current | | | ±20 mA |
| | Continuous current through V _{CC} or GND | | | ±100 mA |
| T _{stg} | Storage temperature | -65 | 150 | °C |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V_{CC} is provided in the recommended operating conditions table.

6.2 ESD Ratings

| | | VALUE | UNIT |
|--------------------|-------------------------|--|------|
| V _(ESD) | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | 2000 |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾ | 1000 |
| | | Machine Model (A115-A) | 200 |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

See⁽¹⁾

| | | MIN | MAX | UNIT |
|-----------------|------------------------------------|-----------------------------------|------------------------|------------------------|
| V _{CC} | Supply voltage | 0.8 | 2.7 | V |
| V _{IH} | High-level control input voltage | V _{CC} = 0.8 V | V _{CC} | 3.6 |
| | | V _{CC} = 1.1 V to 1.95 V | 0.65 × V _{CC} | 3.6 |
| | | V _{CC} = 2.3 V to 2.7 V | 1.7 | 3.6 |
| V _{IL} | Low-level control input voltage | V _{CC} = 0.8 V | 0 | |
| | | V _{CC} = 1.1 V to 1.95 V | 0 | 0.35 × V _{CC} |
| | | V _{CC} = 2.3 V to 2.7 V | 0 | 0.7 |
| V _O | Output voltage | 0 | V _{CC} | V |
| I _{OH} | High-level control output current | V _{CC} = 0.8 V | –0.7 | |
| | | V _{CC} = 1.1 V | –3 | |
| | | V _{CC} = 1.4 V | –5 | |
| | | V _{CC} = 1.65 V | –8 | |
| | | V _{CC} = 2.3 V | –9 | |
| I _{OL} | Low-level control output current | V _{CC} = 0.8 V | 0.7 | |
| | | V _{CC} = 1.1 V | 3 | |
| | | V _{CC} = 1.4 V | 5 | |
| | | V _{CC} = 1.65 V | 8 | |
| | | V _{CC} = 2.3 V | 9 | |
| Δt/Δv | Input transition rise or fall rate | V _{CC} = 0.8 V to 1.95 V | 20 | |
| | | V _{CC} = 2.3 V to 2.7 V | 15 | |
| T _A | Operating free-air temperature | –40 | 85 | °C |

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See [Implications of Slow or Floating CMOS Inputs](#), SCBA004.

6.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | SN74AUC1G19 | | | | UNIT | |
|-------------------------------|--|------------|---------------|-------------|------|------|
| | DBV (SOT-23) | DCK (SC70) | DRL (SOT-5X3) | YZP (DSBGA) | | |
| | 6 PINS | 6 PINS | 6 PINS | 6 PINS | | |
| R _{θJA} | Junction-to-ambient thermal resistance | 206 | 252 | 142 | 132 | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP ⁽¹⁾ | MAX | UNIT |
|------------------|---|-----------------|-----------------------|--------------------|-----|------|
| V _{OH} | I _{OH} = -100 μA | 0.8 V to 2.7 V | V _{CC} - 0.1 | | | V |
| | I _{OH} = -0.7 mA | 0.8 V | 0.55 | | | |
| | I _{OH} = -3 mA | 1.1 V | 0.8 | | | |
| | I _{OH} = -5 mA | 1.4 V | 1 | | | |
| | I _{OH} = -8 mA | 1.65 V | 1.2 | | | |
| | I _{OH} = -9 mA | 2.3 V | 1.8 | | | |
| V _{OL} | I _{OL} = 100 μA | 0.8 V to 2.7 V | 0.2 | | | V |
| | I _{OL} = 0.7 mA | 0.8 V | 0.25 | | | |
| | I _{OL} = 3 mA | 1.1 V | 0.3 | | | |
| | I _{OL} = 5 mA | 1.4 V | 0.4 | | | |
| | I _{OL} = 8 mA | 1.65 V | 0.45 | | | |
| | I _{OL} = 9 mA | 2.3 V | 0.6 | | | |
| I _I | V _I = V _{CC} or GND | 0 to 2.7 V | ±5 | | | μA |
| I _{off} | V _I or V _O = 2.7 V | 0 | ±10 | | | μA |
| I _{CC} | V _I = V _{CC} or GND, I _O = 0 | 0.8 V to 2.7 V | 10 | | | μA |
| C _I | V _I = V _{CC} or GND | 2.5 V | 3 | | | pF |

(1) All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.

6.6 Switching Characteristics: C_L = 15 pF

over recommended operating free-air temperature range, C_L = 15 pF (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V _{CC} = 0.8 V | | V _{CC} = 1.1 V ± 0.1 V | | V _{CC} = 1.5 V ± 0.1 V | | V _{CC} = 1.8 V ± 0.15 V | | V _{CC} = 2.5 V ± 0.2 V | | UNIT |
|-----------------|----------------|-------------|-------------------------|-----|---------------------------------|-----|---------------------------------|-----|----------------------------------|-----|---------------------------------|----|------|
| | | | TYP | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | | |
| t _{pd} | A or \bar{E} | Y | 7.5 | 0.5 | 4.6 | 0.4 | 3.0 | 0.3 | 2.4 | 0.2 | 1.7 | ns | |

6.7 Switching Characteristics: C_L = 30 pF

over recommended operating free-air temperature range, C_L = 30 pF (unless otherwise noted) (see Figure 1)

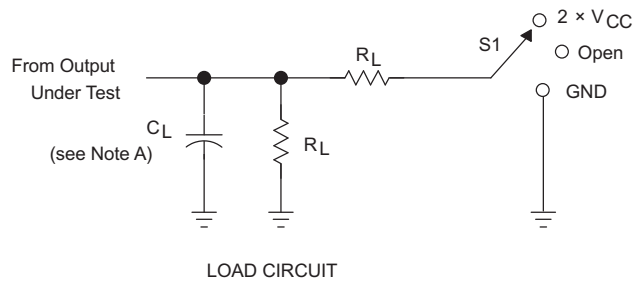
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V _{CC} = 1.8 V ± 0.15 V | | V _{CC} = 2.5 V ± 0.2 V | | UNIT |
|-----------------|----------------|----------------------------------|----------------------------------|-----|---------------------------------|-----|------|
| | | | MIN | MAX | MIN | MAX | |
| t _{pd} | A or \bar{E} | Y ₀ or Y ₁ | 0.5 | 2.8 | 0.4 | 2.0 | ns |

6.8 Operating Characteristics

T_A = 25°C

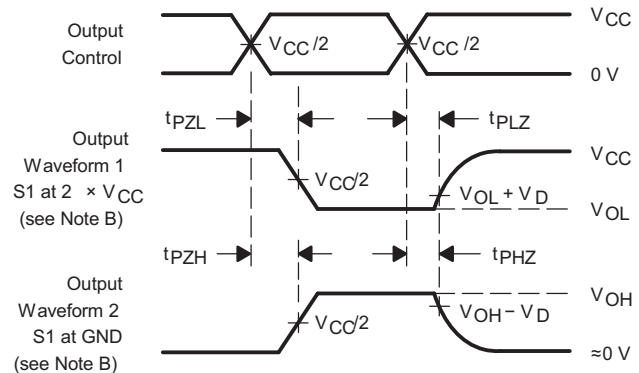
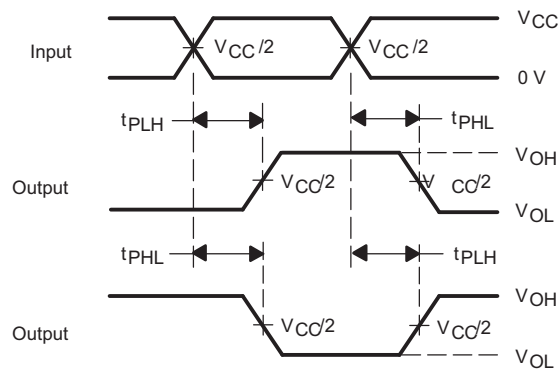
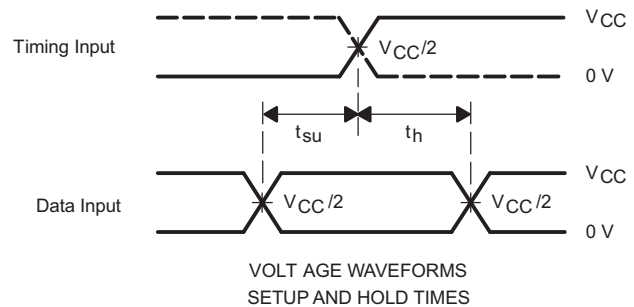
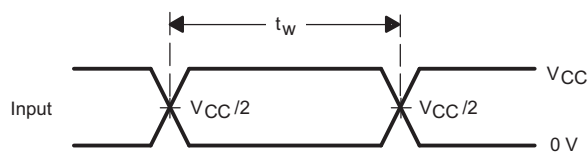
| PARAMETER | TEST CONDITIONS | V _{CC} = 0.8 V | V _{CC} = 1.2 V | V _{CC} = 1.5 V | V _{CC} = 1.8 V | V _{CC} = 2.5 V | UNIT |
|-----------------|---|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|------|
| | | TYP | TYP | TYP | TYP | TYP | |
| C _{pd} | Power dissipation capacitance f = 10 MHz | 13 | 13 | 13 | 13 | 14 | pF |

7 Parameter Measurement Information



| TEST | S1 |
|-------------------|-------------------|
| t_{PLH}/t_{PHL} | Open |
| t_{PLZ}/t_{PZL} | $2 \times V_{CC}$ |
| t_{PHZ}/t_{PZH} | GND |

| V_{CC} | C_L | R_L | V_D |
|--------------------|-------|--------------|--------|
| 0.8 V | 15 pF | 2 k Ω | 0.1 V |
| 1.2 V \pm 0.1 V | 15 pF | 2 k Ω | 0.1 V |
| 1.5 V \pm 0.1 V | 15 pF | 2 k Ω | 0.1 V |
| 1.8 V \pm 0.15 V | 15 pF | 2 k Ω | 0.15 V |
| 2.5 V \pm 0.2 V | 15 pF | 2 k Ω | 0.15 V |
| 1.8 V \pm 0.15 V | 30 pF | 1 k Ω | 0.15 V |
| 2.5 V \pm 0.2 V | 30 pF | 500 Ω | 0.15 V |



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_o = 50 \Omega$, slew rate \leq 1 V/ns.
 - The outputs are measured one at a time, with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .
 - All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Functional Block Diagram

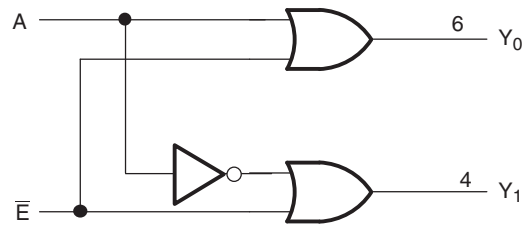


Figure 2. Logic Diagram (Positive Logic)

8.2 Device Functional Modes

Table 1 lists the functional mode of the SN74AUC1G19.

Table 1. Function Table

| INPUTS | | OUTPUTS | |
|-----------|---|----------------|----------------|
| \bar{E} | A | Y ₀ | Y ₁ |
| L | L | L | H |
| L | H | H | L |
| H | X | H | H |

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation see the following:

- [Applications of Texas Instruments AUC Sub-1-V Little Logic Devices](#), SCEA027
- [Implications of Slow or Floating CMOS Inputs](#), SCBA004

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

9.4 Trademarks

NanoFree, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| SN74AUC1G19DBVR | ACTIVE | SOT-23 | DBV | 6 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | U19R | Samples |
| SN74AUC1G19DCKR | ACTIVE | SC70 | DCK | 6 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | U5R | Samples |
| SN74AUC1G19DCKT | ACTIVE | SC70 | DCK | 6 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | U5R | Samples |
| SN74AUC1G19DRLR | ACTIVE | SOT-5X3 | DRL | 6 | 4000 | RoHS & Green | NIPDAU NIPDAUAG | Level-1-260C-UNLIM | -40 to 85 | (1KA, U57, U5R) | Samples |
| SN74AUC1G19YZPR | ACTIVE | DSBGA | YZP | 6 | 3000 | RoHS & Green | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | U5N | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

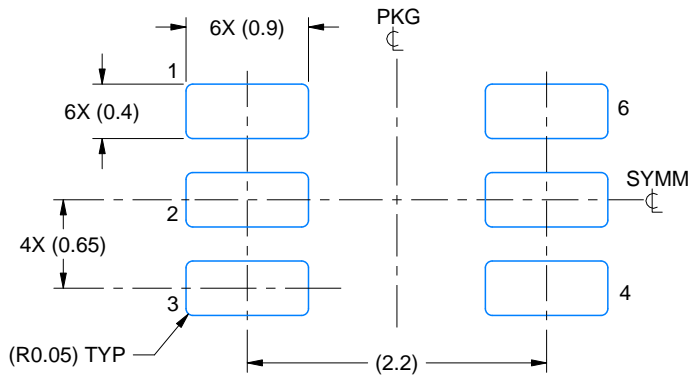

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74AUC1G19DBVR | SOT-23 | DBV | 6 | 3000 | 180.0 | 8.4 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| SN74AUC1G19DCKR | SC70 | DCK | 6 | 3000 | 180.0 | 8.4 | 2.41 | 2.41 | 1.2 | 4.0 | 8.0 | Q3 |
| SN74AUC1G19DCKT | SC70 | DCK | 6 | 250 | 180.0 | 8.4 | 2.41 | 2.41 | 1.2 | 4.0 | 8.0 | Q3 |
| SN74AUC1G19DRLR | SOT-5X3 | DRL | 6 | 4000 | 180.0 | 8.4 | 2.0 | 1.8 | 0.75 | 4.0 | 8.0 | Q3 |
| SN74AUC1G19YZPR | DSBGA | YZP | 6 | 3000 | 178.0 | 9.2 | 1.02 | 1.52 | 0.63 | 4.0 | 8.0 | Q1 |

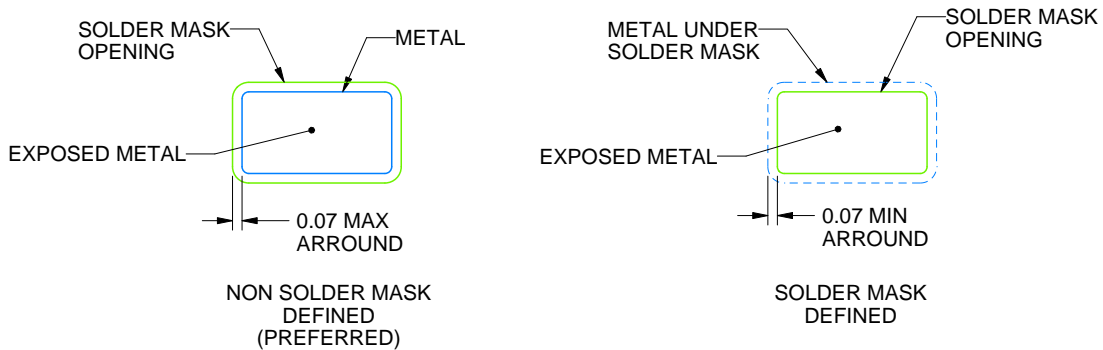
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74AUC1G19DBVR | SOT-23 | DBV | 6 | 3000 | 202.0 | 201.0 | 28.0 |
| SN74AUC1G19DCKR | SC70 | DCK | 6 | 3000 | 202.0 | 201.0 | 28.0 |
| SN74AUC1G19DCKT | SC70 | DCK | 6 | 250 | 202.0 | 201.0 | 28.0 |
| SN74AUC1G19DRLR | SOT-5X3 | DRL | 6 | 4000 | 210.0 | 185.0 | 35.0 |
| SN74AUC1G19YZPR | DSBGA | YZP | 6 | 3000 | 220.0 | 220.0 | 35.0 |



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

4214835/C 08/2024

NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214835/C 08/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

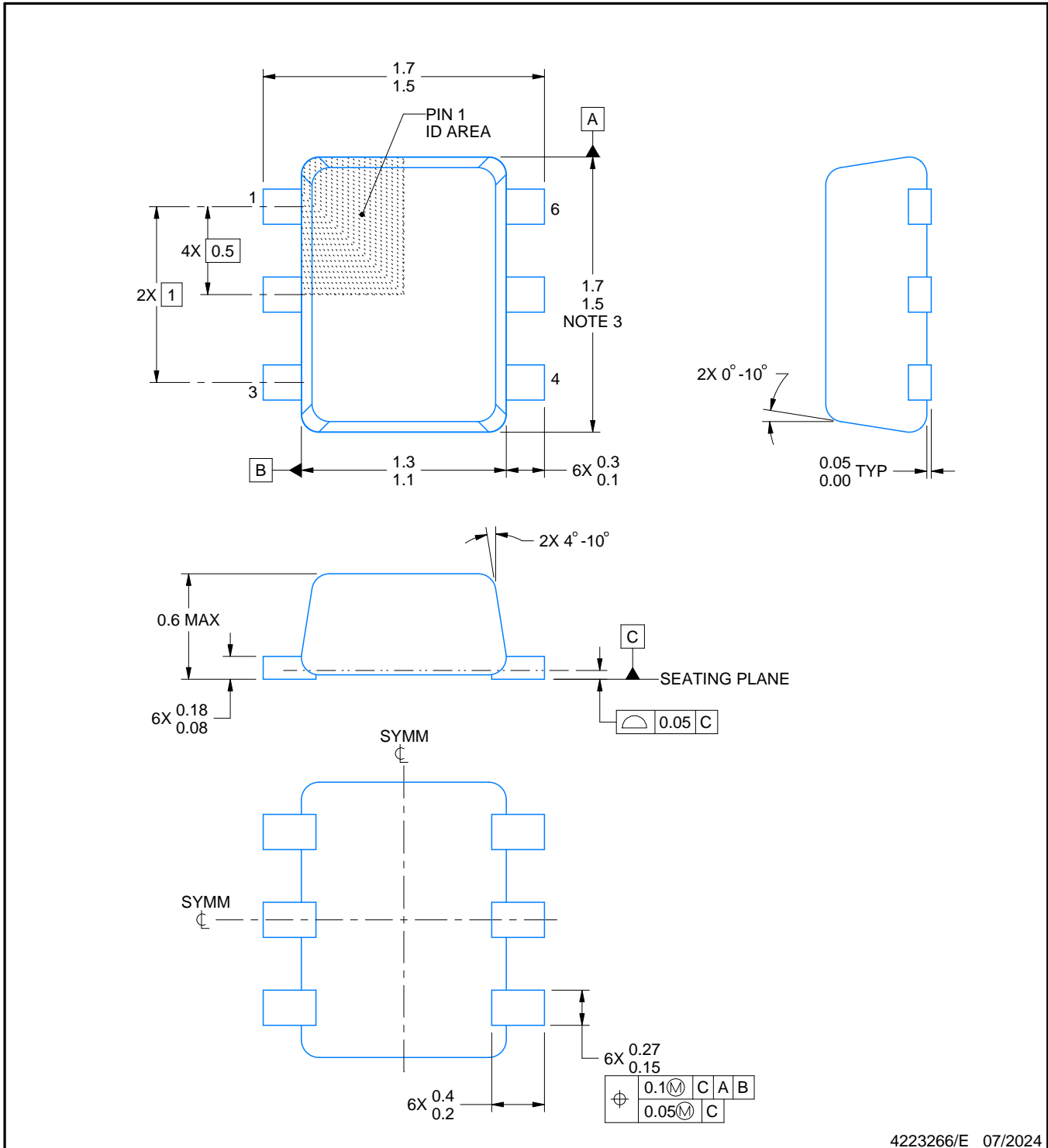
DRL0006A



PACKAGE OUTLINE

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



4223266/E 07/2024

NOTES:

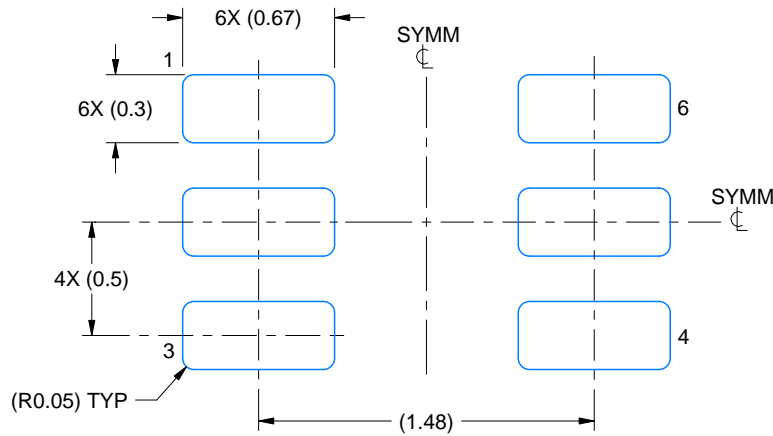
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD

EXAMPLE BOARD LAYOUT

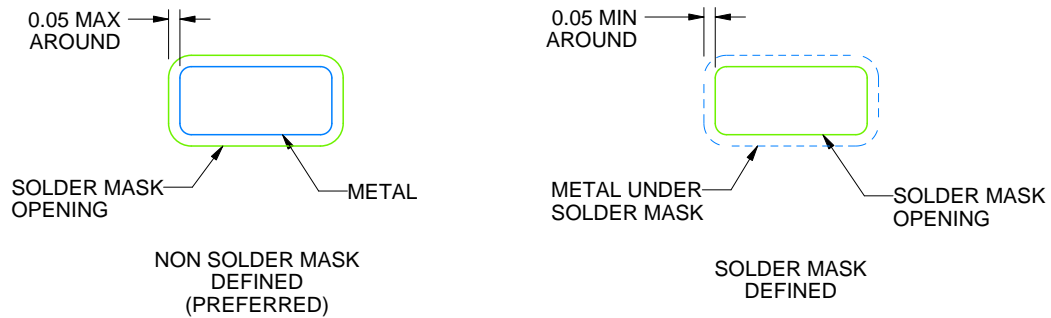
DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
SCALE:30X



SOLDERMASK DETAILS

4223266/E 07/2024

NOTES: (continued)

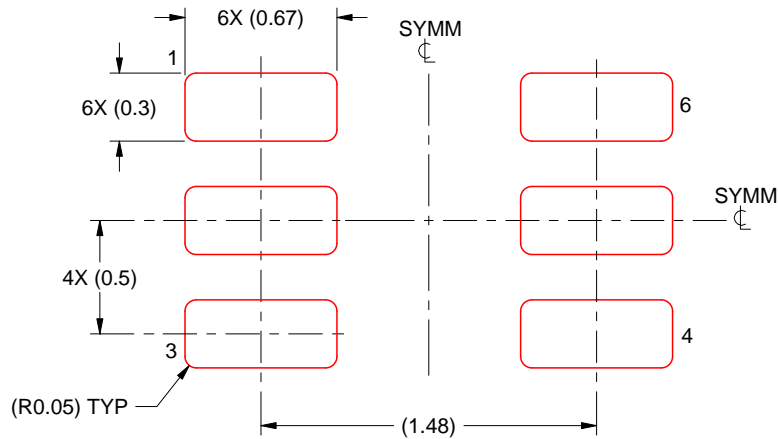
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.

EXAMPLE STENCIL DESIGN

DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4223266/E 07/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



DBV0006A

PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214840/G 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Reference JEDEC MO-178.

EXAMPLE BOARD LAYOUT

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214840/G 08/2024

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

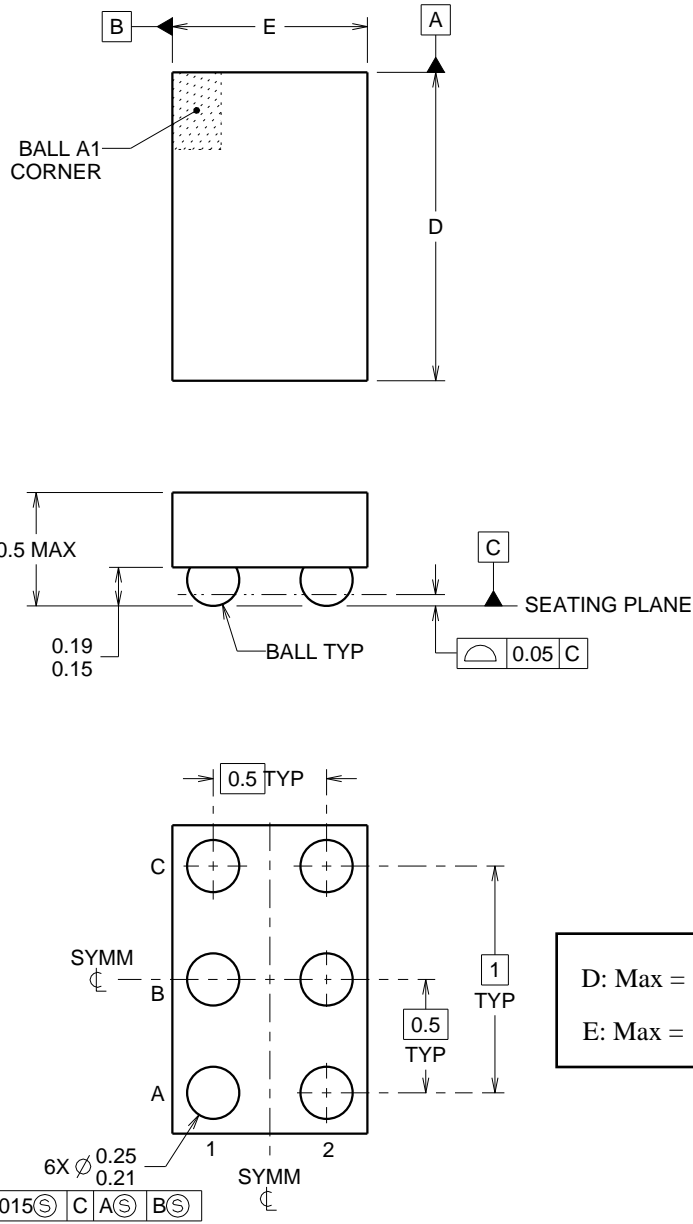


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/G 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



D: Max = 1.418 mm, Min = 1.358 mm
E: Max = 0.918 mm, Min = 0.858 mm

4219524/A 06/2014

NOTES:

NanoFree Is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. NanoFree™ package configuration.

EXAMPLE BOARD LAYOUT

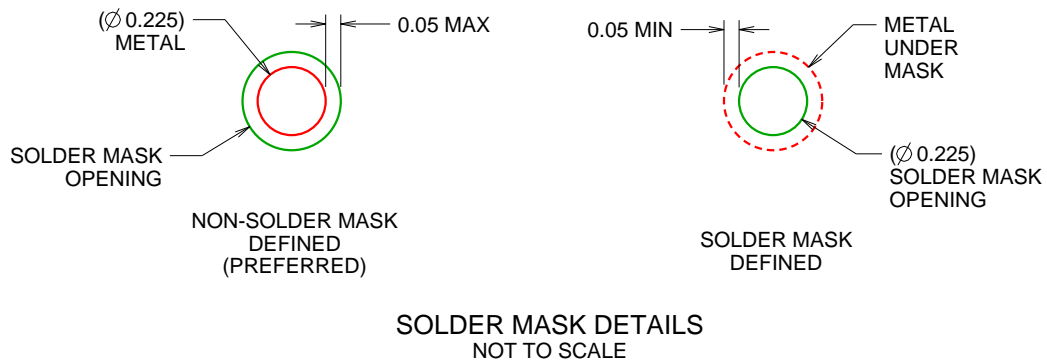
YZP0006

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:40X



SOLDER MASK DETAILS
NOT TO SCALE

4219524/A 06/2014

NOTES: (continued)

- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SBVA017 (www.ti.com/lit/sbva017).

EXAMPLE STENCIL DESIGN

YZP0006

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4219524/A 06/2014

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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