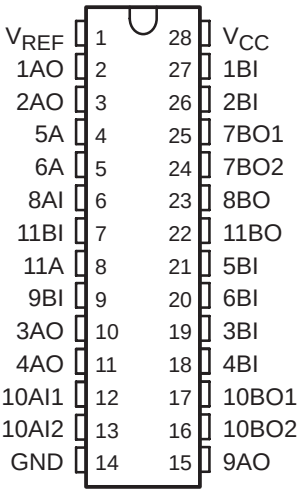
- **Operates as GTL-/GTL/GTL+ to LVTTL or LVTTL to GTL-/GTL/GTL+ Translator**
- **Series Termination on TTL Outputs of 30 Ω**
- **Latch-Up Testing to JEDEC Standard JESD 78 Exceeds 500 mA**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

PW PACKAGE
(TOP VIEW)



description

The SN74GTL2006 is a 13-bit translator to interface between the 3.3-V LVTTL chipset I/O and the Xeon™ processor GTL-/GTL/GTL+ I/O. The device is designed for platform health management in dual-processor applications.

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	V_{REF}	GTL reference voltage
2–6, 8, 10–13, 15	nAn	Data inputs/outputs (LVTTL)
7, 9, 16, 17–27	nBn	Data inputs/outputs (GTL−/GTL/GTL+)
14	GND	Ground (0 V)
28	V_{CC}	Positive supply voltage

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	TSSOP − PW	Tube	SN74GTL2006PW	GK2006
		Tape and reel	SN74GTL2006PWR	GK2006

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design, guidelines are available at www.ti.com/sc/package.

Function Tables

INPUTS 1BI/2BI/3BI/4BI/9BI	OUTPUTS 1AO/2AO/3AO/4AO/9AO
L	L
H	H

INPUT 8AI	OUTPUT 8BO
L	L
H	H

INPUTS		OUTPUTS
10AI1/10AI2	9BI	10BO1/10BO2
L	L	L
L	H	L
H	L	L
H	H	H

INPUTS 5BI/6BI	INPUTS/OUTPUTS 5A/6A (OPEN DRAIN)	OUTPUTS 7BO1/7BO2
L	L	H†
H	L‡	L
H	H	H

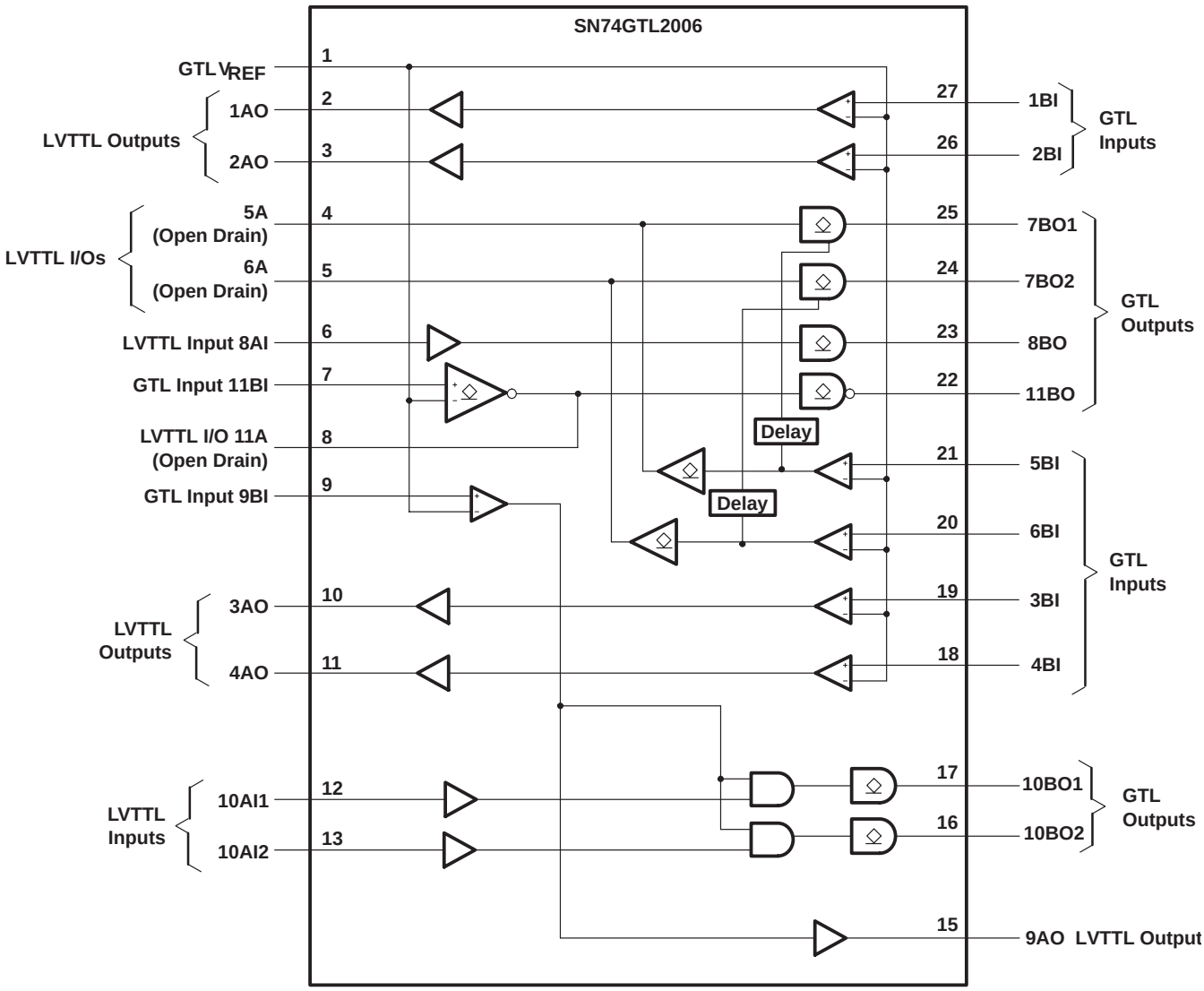
† The enable on 7BO1/7BO2 includes a delay that prevents a transient condition (when 5BI/6BI goes from low to high, and the low to high on 5A/6A lags up to 100 ns) from causing a low glitch on the 7BO1/7BO2 outputs.

‡ Open-drain input/output terminal is driven to a logic-low state by an external driver.

INPUT 11BI	INPUT/OUTPUT 11A (OPEN DRAIN)	OUTPUT 11BO
L	H	L
L	L‡	H
H	L	H

‡ Open-drain input/output terminal is driven to a logic-low state by an external driver.

logic symbol



NOTE A: The enable on 7BO1/7BO2 includes a delay that prevents a transient conditon (where 5BI/6BI go from low to high, and the low to high on 5A/6A lags up to 100 ns) from causing a low glitch on the 7BO1/7BO2 outputs.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†‡

Supply voltage range, V_{CC} . . . . . −0.5 to 4.6 V
Input voltage range, V_I (see Note 2): A port (LVTTL) . . . . . −0.5 to 4.6 V
B port (GTL) . . . . . −0.5 to 4.6 V
Output voltage range, V_O (output in OFF or HIGH state)(see Note 2): A port . . . . . −0.5 to 4.6 V
B port . . . . . −0.5 to 4.6 V
Input diode current, I_{IK} ($V_I < 0$) . . . . . −50 mA
Output diode current, I_{OK} ($V_O < 0$) . . . . . −50 mA
Current into any output in the LOW state: A port . . . . . 32 mA
B port . . . . . 30 mA
Current into any output in the HIGH state, A port . . . . . −32 mA
Storage temperature range, T_{stg} . . . . . −60 to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ Voltages are referenced to GND (ground = 0 V).

NOTES: 1. The performance capability of a high-performance integrated circuit, in conjunction with its thermal environment, can create junction temperatures that are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
2. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3	3.3	3.6	V
V_{TT}	Termination voltage	GTL−	0.85	0.9	0.95	V
		GTL	1.14	1.2	1.26	
		GTL+	1.35	1.5	1.65	
V_{REF}	Reference voltage	Overall	0.5	2/3 V_{TT}	1.8	V
		GTL−	0.5	0.6	0.63	
		GTL	0.76	0.8	0.84	
		GTL+	0.87	1	1.1	
V_I	Input voltage	A port	0	3.3	3.6	V
		B port	0	V_{TT}	3.6	
V_{IH}	High-level input voltage	A port	2			V
		B port	V_{REF} + 50 mV			
V_{IL}	Low-level input voltage	A port			0.8	V
		B port			V_{REF} − 50 mV	
I_{OH}	High-level output current	A port			−16	mA
I_{OL}	Low-level output current	A port			16	mA
		B port			15	
T_A	Operating free-air temperature range		−40		85	°C

electrical characteristics over recommended operating conditions

PARAMETER		TEST CONDITIONS		–40°C TO 85°C			UNIT
				MIN	TYP†	MAX	
V_{OH}‡	A port	V_{CC} = 3 V to 3.6 V,	I_{OH} = –100 μA	V_{CC} – 0.2			V
		V_{CC} = 3 V,	I_{OH} = –16 mA	2.1			
V_{OL}‡	A port	V_{CC} = 3 V,	I_{OL} = 16 mA			0.8	V
	B port	V_{CC} = 3 V,	I_{OL} = 15 mA			0.4	
I_I	A port	V_{CC} = 3.6 V	V_I = V_{CC}			±1	μA
			V_I = 0 V			±1	
	B port	V_{CC} = 3.6 V,	V_I = V_{TT} or GND			±1	
I_{CC}	A or B port	V_{CC} = 3.6 V,	V_I = V_{CC} or GND, I_O = 0			12	mA
ΔI_{CC}§	A port or control inputs	V_{CC} = 3.6 V,	V_I = V_{CC} – 0.6 V			500	μA
C_{IO}	A port	V_O = 3 V or 0,	V_O = 3 V or 0		5		pF
	B port	V_O = V_{TT} or 0,	V_O = V_{TT} or 0		4		

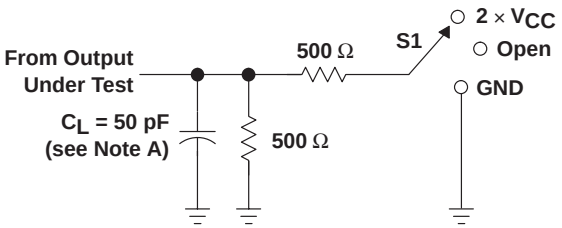
† All typical values are measured at V_{CC} = 3.3 V and T_A = 25°C.
‡ The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
§ This is the increase in supply current for each input that is at the specified LVTTL voltage, rather than V_{CC} or GND.

switching characteristics over recommended operating free-air temperature range

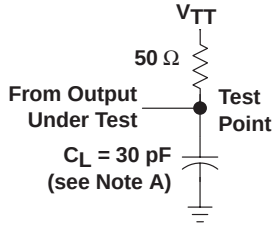
PARAMETER		WAVEFORM	GTL–			GTL			GTL+			UNIT
			V_{CC} = 3.3 V ± 0.3 V, V_{REF} = 0.6 V			V_{CC} = 3.3 V ± 0.3 V, V_{REF} = 0.8 V			V_{CC} = 3.3 V ± 0.3 V, V_{REF} = 1 V			
			MIN	TYP†	MAX	MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	An to Bn	1	2	4	8	2	4	8	2	4	8	ns
t_{PHL}			2	5.5	10	2	5.5	10	2	5.5	10	
t_{PLH}	Bn to An	2	2	5.5	10	2	5.5	10	2	5.5	10	ns
t_{PHL}			2	5.5	10	2	5.5	10	2	5.5	10	
t_{PLH}	9BI to 10BOn	3	2	6	11	2	6	11	2	6	11	ns
t_{PHL}			2	6	11	2	6	11	2	6	11	
t_{PLH}	11BI to 11BO	3	2	8	13	2	8	13	2	8	13	ns
t_{PHL}¶			2	14	21	2	14	21	2	14	21	
t_{PLH}	Bn to Bn	3	4	7	11	4	7	11	4	7	11	ns
t_{PHL}			120	205	350	120	205	350	120	205	350	
t_{PLZ}	Bn to An (I/O)	4	2	5	10	2	5	10	2	5	10	ns
t_{PZL}			2	5	10	2	5	10	2	5	10	

† All typical values are measured at V_{CC} = 3.3 V and T_A = 25°C.
¶ Includes ~7.6-ns RC rise time of test-load pullup on 11-A, 1.5-kΩ pullup, and 21-pF load on 11 A has approximately 23-ns RC rise time.

PARAMETER MEASUREMENT INFORMATION
V_{TT} = 1.2 V, V_{REF} = 0.8 V FOR GTL AND V_{TT} = 1.5 V, V_{REF} = 1 V FOR GTL+

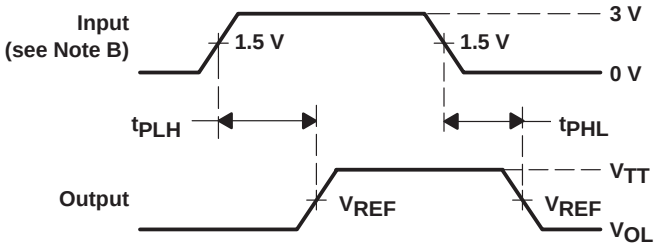


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}

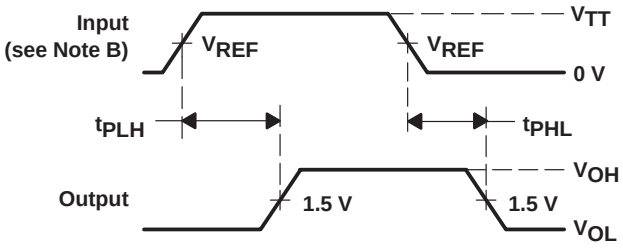


LOAD CIRCUIT FOR A OUTPUTS

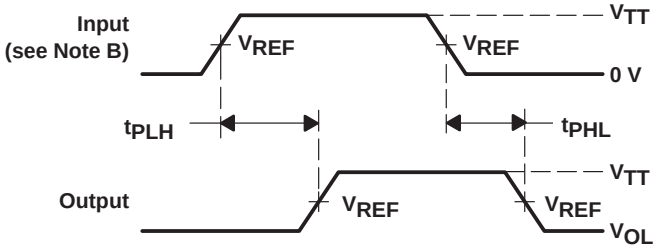
LOAD CIRCUIT FOR B OUTPUTS



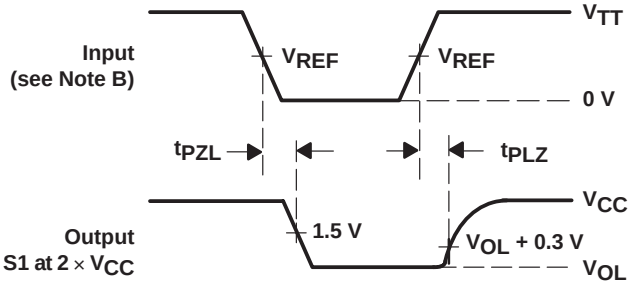
VOLTAGE WAVEFORM 1
PROPAGATION DELAY TIMES
(A port to B port)†



VOLTAGE WAVEFORM 2
PROPAGATION DELAY TIMES
(B port to A port)†



VOLTAGE WAVEFORM 3
PROPAGATION DELAY TIMES
(B port to B port)†



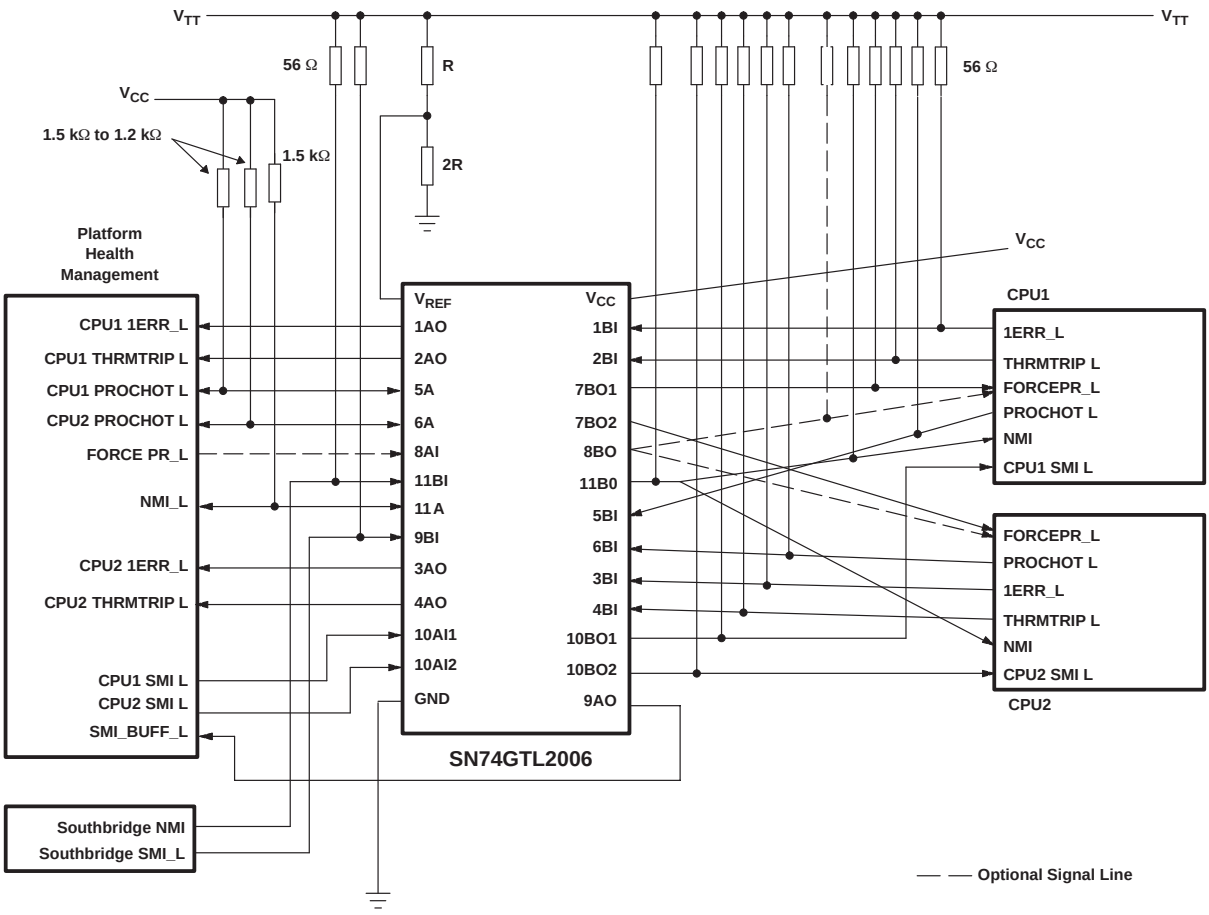
VOLTAGE WAVEFORM 4
PROPAGATION DELAY TIMES
(B port to A (I/O) port)†

† All control inputs are LVTTL levels.

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. The outputs are measured one at a time, with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

APPLICATION INFORMATION



frequently asked questions

Question 1: On SN74GTL2006 LVTTL inputs, specifically 10AI1 and 10AI2, when the device is powered down, these inputs may be pulled up to 3.3 V, and we want to ensure that there is no leakage path to the power rail under this condition. Are the LVTTL inputs high impedance when the device is powered down, and will there be any leakage?

Answer 1: When the device is powered down, the LVTTL inputs are in a high-impedance state and do not leak to V_{DD} if they are pulled high while the device is powered down.

Question 2: Do all the LVTTL inputs have the same powered-down characteristic?

Answer 2: Yes

Question 3: What is the condition of the other GTL I/O and LVTTL output pins when the device is powered down?

Answer 3: The open-drain outputs, both GTL and LVTTL, do not leak to the power supply if they are pulled high while the device is powered down. The GTL inputs also do not leak to the power supply under the same conditions. The LVTTL totem-pole outputs, however, are not open-drain type outputs, and there will be current flow on these pins if they are pulled high when V_{DD} is at ground.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74GTL2006PWR	ACTIVE	TSSOP	PW	28	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	GK2006	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

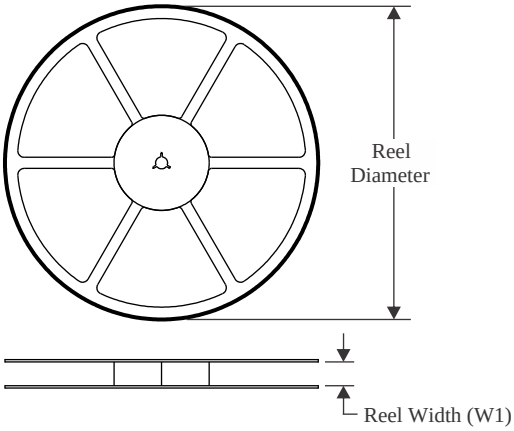
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

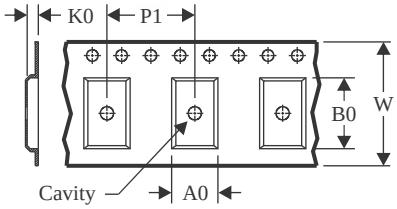
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

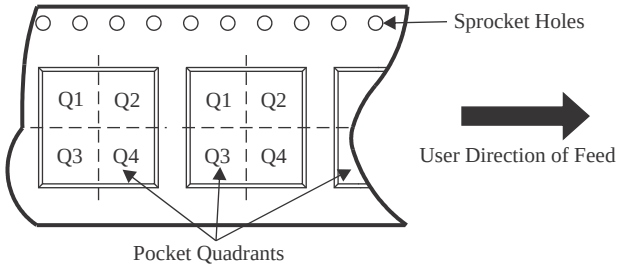


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

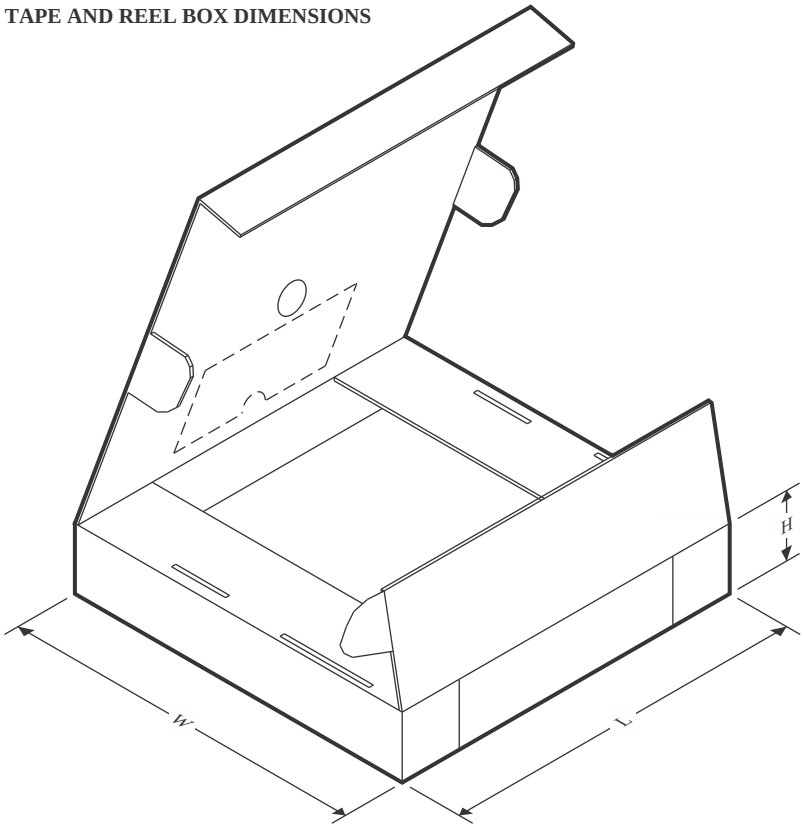
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74GTL2006PWR	TSSOP	PW	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1

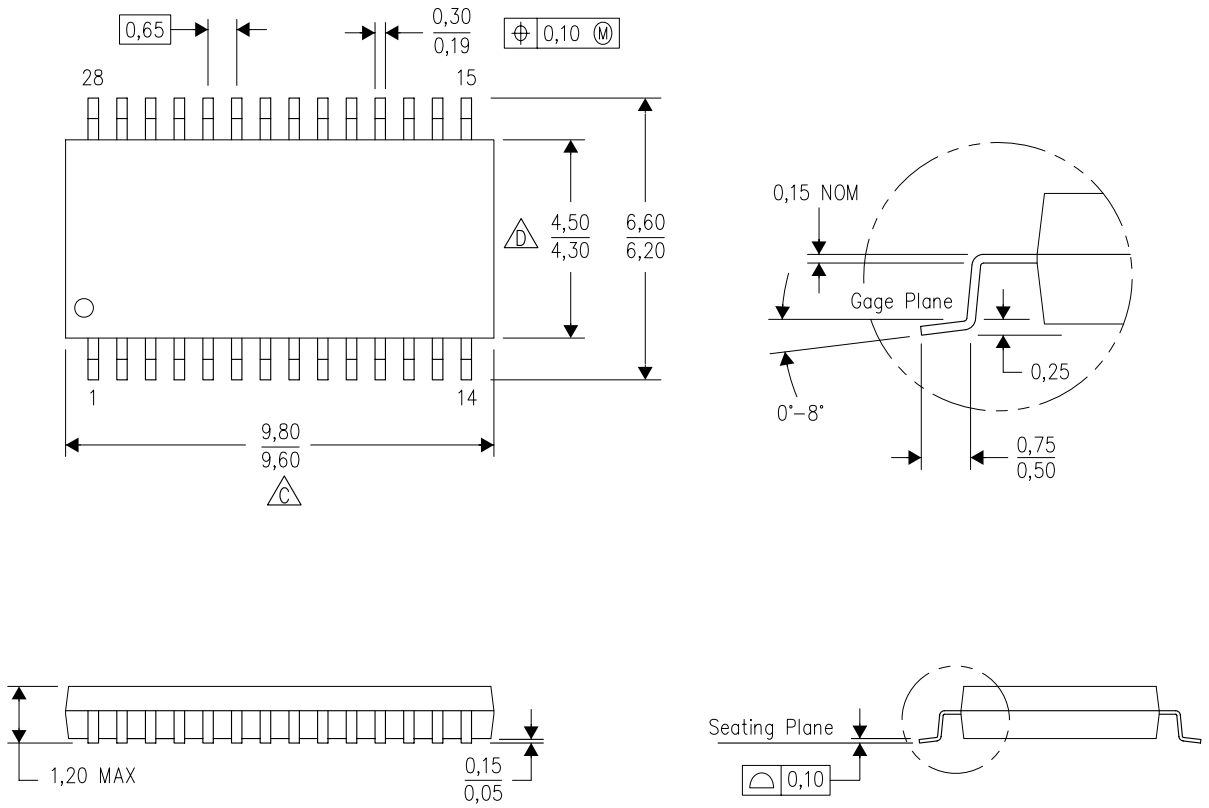
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74GTL2006PWR	TSSOP	PW	28	2000	356.0	356.0	35.0

PW (R–PDSO–G28) PLASTIC SMALL OUTLINE



4040064–7/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

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