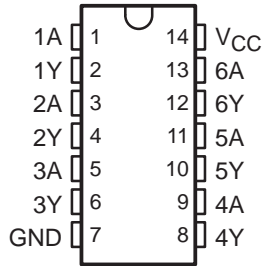


# SN54HCU04, SN74HCU04 HEX INVERTERS

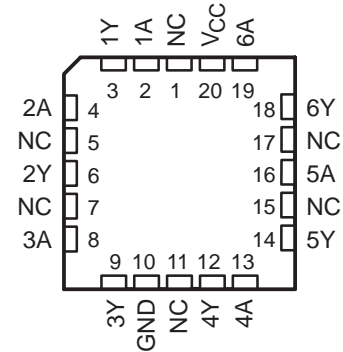
SCLS079E – MARCH 1984 – REVISED MARCH 2004

- Wide Operating Voltage Range of 2 V to 6 V
- Outputs Can Drive Up To 10 LSTTL Loads
- Low Power Consumption, 20- $\mu$ A Max  $I_{CC}$
- Typical  $t_{pd} = 7$  ns
- $\pm 4$ -mA Output Drive at 5 V
- Low Input Current of 1  $\mu$ A Max
- Unbuffered Outputs

SN54HCU04 . . . J OR W PACKAGE  
SN74HCU04 . . . D, DB, N, NS, OR PW PACKAGE  
(TOP VIEW)



SN54HCU04 . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

## description/ordering information

The 'HCU04 devices contain six independent inverters. They perform the Boolean function  $Y = \bar{A}$  in positive logic.

## ORDERING INFORMATION

TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	PDIP – N	Tube of 25	SN74HCU04N	SN74HCU04N
	SOIC – D	Tube of 50	SN74HCU04D	HCU04
		Reel of 2500	SN74HCU04DR	
		Reel of 250	SN74HCU04DT	
	SOP – NS	Reel of 2000	SN74HCU04NSR	HCU04
	SSOP – DB	Reel of 2000	SN74HCU04DBR	HU04
	TSSOP – PW	Reel of 90	SN74HCU04PW	HCU04
Reel of 2000		SN74HCU04PWR		
Reel of 250		SN74HCU04PWT		
-55°C to 125°C	CDIP – J	Tube of 25	SNJ54HCU04J	SNJ54HCU04J
	CFP – W	Tube of 150	SNJ54HCU04W	SNJ54HCU04W
	LCCC – FK	Tube of 55	SNJ54HCU04FK	SNJ54HCU04FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

# SN54HCU04, SN74HCU04 HEX INVERTERS

SCLS079E – MARCH 1984 – REVISED MARCH 2004

**FUNCTION TABLE**  
(each inverter)

INPUT A	OUTPUT Y
H	L
L	H

## logic diagram (positive logic)



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$	-0.5 V to 7 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) (see Note 1)	$\pm 20$ mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) (see Note 1)	$\pm 20$ mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	$\pm 25$ mA
Continuous current through $V_{CC}$ or GND	$\pm 50$ mA
Package thermal impedance, $\theta_{JA}$ (see Note 2):	
D package	86°C/W
DB package	96°C/W
N package	80°C/W
NS package	76°C/W
PW package	113°C/W
Storage temperature range, $T_{stg}$	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.

## recommended operating conditions (see Note 3)

		SN54HCU04			SN74HCU04			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage	2	5	6	2	5	6	V
$V_{IH}$	High-level input voltage	$V_{CC} = 2$ V	1.7		1.7			V
		$V_{CC} = 4.5$ V	3.6		3.6			
		$V_{CC} = 6$ V	4.8		4.8			
$V_{IL}$	Low-level input voltage	$V_{CC} = 2$ V		0.5		0.5		V
		$V_{CC} = 4.5$ V		1.35		1.35		
		$V_{CC} = 6$ V		1.8		1.8		
$V_I$	Input voltage	0		$V_{CC}$	0		$V_{CC}$	V
$V_O$	Output voltage	0		$V_{CC}$	0		$V_{CC}$	V
$T_A$	Operating free-air temperature	-55		125	-40		85	°C

NOTE 3: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

# SN54HCU04, SN74HCU04 HEX INVERTERS

SCLS079E – MARCH 1984 – REVISED MARCH 2004

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54HCU04		SN74HCU04		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	I <sub>OH</sub> = -20 μA	2 V	1.8			1.8		1.8	V	
			4.5 V	4			4		4		
			6 V	5.5			5.5		5.5		
		I <sub>OH</sub> = -4 mA	4.5 V	3.98			3.7		3.84		
		I <sub>OH</sub> = -5.2 mA	6 V	5.48			5.2		5.34		
V <sub>OL</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	I <sub>OL</sub> = 20 μA	2 V			0.2		0.2	0.2	V	
			4.5 V			0.5		0.5	0.5		
			6 V			0.5		0.5	0.5		
		I <sub>OL</sub> = 4 mA	4.5 V			0.26		0.4	0.33		
		I <sub>OL</sub> = 5.2 mA	6 V			0.26		0.4	0.33		
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0		6 V			±100		±1000	±1000	nA	
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0, I <sub>O</sub> = 0		6 V			2		40	20	μA	
C <sub>i</sub>			2 V to 6 V		3	10		10	10	pF	

switching characteristics over recommended operating free-air temperature range, C<sub>L</sub> = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54HCU04		SN74HCU04		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	A	Y	2 V		40	80		120		100	ns
			4.5 V		8	16		24		20	
			6 V		7	14		20		17	
t <sub>f</sub>		Y	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

operating characteristics, T<sub>A</sub> = 25°C

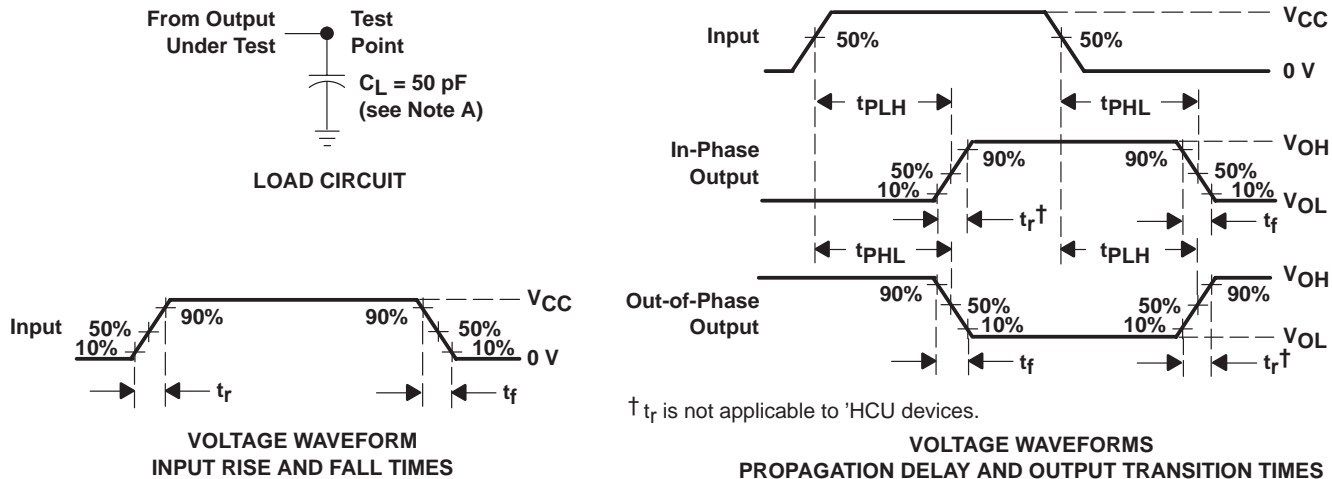
PARAMETER	TEST CONDITIONS	TYP	UNIT
C <sub>pd</sub> Power dissipation capacitance per inverter	No load	20	pF



# SN54HCU04, SN74HCU04 HEX INVERTERS

SCLS079E – MARCH 1984 – REVISED MARCH 2004

## PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A.  $C_L$  includes probe and test-fixture capacitance.
  - B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r = 6 \text{ ns}$ ,  $t_f = 6 \text{ ns}$ .
  - C. The outputs are measured one at a time, with one input transition per measurement.
  - D.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
86010012A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	86010012A SNJ54HCU 04FK	<a href="#">Samples</a>
8601001CA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8601001CA SNJ54HCU04J	<a href="#">Samples</a>
SN54HCU04J	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SN54HCU04J	<a href="#">Samples</a>
SN74HCU04D	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	-40 to 85	HCU04	
SN74HCU04DR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 85	HCU04	<a href="#">Samples</a>
SN74HCU04DT	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	-40 to 85	HCU04	
SN74HCU04N	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74HCU04N	<a href="#">Samples</a>
SN74HCU04NE4	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74HCU04N	<a href="#">Samples</a>
SN74HCU04NSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCU04	<a href="#">Samples</a>
SN74HCU04PW	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI	-40 to 85	HCU04	
SN74HCU04PWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 85	HCU04	<a href="#">Samples</a>
SN74HCU04PWRG4	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCU04	<a href="#">Samples</a>
SN74HCU04PWT	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI	-40 to 85	HCU04	
SNJ54HCU04FK	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	86010012A SNJ54HCU 04FK	<a href="#">Samples</a>
SNJ54HCU04J	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8601001CA SNJ54HCU04J	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of  $\leq 1000$ ppm threshold. Antimony trioxide based flame retardants must also meet the  $\leq 1000$ ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN54HCU04, SN74HCU04 :**

● Catalog : [SN74HCU04](#)

● Military : [SN54HCU04](#)

NOTE: Qualified Version Definitions:

● Catalog - TI's standard catalog product

● Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HCU04DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HCU04NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74HCU04PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HCU04PWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

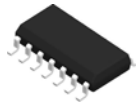
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HCU04DR	SOIC	D	14	2500	353.0	353.0	32.0
SN74HCU04NSR	SO	NS	14	2000	356.0	356.0	35.0
SN74HCU04PWR	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74HCU04PW RG4	TSSOP	PW	14	2000	356.0	356.0	35.0



**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
86010012A	FK	LCCC	20	55	506.98	12.06	2030	NA
SN74HCU04N	N	PDIP	14	25	506	13.97	11230	4.32
SN74HCU04N	N	PDIP	14	25	506	13.97	11230	4.32
SN74HCU04NE4	N	PDIP	14	25	506	13.97	11230	4.32
SN74HCU04NE4	N	PDIP	14	25	506	13.97	11230	4.32
SNJ54HCU04FK	FK	LCCC	20	55	506.98	12.06	2030	NA

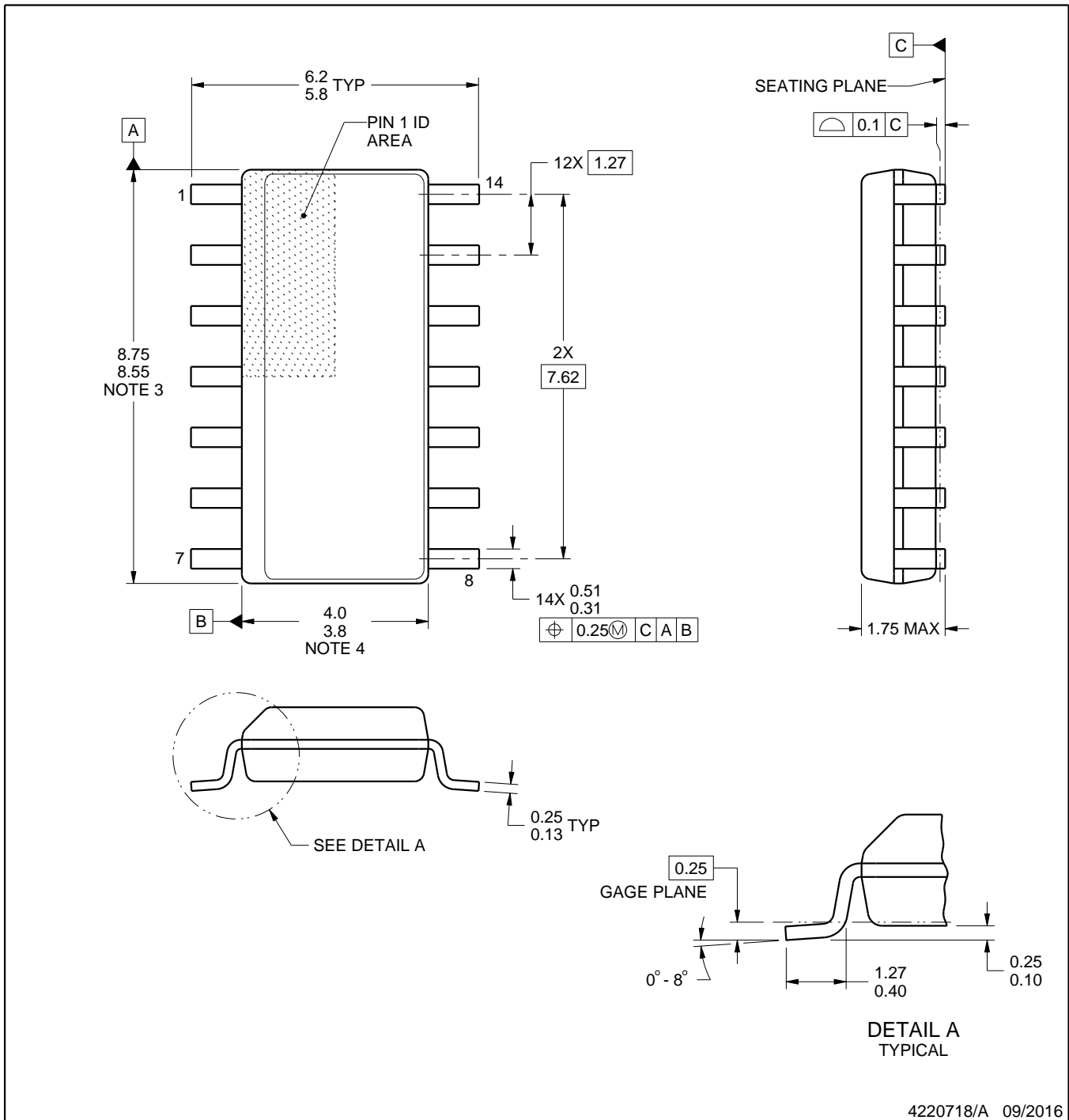


# D0014A

# PACKAGE OUTLINE

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

### NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

# EXAMPLE BOARD LAYOUT

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

## GENERIC PACKAGE VIEW

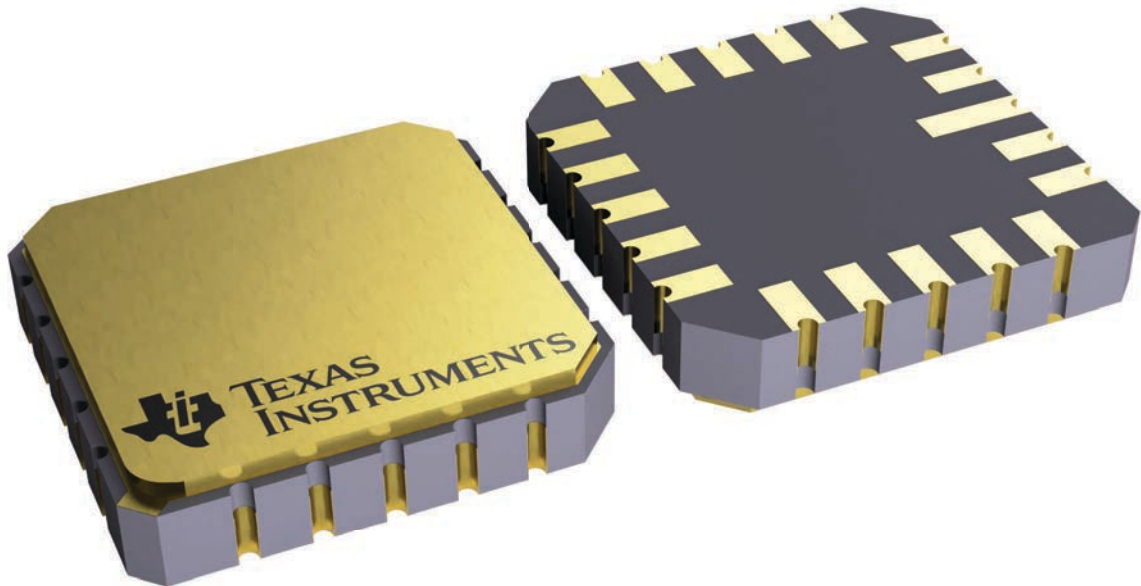
**FK 20**

**LCCC - 2.03 mm max height**

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4229370VA\

J 14

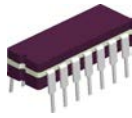
**GENERIC PACKAGE VIEW**  
**CDIP - 5.08 mm max height**  
CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4040083-5/G

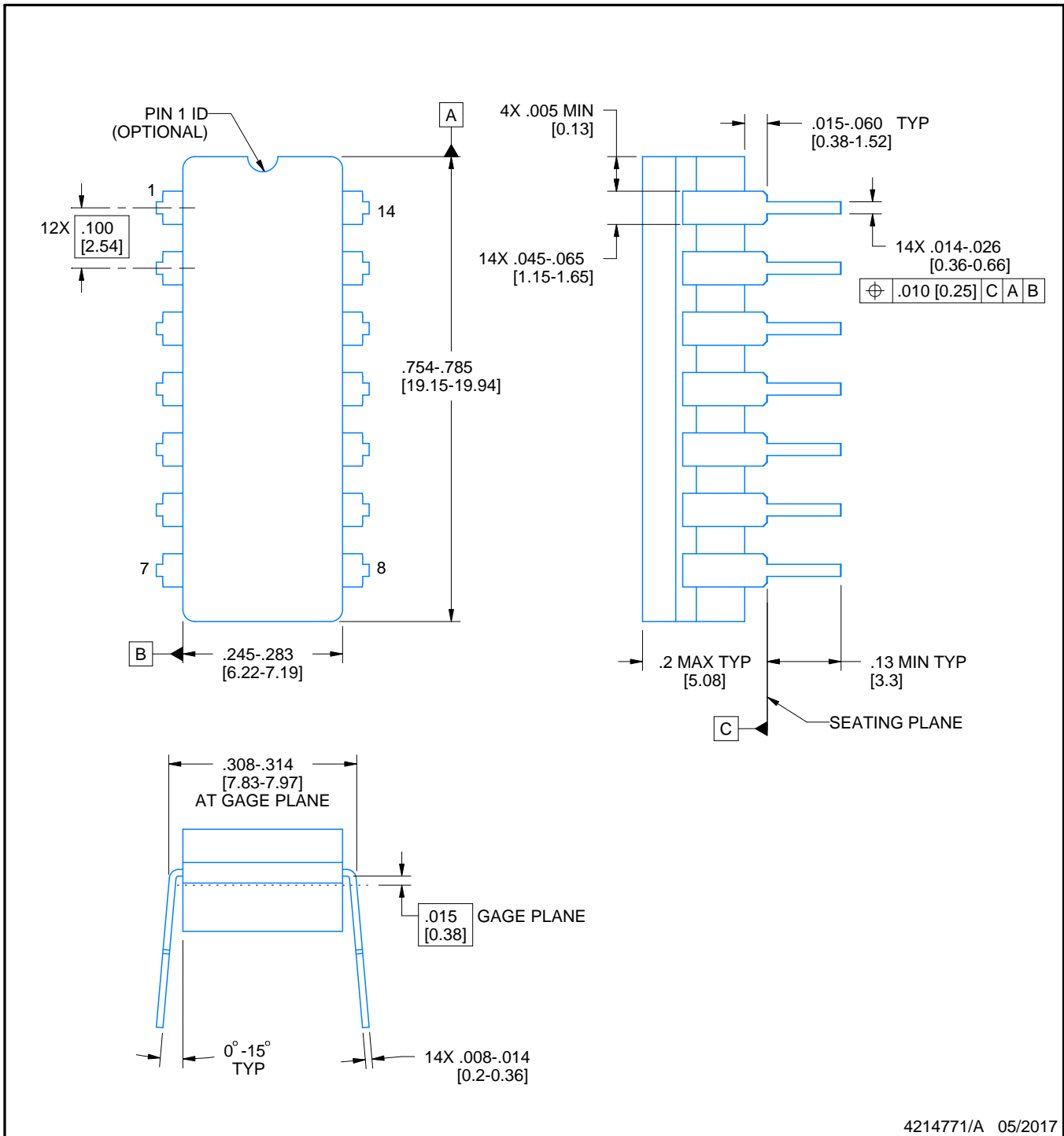
J0014A



# PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

**NOTES:**

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.



# EXAMPLE BOARD LAYOUT

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE  
NON-SOLDER MASK DEFINED  
SCALE: 5X



4214771/A 05/2017

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



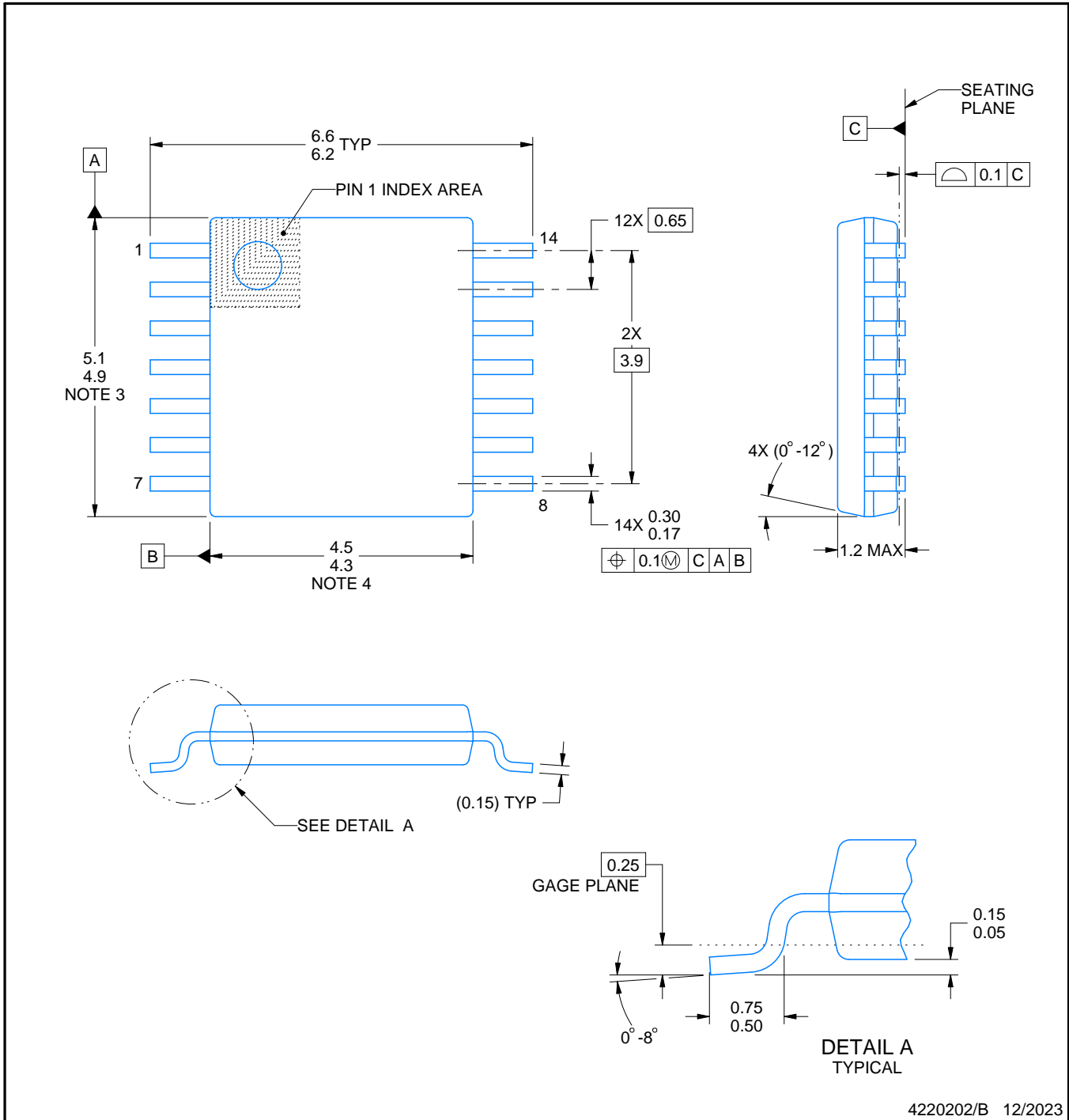
- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

PW0014A



**PACKAGE OUTLINE**  
**TSSOP - 1.2 mm max height**

SMALL OUTLINE PACKAGE



4220202/B 12/2023

NOTES:

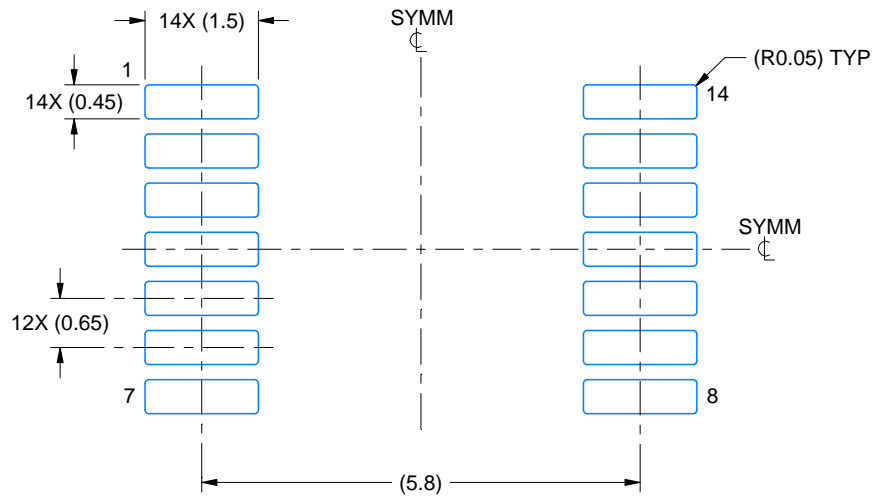
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

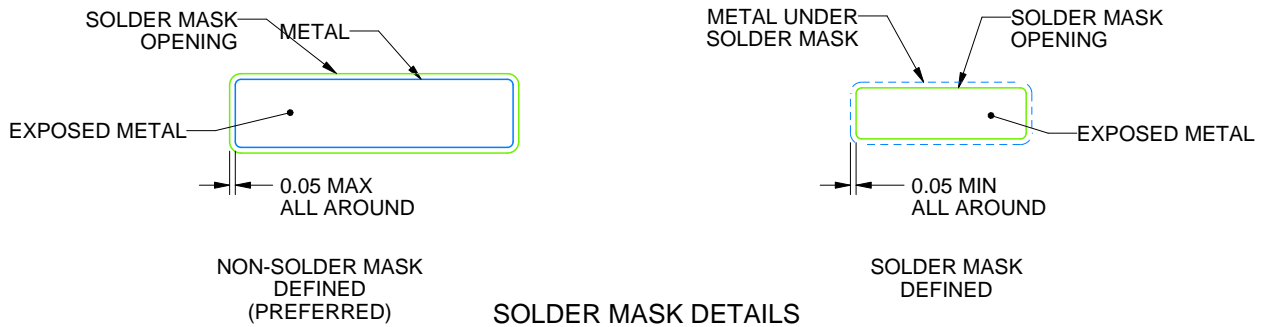
PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220202/B 12/2023

NOTES: (continued)

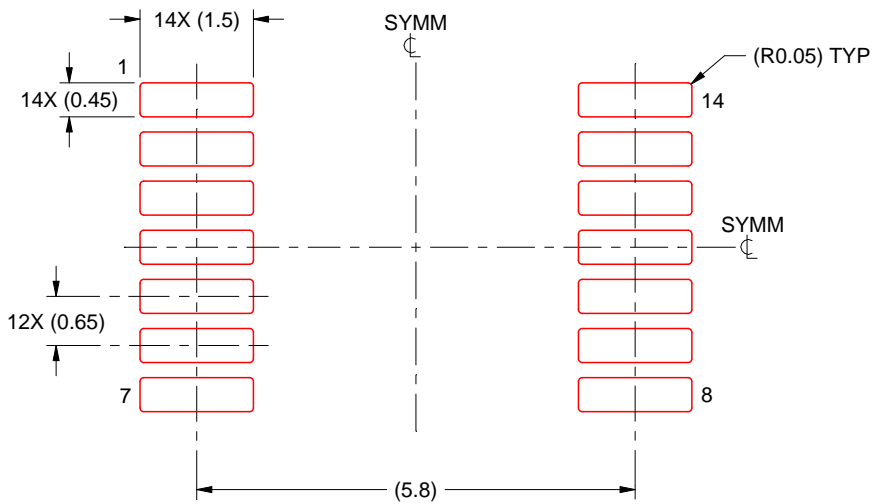
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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