

# SN54LS620, SN54LS621, SN74LS620, SN74LS621, SN74LS623 OCTAL BUS TRANSCEIVERS

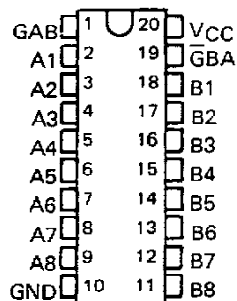
SDLS185

D2537, AUGUST 1979—REVISED MARCH 1988

- Bidirectional Bus Transceivers in High-Density 20-Pin Packages
- Local Bus-Latch Capability
- Hysteresis at Bus Inputs Improves Noise Margins
- Choice of True or Inverting Logic
- Choice of 3-State or Open-Collector Outputs

DEVICE	OUTPUT	LOGIC
'LS620	3-State	Inverting
'LS621	Open-Collector	True
'LS623	3-State	True

SN54LS620, SN54LS621,  
SN54LS622 . . . J PACKAGE  
SN74LS620, SN74LS621,  
SN74LS623 . . . DW OR N PACKAGE  
(TOP VIEW)



## description

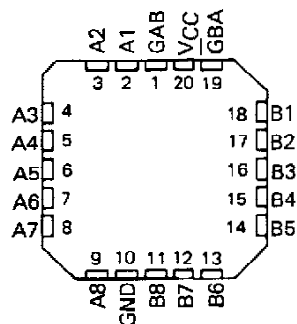
These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing.

These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic levels at the enable inputs ( $\overline{\text{GBA}}$  and GAB).

The enable inputs can be used to disable the device so that the buses are effectively isolated.

The dual-enable configuration gives the 'LS620, 'LS621, and 'LS623 the capability to store data by simultaneous enabling of  $\overline{\text{GBA}}$  and GAB. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines (16 in all) will remain at their last states. The 8-bit codes appearing on the two sets of buses will be identical for the 'LS621 and 'LS623 devices or complementary for the 'LS620.

SN54LS620, SN54LS621,  
SN54LS622 . . . FK PACKAGE  
(TOP VIEW)



FUNCTION TABLE

ENABLE INPUTS		OPERATION	
$\overline{\text{GBA}}$	GAB	'LS620	'LS621, 'LS623
L	L	B data to A bus	B data to A bus
H	H	A data to B bus	A data to B bus
H	L	Isolation	Isolation
L	H	$\overline{\text{B}}$ data to A bus, $\overline{\text{A}}$ data to B bus	B data to A bus, A data to B bus

H = high level, L = low level

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{\text{CC}}$ (see Note 1)	7 V
Input voltage	7 V
Off-state output voltage	5.5 V
Operating free-air temperature range: SN54LS'	-55°C to 125°C
SN74LS'	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

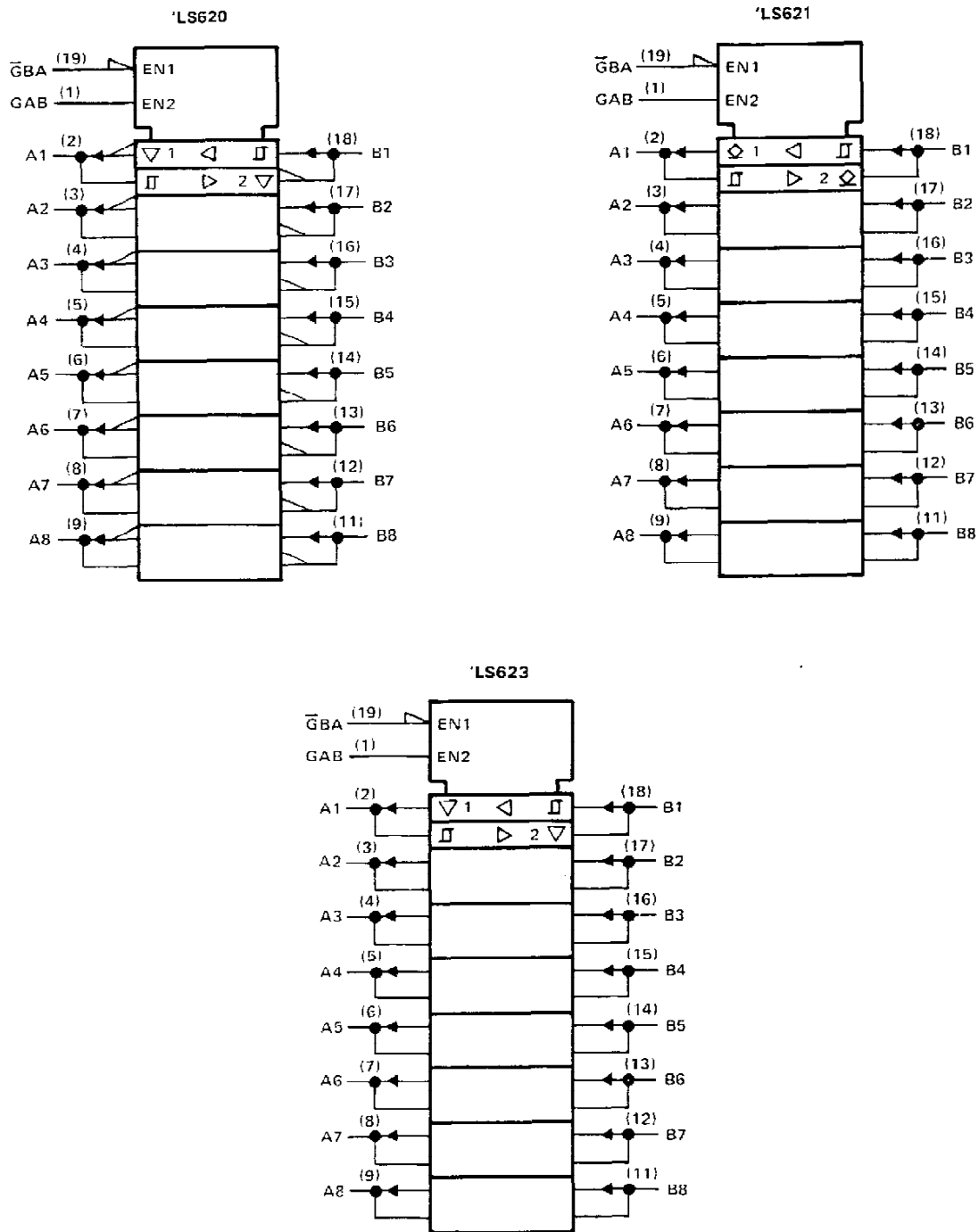
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# SN54LS620, SN54LS621, SN74LS620, SN74LS621, SN74LS623 OCTAL BUS TRANSCEIVERS

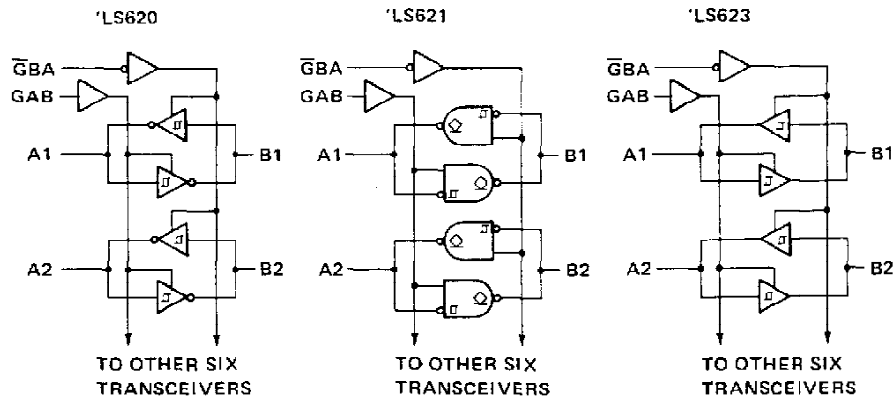
logic symbols†



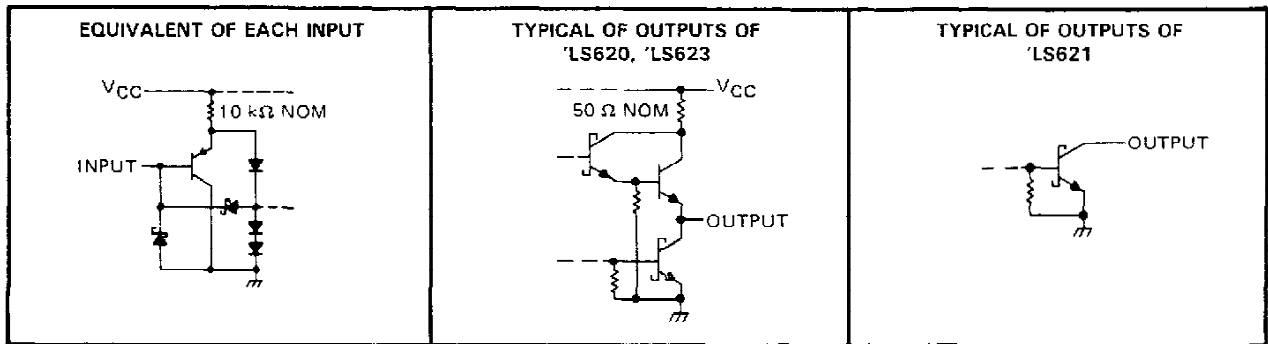
† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, J, and N packages.

**SN54LS620, SN54LS621,  
SN74LS620, SN74LS621, SN74LS623  
OCTAL BUS TRANSCEIVERS**

logic diagrams (positive logic)



schematics of inputs and outputs



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# SN54LS620, SN74LS620, SN74LS623 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

## recommended operating conditions

PARAMETER	SN54LS620			SN74LS620 SN74LS623			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, $V_{CC}$ (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
High-level output current, $I_{OH}$			-12			-15	mA
Low-level output current, $I_{OL}$			12			24	mA
Operating free-air temperature, $T_A$	-55		125	0		70	°C

NOTE 1: Voltage values are with respect to network ground terminal.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS620			SN74LS620 SN74LS623			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
$V_{IH}$ High-level input voltage							V	
$V_{IL}$ Low-level input voltage							V	
$V_{IK}$ Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5			-1.5	V
Hysteresis ( $V_{T+} - V_{T-}$ ) A or B input	$V_{CC} = \text{MIN}$	0.1	0.4		0.2	0.4		V
$V_{OH}$ High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OH} = -3 \text{ mA}$	2.4	3.4		2.4	3.4		V
	$I_{OH} = \text{MAX}$	2			2			
$V_{OL}$ Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OL} = 12 \text{ mA}$		0.25	0.4		0.25	0.4	V
	$I_{OL} = 24 \text{ mA}$					0.35	0.5	
$I_{OZH}$ Off-state output current, high-level voltage applied	$V_{CC} = \text{MAX}, V_O = 2.7 \text{ V}, \bar{G}$ at 2 V,			20			20	μA
$I_{OZL}$ Off-state output current, low-level voltage applied	$V_{CC} = \text{MAX}, V_O = 0.4 \text{ V}, \bar{G}$ at 2 V,			-400			-400	μA
$I_I$ Input current at maximum input voltage	A or B			0.1			0.1	mA
	GBA or GAB			0.1			0.1	
$I_{IH}$ High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			20			20	μA
$I_{IL}$ Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-0.4			-0.4	mA
$I_{OS}$ Short-circuit output current §	$V_{CC} = \text{MAX}$	-40		-225	-40		-225	mA
$I_{CC}$ Total supply current	Outputs high		48	70		48	70	mA
	Outputs low		62	90		62	90	
	Outputs at Hi-Z		64	95		64	95	

† For conditions shown as MIN or MAX use the appropriate value specified under recommended operating conditions.

‡ All typical values are at  $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$ .

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

## switching characteristics at $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS620			SN74LS623			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
$t_{PLH}$ Propagation delay time, low-to-high-level output	A	B	$C_L = 45 \text{ pF}, R_L = 667 \Omega,$ See Note 2	6	10		8	15	ns	
	B	A		6	10		8	15		
$t_{PHL}$ Propagation delay time, high-to-low-level output	A	B		8	15		11	15	ns	
	B	A		8	15		11	15		
$t_{PZL}$ Output enable time to low level	$\bar{G}$ BA	A	See Note 2	31	40		31	40	ns	
	GAB	B		31	40		31	40		
$t_{PZH}$ Output enable time to high level	$\bar{G}$ BA	A		23	40		26	40	ns	
	GAB	B		23	40		26	40		
$t_{PLZ}$ Output disable time from low level	$\bar{G}$ BA	A	$C_L = 5 \text{ pF}, R_L = 667 \Omega,$ See Note 2	15	25		15	25	ns	
	GAB	B		15	25		15	25		
$t_{PHZ}$ Output disable time from high level	$\bar{G}$ BA	A		15	25		15	25	ns	
	GAB	B		15	25		15	25		

$t_{PLH}$  = Propagation delay time, low-to-high-level output

$t_{PHL}$  = Propagation delay time, high-to-low-level output

$t_{PZH}$  = Output enable time to high level

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

$t_{PZL}$  = Output enable time to low level

$t_{PHZ}$  = Output disable time from high level

$t_{PLZ}$  = Output disable time from low level

  
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# SN54LS621, SN74LS621

## OCTAL BUS TRANSCEIVERS WITH OPEN-COLLECTOR OUTPUTS

### recommended operating conditions

PARAMETER	SN54LS621			SN74LS621			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, $V_{CC}$ (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, $V_{OH}$			5.5			5.5	V
Low-level output current, $I_{OL}$			12			24	mA
Operating free-air temperature, $T_A$	-55		125	0		70	°C

NOTE 1: Voltage values are with respect to network ground terminal.

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS621			SN74LS621			UNIT	
		MIN	TYP‡	MAX	MIN	TYP‡	MAX		
$V_{IH}$ High-level input voltage		2			2			V	
$V_{IL}$ Low-level input voltage				0.5			0.6	V	
$V_{IK}$ Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5			-1.5	V	
Hysteresis ( $V_{T+} - V_{T-}$ ) A or B input	$V_{CC} = \text{MIN}$	0.1	0.4		0.2	0.4		V	
$I_{OH}$ High-level output current	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, V_{OH} = 5.5 \text{ V}$			100			100	μA	
$V_{OL}$ Low-level output voltage	$V_{CC} = \text{MIN}, I_{OL} = 12 \text{ mA}$	0.25	0.4		0.25	0.4		V	
	$V_{CC} = \text{MIN}, I_{OL} = 24 \text{ mA}$				0.35	0.5			
$I_I$ Input current at maximum input voltage	A or B			0.1			0.1	mA	
	GAB or $\bar{G}BA$			0.1			0.1		
$I_{IH}$ High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			20			20	μA	
$I_{IL}$ Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-0.4			-0.4	mA	
$I_{CC}$ Total supply current	Outputs high			48	70		48	70	mA
	Outputs low			62	90		62	90	

†For conditions shown as MIN or MAX use the appropriate value specified under recommended operating conditions.

‡All typical values are at  $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ .

### switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS621			UNIT
				MIN	TYP	MAX	
$t_{PLH}$ Propagation delay time, low-to-high-level output	A	B	$C_L = 45 \text{ pF}, R_L = 667 \Omega,$ See Note 2		17	25	ns
	B	A			17	25	
$t_{PHL}$ Propagation delay time, high-to-low-level output	A	B			16	25	ns
	B	A			16	25	
$t_{PLH}$ Output disable time from low level	$\bar{G}BA$	A			23	40	ns
	GAB	B			25	40	
$t_{PHL}$ Output enable time from high level	$\bar{G}BA$	A			34	50	ns
	GAB	B			37	50	

$t_{PLH}$  = Propagation delay time, low-to-high-level output

$t_{PHL}$  = Propagation delay time, high-to-low-level output

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

  
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**TAPE AND REEL INFORMATION**



**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS623DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
SN74LS623NSR	SO	NS	20	2000	330.0	24.4	8.2	13.0	2.5	12.0	24.0	Q1

**TAPE AND REEL BOX DIMENSIONS**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS623DWR	SOIC	DW	20	2000	346.0	346.0	41.0
SN74LS623NSR	SO	NS	20	2000	346.0	346.0	41.0



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LS623N	ACTIVE	PDIP	N	20	20	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74LS623N	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74LS623N	N	PDIP	20	20	506	13.97	11230	4.32



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