SN74LV273A Octal D-Type Flip-Flops With Clear

1 Features

- Operation of 2-V to 5.5-V V_{CC}
- Maximum t_{pd} of 10.5 ns at 5 V
- Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (output V_{OH} undershoot) > 2.3 V at V_{CC} = 3.3 V, T_A = 25°C
- I_{off} supports partial-power-down mode operation
- Supports mixed-mode voltage operation on all ports
- Latch-up performance exceeds 250 mA per JESD 17

2 Applications

- Power sub-station controls
- I/O modules; analog PLC/DCS inputs
- Human machine interfaces (HMI)
- Flow meters
- Patient monitoring
- Test and measurement solutions

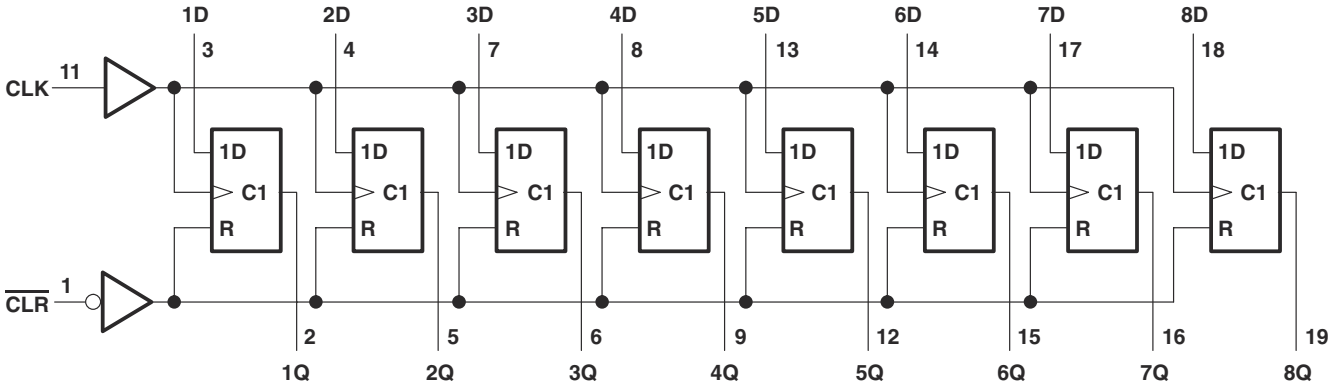
3 Description

The SN74LV273A device is an octal D-type flip-flop designed for 2-V to 5.5-V V_{CC} operation.

Package Information

PART NUMBER	PACKAGE[1]	PACKAGE SIZE[2]
SN74LV273A	DB (SSOP, 20)	7.2 mm × 7.8 mm
	DGV (TVSOP, 20)	5.00 mm × 6.4 mm
	DW (SOIC, 20)	12.80 mm × 10.3 mm
	NS (SO, 20)	12.60 mm × 5.30 mm
	PW (TSSOP, 20)	6.50 mm × 7.8 mm
	RGY (VQFN, 20)	4.5 mm × 3.50 mm
	RKS (VQFN, 20)	4.50 mm × 2.50 mm
	DGS (VSSOP, 20)	5.10 mm × 4.9 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Logic Diagram (Positive Logic)

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision N (March 2023) to Revision O (August 2023)	Page
• Deleted *ZQN* and *GQN* from *Package Information* table	1
• Updated thermal values for PW package from RθJA = 104.7 to 128.2, RθJC(top) = 38.8 to 70.5, RθJB = 55.7 to 79.3, ΨJT = 2.9 to 23.4, ΨJB = 55.1 to 78.9, all values in °C/W	6

Changes from Revision M (January 2023) to Revision N (March 2023)	Page
• Updated thermal values for DB package from RθJA = 98.7 to 128.2, RθJC(top) = 60.4 to 70.5, RθJB = 56.9 to 79.3, ΨJT = 21.6 to 23.4, ΨJB = 55.1 to 78.9, all values in °C/W	6
• Updated thermal values for DW package from RθJA = 81.8 to 102.3, RθJC(top) = 47.8 to 69.9, RθJB = 49.4 to 70.8, ΨJT = 20.1 to 46.4, ΨJB = 49.0 to 70.4, all values in °C/W	6

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5 Pin Configurations and Functions

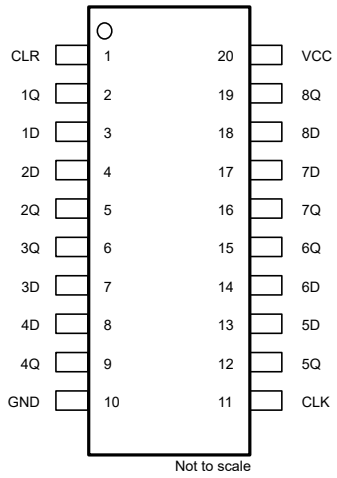

Figure 5-1. SN74LV273A DB, DGV, DW, NS, PW, or DGS Package, 20-Pin SSOP, TVSOP, SOP, TSSOP, or VSSOP (Top View)

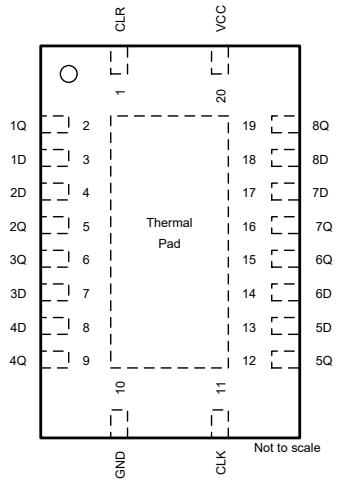

Figure 5-2. SN74LV273A RGY or RKS Package, 20-Pin VQFN (Top View)

Table 5-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
$\overline{CLR}$	1	I	Clear Pin
1Q	2	O	1Q Output
1D	3	I	1D Input
2D	4	I	2D Input
2Q	5	O	2Q Output
3Q	6	O	3Q Output
3D	7	I	3D Input
4D	8	I	4D Input
4Q	9	O	4Q Output
GND	10	—	Ground Pin
CLK	11	I	Clock Pin
5Q	12	O	5Q Output
5D	13	I	5D Input
6D	14	I	6D Input
6Q	15	O	6Q Output
7Q	16	O	7Q Output
7D	17	I	7D Input
8D	18	I	8D Input
8Q	19	O	8Q Output
V_{CC}	20	—	Power Pin
Thermal Pad		—	Thermal Pad[2]

(1) I = input, O = output
(2) RKS package only

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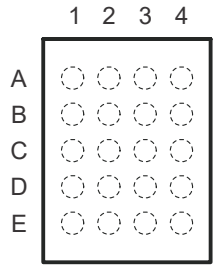

Figure 5-3. GQN or ZQN Package, 20-Pin BGA (Top View)

Table 5-2. GQN or ZQN Pin Assignments

	1	2	3	4
A	1Q	$\overline{CLR}$	V_{CC}	8Q
B	2D	7D	1D	8D
C	3Q	2Q	6Q	7Q
D	4D	5D	3D	6D
E	GND	4Q	CLK	5Q

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	7	V
V_I	Input voltage range(2)		–0.5	7	V
V_O	Voltage range applied to any output in the high-impedance or power-off state(2)		–0.5	7	V
V_O	Output voltage range(2) (3)		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0		–20	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current	V_O = 0 to V_{CC}		±25	mA
	Continuous current through V_{CC} or GND			±50	mA
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) This value is limited to 5.5 V maximum.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±3000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2)	±2000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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6.3 Recommended Operating Conditions

(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		V
		V_{CC} = 2.3 V to 2.7 V	V_{CC} × 0.7		
		V_{CC} = 3 V to 3.6 V	V_{CC} × 0.7		
		V_{CC} = 4.5 V to 5.5 V	V_{CC} × 0.7		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5	V
		V_{CC} = 2.3 V to 2.7 V		V_{CC} × 0.3	
		V_{CC} = 3 V to 3.6 V		V_{CC} × 0.3	
		V_{CC} = 4.5 V to 5.5 V		V_{CC} × 0.3	
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		–50	μA
		V_{CC} = 2.3 V to 2.7 V		–2	mA
		V_{CC} = 3 V to 3.6 V		–6	
		V_{CC} = 4.5 V to 5.5 V		–12	
I_{OL}	Low-level output current	V_{CC} = 2 V		50	μA
		V_{CC} = 2.3 V to 2.7 V		2	mA
		V_{CC} = 3 V to 3.6 V		6	
		V_{CC} = 4.5 V to 5.5 V		12	
Δt/Δv	Input transition rise or fall rate	V_{CC} = 2.3 V to 2.7 V		200	ns/V
		V_{CC} = 3 V to 3.6 V		100	
		V_{CC} = 4.5 V to 5.5 V		20	
T_A	Operating free-air temperature		–40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs (SCBA004).

6.4 Thermal Information

THERMAL METRIC(1)		SN74LV273A								UNIT
		DB	DGV	DW	NS	PW	RGY	RKS	DGS	
		20 PINS								
$R_{\theta JA}$	Junction-to-ambient thermal resistance	118.2	118.1	102.3	79.4	128.2	37.1	75.2	125.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	77.2	33.4	69.9	45.9	70.5	46.1	79.4	80.0	
$R_{\theta JB}$	Junction-to-board thermal resistance	73	59.6	70.8	46.9	79.3	14.9	47.8	63.8	
ψ_{JT}	Junction-to-top characterization parameter	42.2	1.1	46.4	19.1	23.4	1.3	14.6	8.4	
ψ_{JB}	Junction-to-board characterization parameter	72.6	58.9	70.4	46.5	78.9	15.0	47.8	79.9	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	N/A	9.8	31.5	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

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6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			–40°C to 85°C		–40°C to 125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = –50 µA	2 V to 5.5 V	V_{CC} – 0.1			V_{CC} – 0.1		V_{CC} – 0.1		V
	I_{OH} = –2 mA	2.3 V	2			2		2		
	I_{OH} = –6 mA	3 V	2.48			2.48		2.48		
	I_{OH} = –12 mA	4.5 V	3.8			3.8		3.8		
V_{OL}	I_{OL} = –50 µA	2 V to 5.5 V			0.1		0.1		0.1	V
	I_{OL} = –2 mA	2.3 V			0.4		0.4		0.4	
	I_{OL} = –6 mA	3 V			0.44		0.44		0.44	
	I_{OL} = –12 mA	4.5 V			0.55		0.55		0.55	
I_I	V_I = 5.5 V or GND	0 to 5.5 V			±1		±1		±1	µA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			20		20		20	µA
I_{off}	V_I or V_O = 0 to 5.5 V	0 V			5		5		5	µA
C_i	V_I = V_{CC} or GND	3.3 V		2						pF

6.6 Timing Requirements, V_{CC} = 2.5 V ± 0.2 V

over recommended operating free-air temperature range (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

			T_A = 25°C		–40°C to 85°C		–40°C to 125°C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	$\overline{CLR}$ low	6.5		7		7.5		ns
		CLK high or low	7		8.5		9		
t_{su}	Setup time, data before CLK↑	Data	8.5		10.5		12		ns
		$\overline{CLR}$ inactive	4		4		4.5		
t_h	Hold time, data after CLK↑		0.5		1		2.5		ns

6.7 Timing Requirements, V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

			T_A = 25°C		–40°C to 85°C		–40°C to 125°C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	$\overline{CLR}$ low	5		6		6.5		ns
		CLK high or low	5		6.5		7		
t_{su}	Setup time, data before CLK↑	Data	5.5		6.5		8		ns
		$\overline{CLR}$ inactive	2.5		2.5		3		
t_h	Hold time, data after CLK↑		1		1		2.5		ns

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6.8 Timing Requirements, V_{CC} = 5 V ± 0.5 V

over recommended operating free-air temperature range (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

			T_A = 25°C		–40°C to 85°C		–40°C to 125°C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	$\overline{CLR}$ low	5		5		5.5		ns
		CLK high or low	5		5		5.5		
t_{su}	Setup time, data before CLK↑	Data	4.5		4.5		6		ns
		$\overline{CLR}$ inactive	2		2		2.5		
t_h	Hold time, data after CLK↑		1		1		2		ns

6.9 Switching Characteristics, V_{CC} = 2.5 V ± 0.2 V

over recommended operating free-air temperature range (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			–40°C to 85°C		–40°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			C_L = 15 pF	55	95		45		45		MHz
			C_L = 50 pF	45	75		40		40		
t_{pd}	CLK	Q	C_L = 15 pF		10.4	18.3	1	20.5	1	22.5	ns
t_{PHL}	$\overline{CLR}$	Q			10.3	19	1	21	1	23	ns
t_{pd}	CLK	Q	C_L = 50 pF		12.9	22.1	1	25	1	27	ns
t_{PHL}	$\overline{CLR}$	Q			13.1	22.8	1	25.5	1	27.5	ns
$t_{sk(o)}$						2				2	ns

6.10 Switching Characteristics, V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			–40°C to 85°C		–40°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			C_L = 15 pF	75	140		65		65		MHz
			C_L = 50 pF	50	110		45		45		
t_{pd}	CLK	Q	C_L = 15 pF		7.1	13.6	1	16	1	17.5	ns
t_{PHL}	$\overline{CLR}$	Q			6.9	13.6	1	16	1	17.5	ns
t_{pd}	CLK	Q	C_L = 50 pF		9.1	17.1	1	19.5	1	21	ns
t_{PHL}	$\overline{CLR}$	Q			8.7	17.1	1	19.5	1	21	ns
$t_{sk(o)}$						1.5				1.5	ns

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6.11 Switching Characteristics, V_{CC} = 5 V ± 0.5 V

over recommended operating free-air temperature range (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			–40°C to 85°C		–40°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			C_L = 15 pF	120	205		100		100		MHz
			C_L = 50 pF	80	160		70		70		
t_{pd}	CLK	Q	C_L = 15 pF		4.8	9	1	10.5	1	11.5	ns
t_{PHL}	$\overline{CLR}$	Q			4.7	8.5	1	10	1	11	ns
t_{pd}	CLK	Q	C_L = 50 pF		6.2	11	1	12.5	1	14	ns
t_{PHL}	$\overline{CLR}$	Q			6	10.5	1	12	1	13.5	ns
$t_{sk(o)}$						1				1	ns

6.12 Noise Characteristics

V_{CC} = 3.3 V, C_L = 50 pF, T_A = 25°C

PARAMETER		SN74LV273A			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.4	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		–0.4	–0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		2.9		V
$V_{IH(D)}$	High-level dynamic input voltage	2.31			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.99	V

6.13 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS		V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF,	f = 10 MHz	3.3 V	15.9	pF
				5 V	17.1	

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6.14 Typical Characteristics

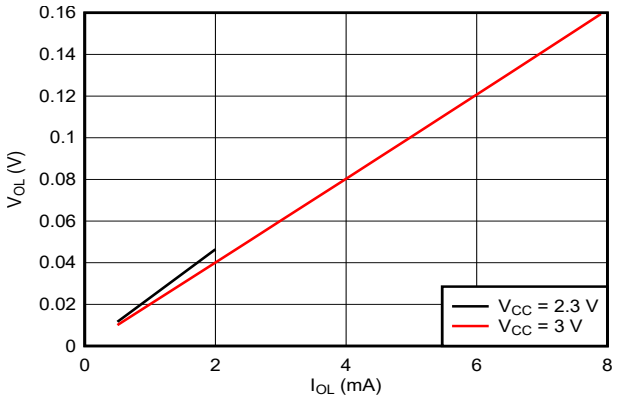

Figure 6-1. Output Voltage in LOW state, 2.3- and 3-V Supply

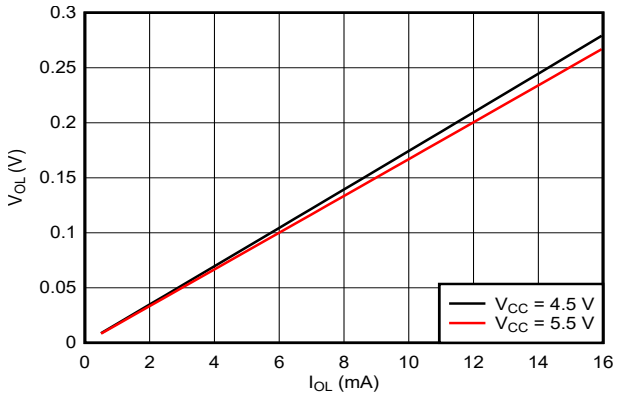

Figure 6-2. Output Voltage in LOW state, 4.5- and 5.5-V Supply

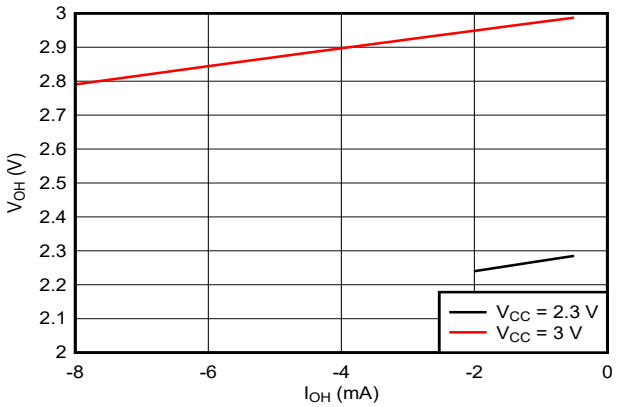

Figure 6-3. Output Voltage in HIGH state, 2.3- and 3-V Supply

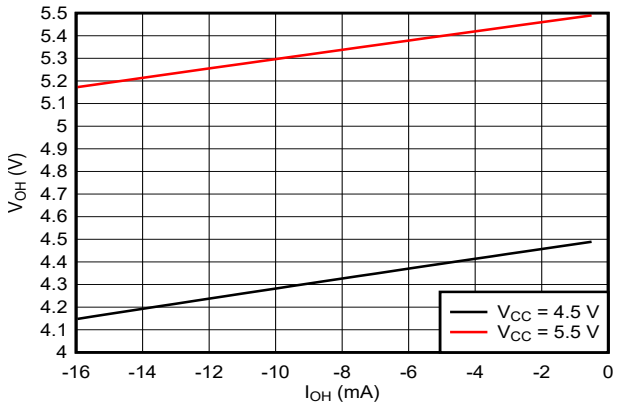

Figure 6-4. Output Voltage in HIGH state, 4.5- and 5.5-V Supply

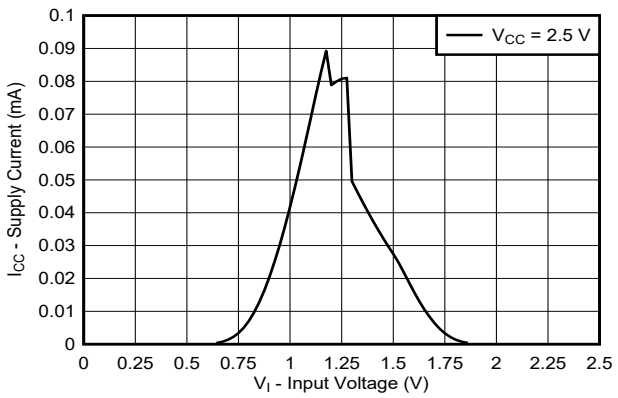

Figure 6-5. Supply Current across Input Voltage, 2.5-V Supply

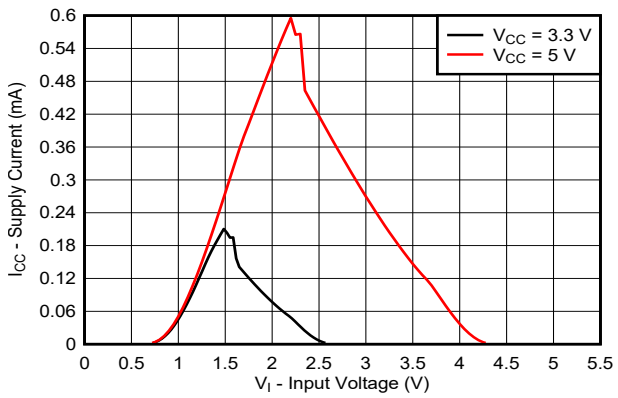

Figure 6-6. Supply Current across Input Voltage, 3.3- and 5-V Supply

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6.14 Typical Characteristics (continued)

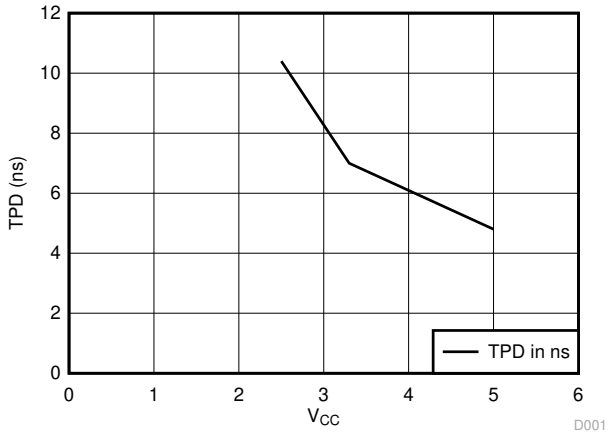

Figure 6-7. TPD vs V_{CC} at 25°C

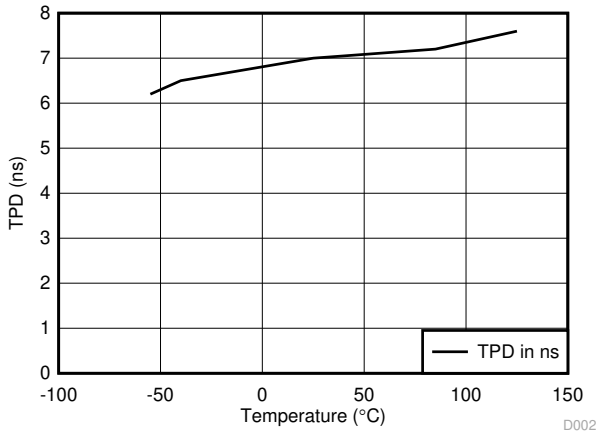

Figure 6-8. TPD vs Temperature

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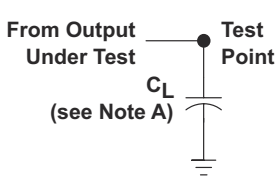
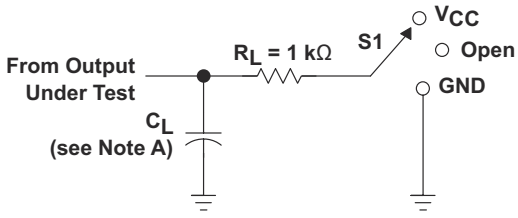
7 Parameter Measurement Information

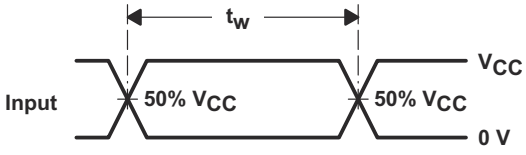


LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

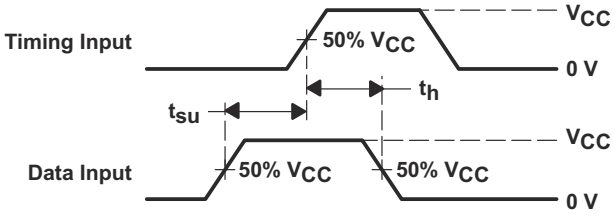


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}

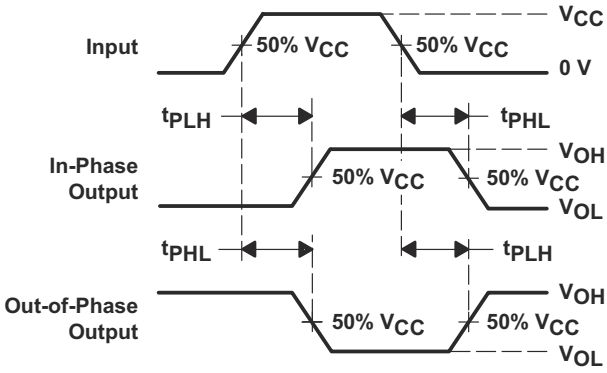
LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS



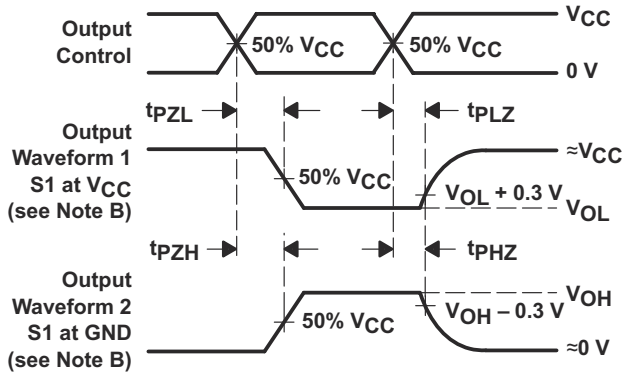
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.
D. The outputs are measured one at a time, with one input transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PHL} and t_{PLH} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 7-1. Load Circuit and Voltage Waveforms

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8 Detailed Description

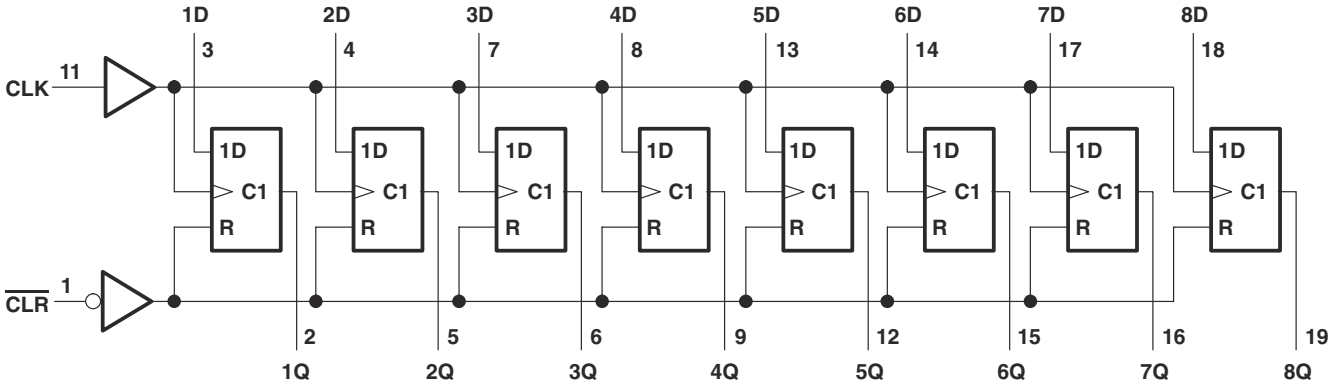
8.1 Overview

The SN74LV273A device is an octal D-type flip-flop designed for 2-V to 5.5-V V_{CC} operation.

This device is a positive-edge-triggered flip-flop with direct clear ($\overline{CLR}$) input. Information at the data (D) inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock (CLK) input is at either the high or low level, the D-input signal has no effect at the output.

The SN74LV273A device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Balanced CMOS Push-Pull Outputs

This device includes balanced CMOS push-pull outputs. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

Unused push-pull CMOS outputs should be left disconnected.

8.3.2 Latching Logic

This device includes latching logic circuitry. Latching circuits commonly include D-type latches and D-type flip-flops, but include all logic circuits that act as volatile memory.

When the device is powered on, the state of each latch is unknown. There is no default state for each latch at start-up.

The output state of each latching logic circuit only remains stable as long as power is applied to the device within the supply voltage range specified in the *Recommended Operating Conditions* table.

8.3.3 Partial Power Down (I_{off})

This device includes circuitry to disable all outputs when the supply pin is held at 0 V. When disabled, the outputs will neither source nor sink current, regardless of the input voltages applied. The amount of leakage current at each output is defined by the I_{off} specification in the *Electrical Characteristics* table.

8.3.4 Clamp Diode Structure

Figure 8-1 shows the inputs and outputs to this device have negative clamping diodes only.

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CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

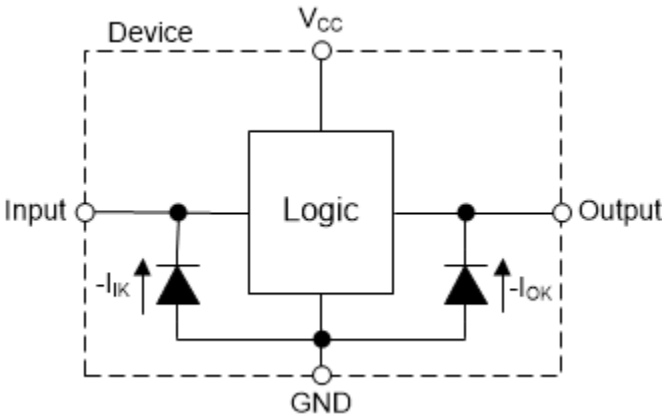

Figure 8-1. Electrical Placement of Clamping Diodes for Each Input and Output

8.4 Device Functional Modes

Table 8-1. Function Table (Each Flip-Flop)

INPUTS			OUTPUT Q
$\overline{CLR}$	CLK	D	
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

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9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The SN74LV273A is a low-drive CMOS device that can be used for a multitude of bus interface type applications where the data needs to be retained or latched. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. The inputs are tolerant to 5.5 V at any valid V_{CC}. This feature makes it Ideal for translating down to the V_{CC} level. Figure 9-2 shows the reduction in ringing compared to higher drive parts such as AC.

9.2 Typical Application

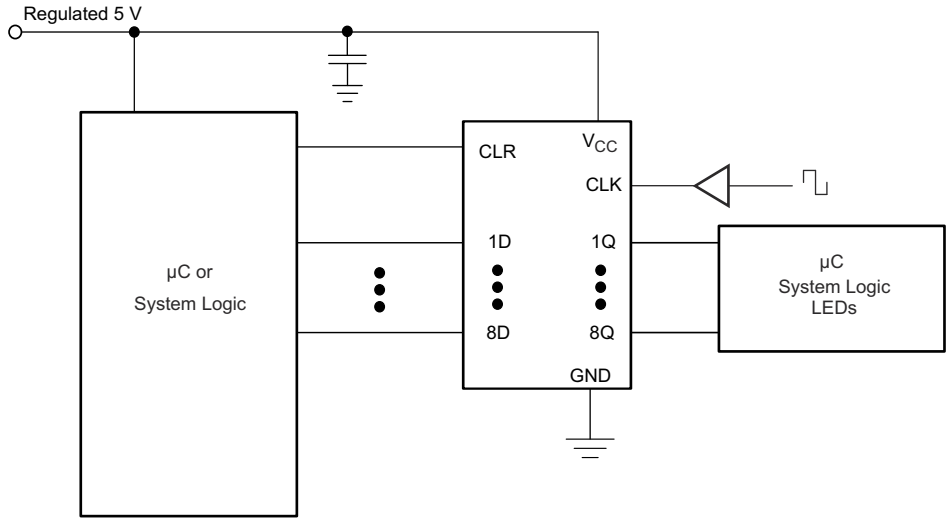

Figure 9-1. Typical Application Schematic

9.2.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the device's electrical characteristics as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74LV273A plus the maximum static supply current, I_{CC}, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only source as much current that is provided by the positive supply source. Be sure to not exceed the maximum total current through V_{CC} listed in the *Absolute Maximum Ratings*.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74LV273A plus the maximum supply current, I_{CC}, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into its ground connection. Be sure to not exceed the maximum total current through GND listed in the *Absolute Maximum Ratings*.

The SN74LV273A can drive a load with a total capacitance less than or equal to 50 pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, it is not recommended to exceed 50 pF.

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The SN74LV273A can drive a load with total resistance described by $R_L \geq V_O / I_O$, with the output voltage and current defined in the *Electrical Characteristics* table with V_{OH} and V_{OL}. When outputting in the HIGH state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the V_{CC} pin.

Total power consumption can be calculated using the information provided in *CMOS Power Consumption and Cpd Calculation*.

Thermal increase can be calculated using the information provided in *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices*.

CAUTION

The maximum junction temperature, $T_{J(max)}$ listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

9.2.2 Input Considerations

Input signals must cross $V_{IL(max)}$ to be considered a logic LOW, and $V_{IH(min)}$ to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either V_{CC} or ground. The unused inputs can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input will be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The drive current of the controller, leakage current into the SN74LV273A (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10-kΩ resistor value is often used due to these factors.

The SN74LV273A has CMOS inputs and thus requires fast input transitions to operate correctly, as defined in the *Recommended Operating Conditions* table. Slow input transitions can cause oscillations, additional power consumption, and reduction in device reliability.

Refer to the *Feature Description* section for additional information regarding the inputs for this device.

9.2.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the V_{OH} specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the V_{OL} specification in the *Electrical Characteristics*.

Push-pull outputs that could be in opposite states, even for a very short time period, should never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to V_{CC} or ground.

Refer to the *Feature Description* section for additional information regarding the outputs for this device.

9.2.4 Detailed Design Procedure

1. Add a decoupling capacitor from V_{CC} to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V_{CC} and GND pins. An example layout is shown in the *Layout* section.
2. Ensure the capacitive load at the output is ≤ 50 pF. This is not a hard limit; by design, however, it will optimize performance. This can be accomplished by providing short, appropriately sized traces from the SN74LV273A to one or more of the receiving devices.
3. Ensure the resistive load at the output is larger than ($V_{CC} / I_{O(max)}$) Ω. Doing this will prevent the maximum output current from the *Absolute Maximum Ratings* from being violated. Most CMOS inputs have a resistive load measured in MΩ; much larger than the minimum calculated previously.

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4. Thermal issues are rarely a concern for logic gates; the power consumption and thermal increase, however, can be calculated using the steps provided in the application report, *CMOS Power Consumption and Cpd Calculation*.

9.2.5 Application Curves

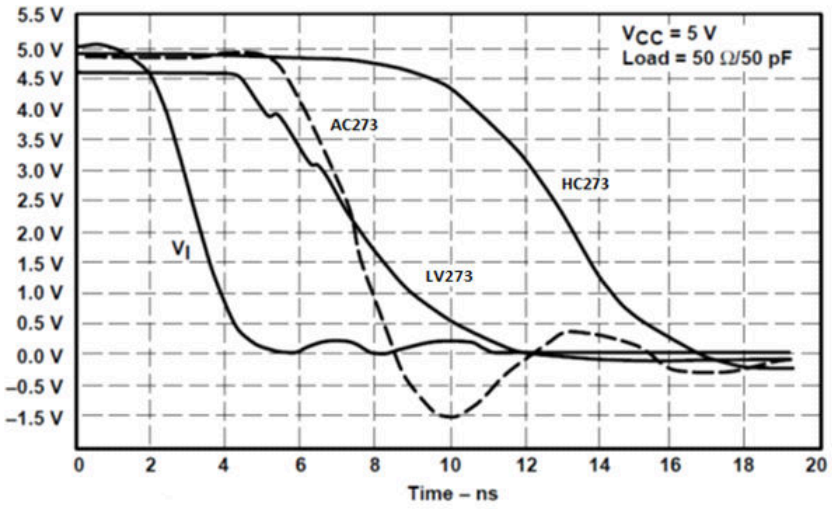

Figure 9-2. Switching Characteristics Comparison

9.3 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the *Recommended Operating Conditions* table.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 µF is recommended. If there are multiple V_{CC} pins, 0.01 µF or 0.022 µF is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 µF and 1 µF are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

9.4 Layout

9.4.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in Figure 9-3 are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC}, whichever makes more sense or is more convenient. It is acceptable to float outputs unless the part is a transceiver.

9.4.2 Layout Example

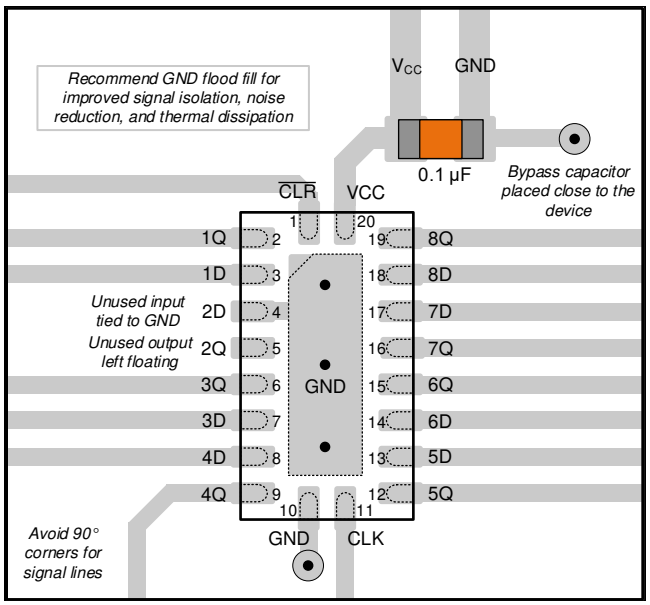

Figure 9-3. Layout Example for SN74LV273A in the RKS Package

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10 Device and Documentation Support

10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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10.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LV273ADBR	Active	Production	SSOP (DB) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV273A
SN74LV273ADBR.A	Active	Production	SSOP (DB) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV273A
SN74LV273ADBRE4	Active	Production	SSOP (DB) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV273A
SN74LV273ADBRG4	Active	Production	SSOP (DB) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV273A
SN74LV273ADGSR	Active	Production	VSSOP (DGS) | 20	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L273A
SN74LV273ADGSR.A	Active	Production	VSSOP (DGS) | 20	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L273A
SN74LV273ADGVR	Active	Production	TVSOP (DGV) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV273A
SN74LV273ADGVR.A	Active	Production	TVSOP (DGV) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV273A
SN74LV273ADW	Obsolete	Production	SOIC (DW) | 20	-	-	Call TI	Call TI	-40 to 125	LV273A
SN74LV273ADWR	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV273A
SN74LV273ADWR.A	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV273A
SN74LV273ANSR	Active	Production	SOP (NS) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	74LV273A
SN74LV273ANSR.A	Active	Production	SOP (NS) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	74LV273A
SN74LV273APW	Obsolete	Production	TSSOP (PW) | 20	-	-	Call TI	Call TI	-40 to 125	LV273A
SN74LV273APWR	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV273A
SN74LV273APWR.A	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV273A
SN74LV273APWRE4	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV273A
SN74LV273APWRG4	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV273A
SN74LV273APWRG4.A	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV273A
SN74LV273ARGYR	Active	Production	VQFN (RGY) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LV273A
SN74LV273ARGYR.A	Active	Production	VQFN (RGY) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LV273A
SN74LV273ARKSR	Active	Production	VQFN (RKS) | 20	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LV273A
SN74LV273ARKSR.A	Active	Production	VQFN (RKS) | 20	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LV273A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LV273A :

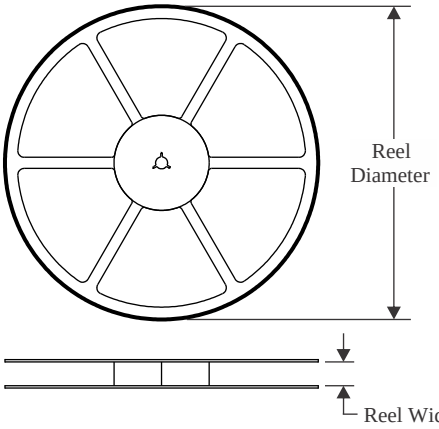
- Automotive : SN74LV273A-Q1

NOTE: Qualified Version Definitions:

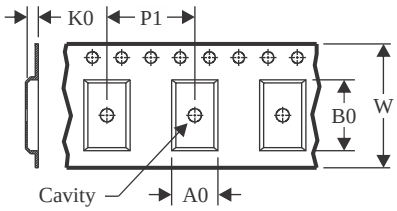
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

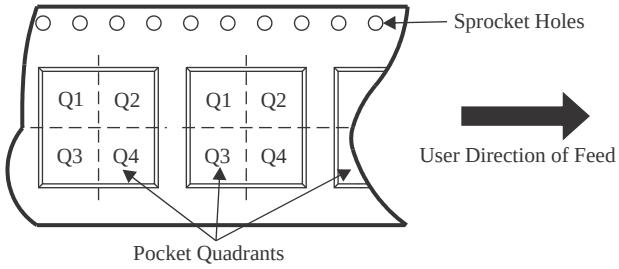


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

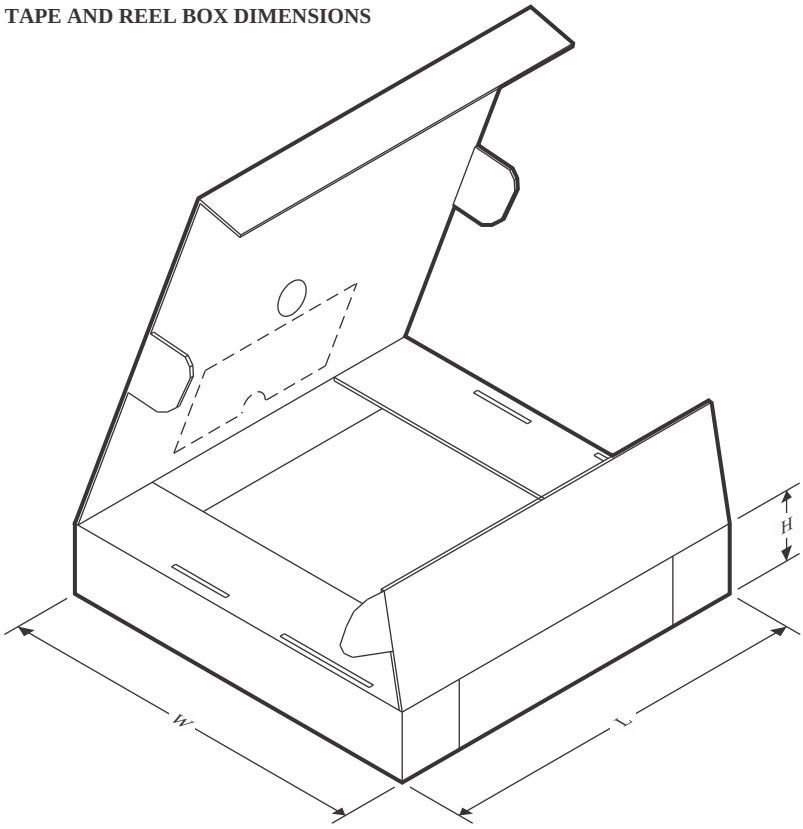
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV273ADBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74LV273ADGSR	VSSOP	DGS	20	5000	330.0	16.4	5.4	5.4	1.45	8.0	16.0	Q1
SN74LV273ADGVR	TVSOP	DGV	20	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV273ADWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74LV273ADWR	SOIC	DW	20	2000	330.0	24.4	10.9	13.3	2.7	12.0	24.0	Q1
SN74LV273ANSR	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74LV273APWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74LV273APWRG4	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74LV273APWRG4	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74LV273ARGYR	VQFN	RGY	20	3000	330.0	12.4	3.71	4.71	1.1	8.0	12.0	Q1
SN74LV273ARKSR	VQFN	RKS	20	3000	180.0	12.4	2.8	4.8	1.2	4.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

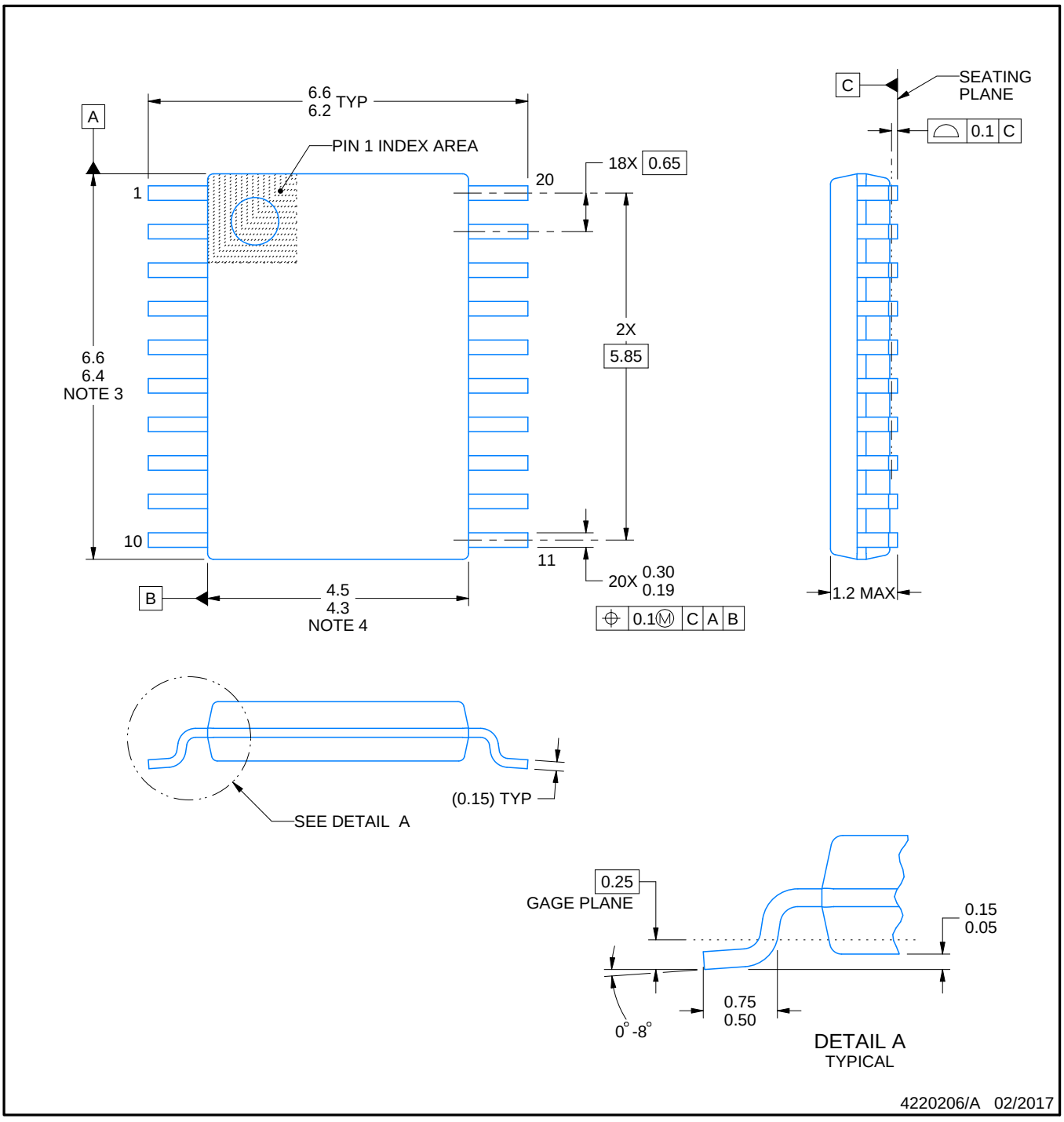
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV273ADBR	SSOP	DB	20	2000	353.0	353.0	32.0
SN74LV273ADGSR	VSSOP	DGS	20	5000	353.0	353.0	32.0
SN74LV273ADGVR	TVSOP	DGV	20	2000	353.0	353.0	32.0
SN74LV273ADWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74LV273ADWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74LV273ANSR	SOP	NS	20	2000	356.0	356.0	45.0
SN74LV273APWR	TSSOP	PW	20	2000	353.0	353.0	32.0
SN74LV273APWRG4	TSSOP	PW	20	2000	353.0	353.0	32.0
SN74LV273APWRG4	TSSOP	PW	20	2000	353.0	353.0	32.0
SN74LV273ARGYR	VQFN	RGY	20	3000	353.0	353.0	32.0
SN74LV273ARKSR	VQFN	RKS	20	3000	210.0	185.0	35.0

PACKAGE OUTLINE

PW0020A

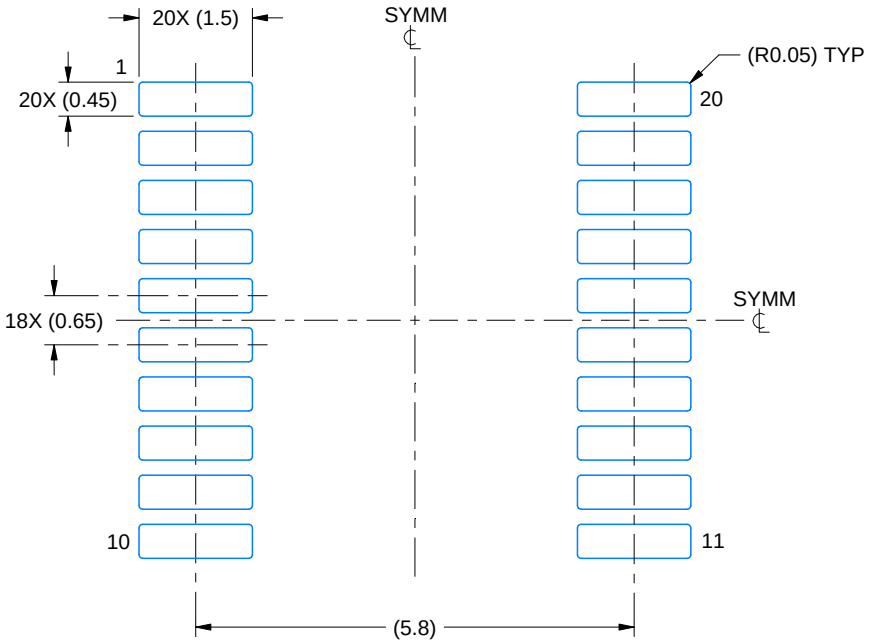
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

NON-SOLDER MASK DEFINED (PREFERRED)

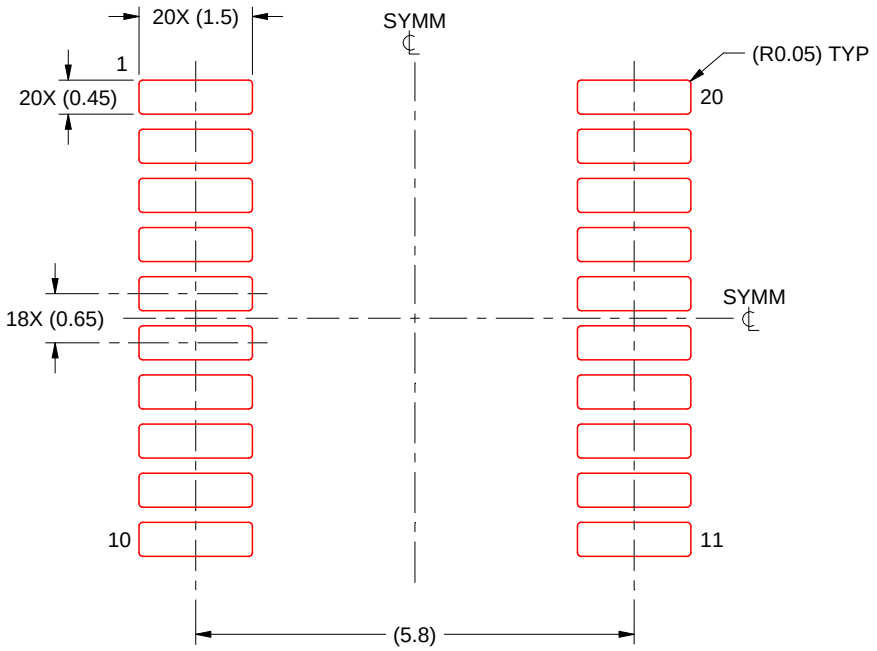
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

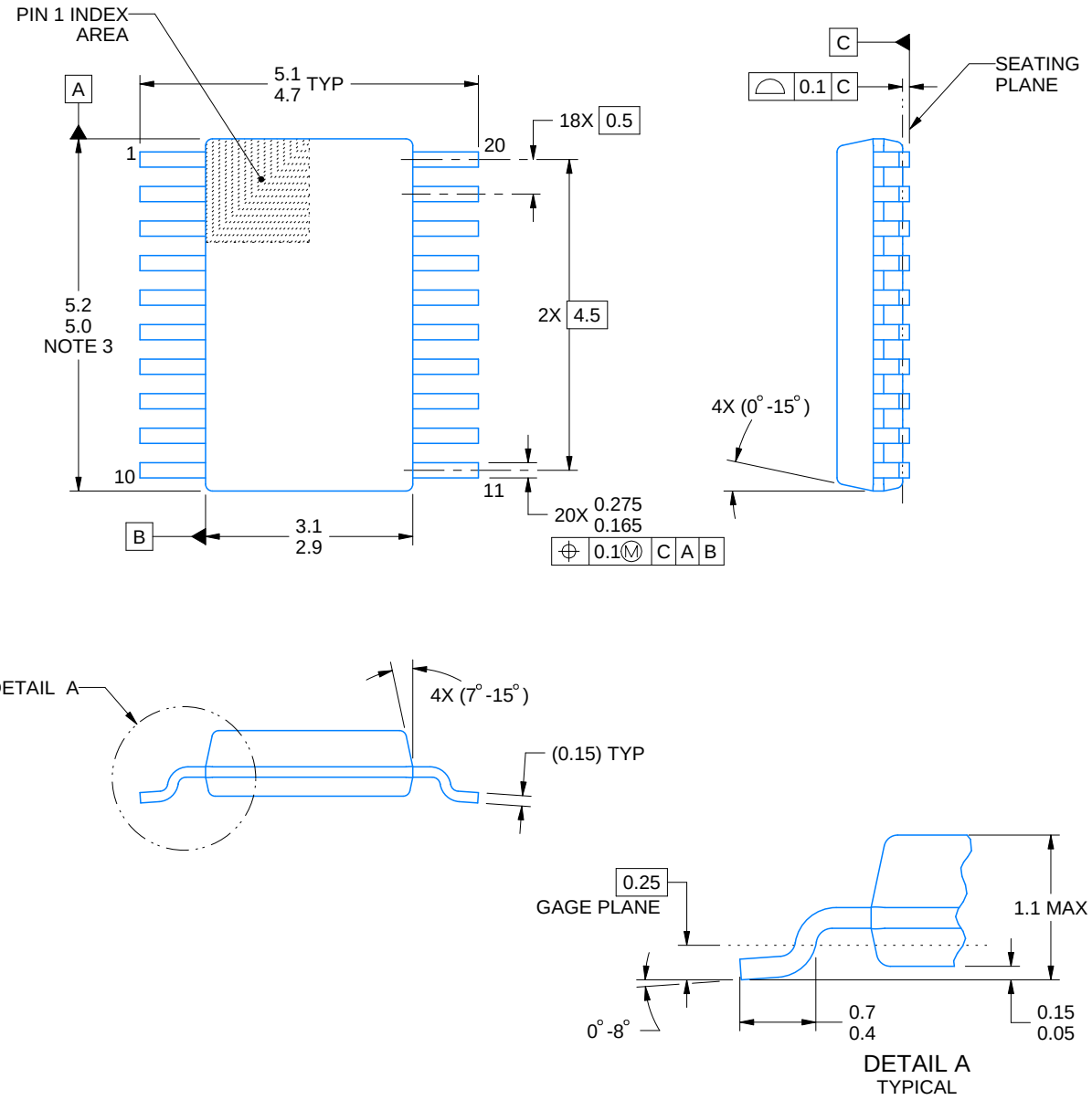
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGS0020A

VSSOP - 1.1 mm max height

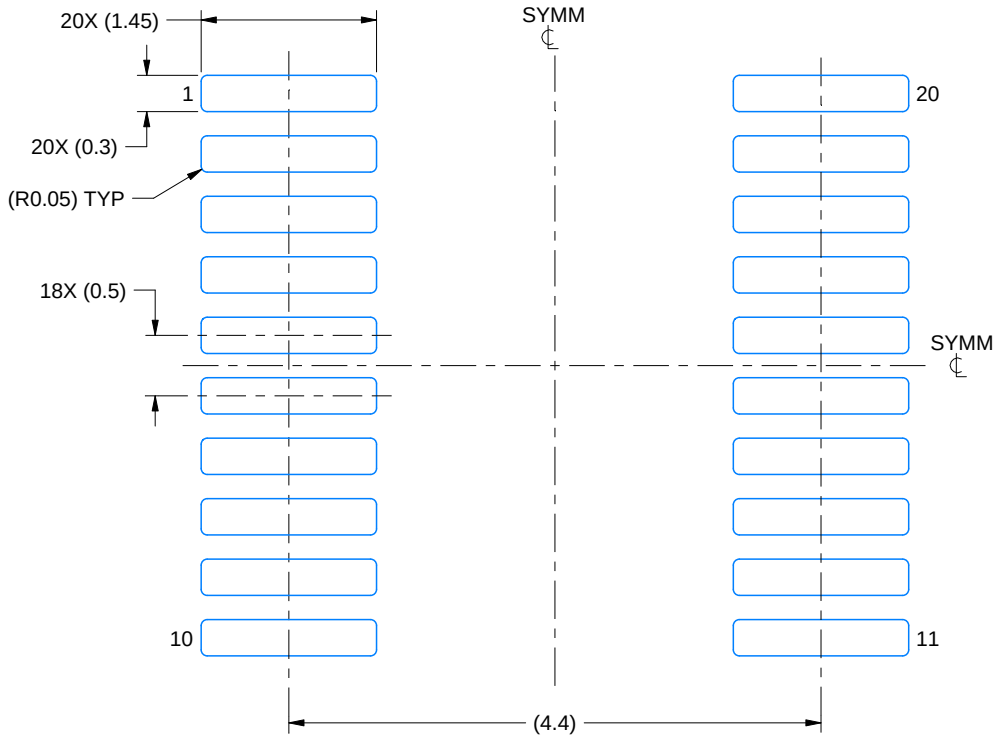
SMALL OUTLINE PACKAGE



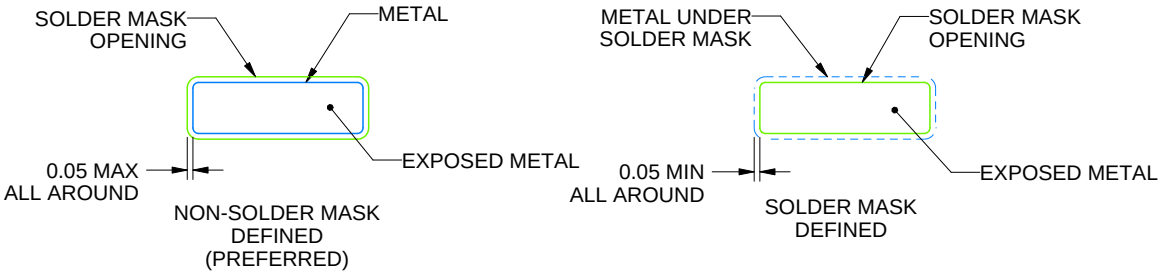
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. No JEDEC registration as of September 2020.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
SCALE: 16X

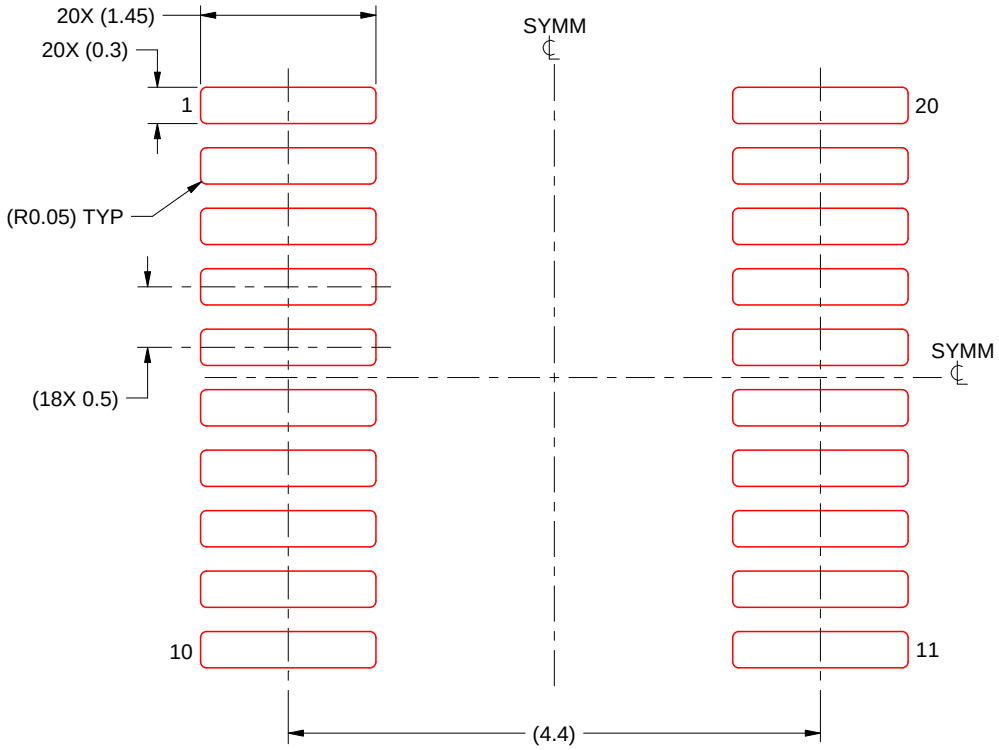


SOLDER MASK DETAILS

4226367/A 10/2020

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



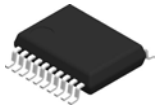
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 16X

4226367/A 10/2020

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

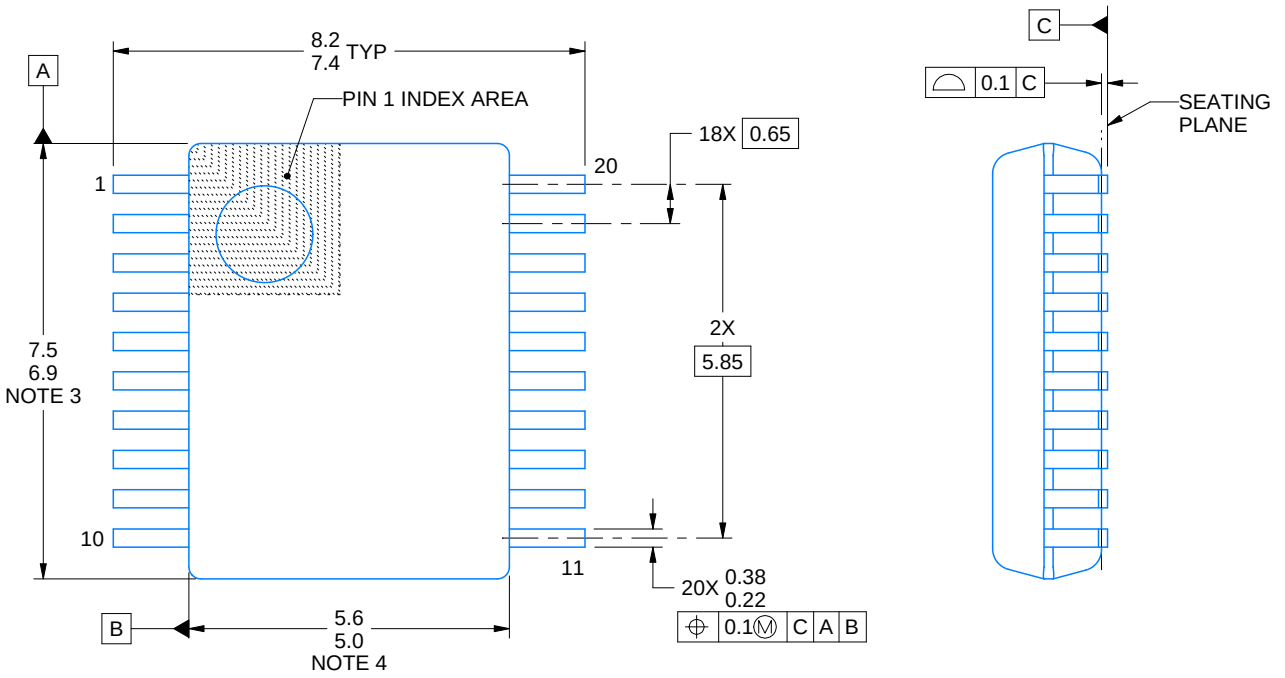
DB0020A

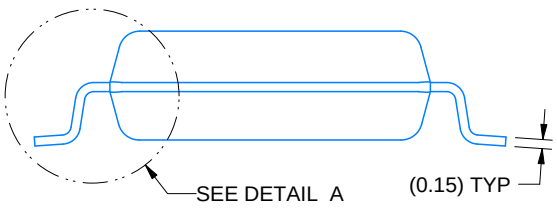


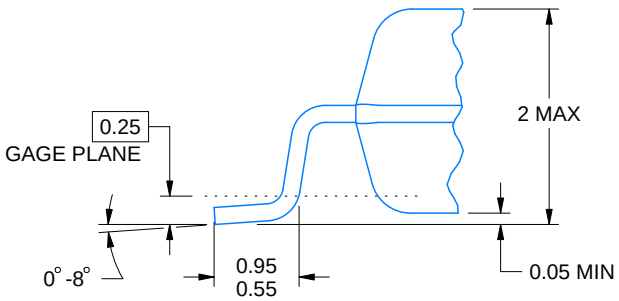
PACKAGE OUTLINE

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE





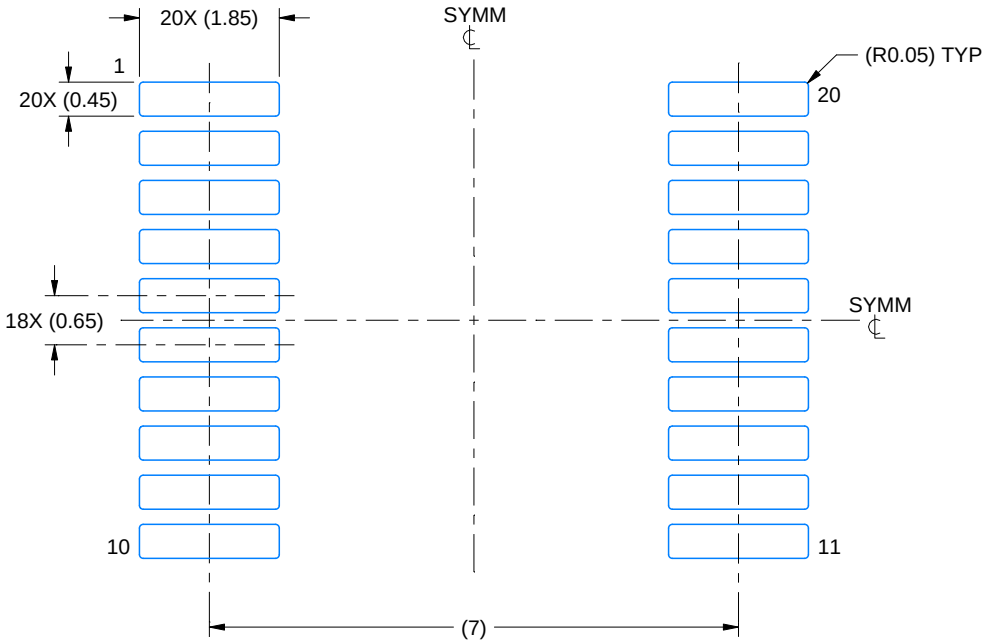


DETAIL A
TYPICAL

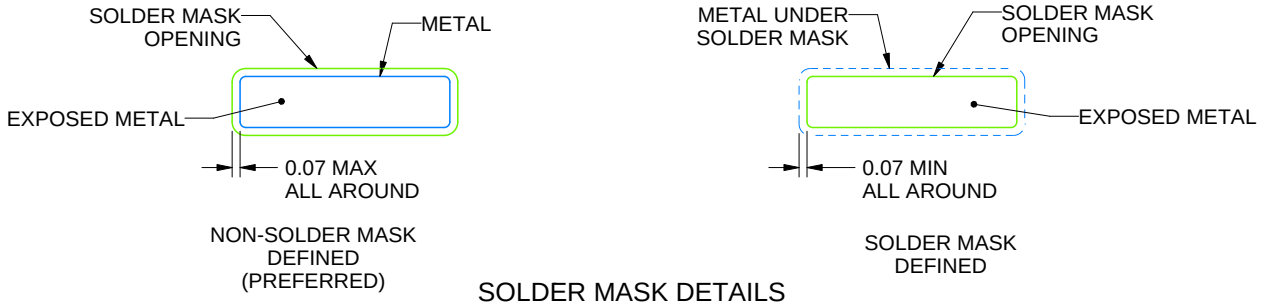
4214851/B 08/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4214851/B 08/2019

NOTES: (continued)

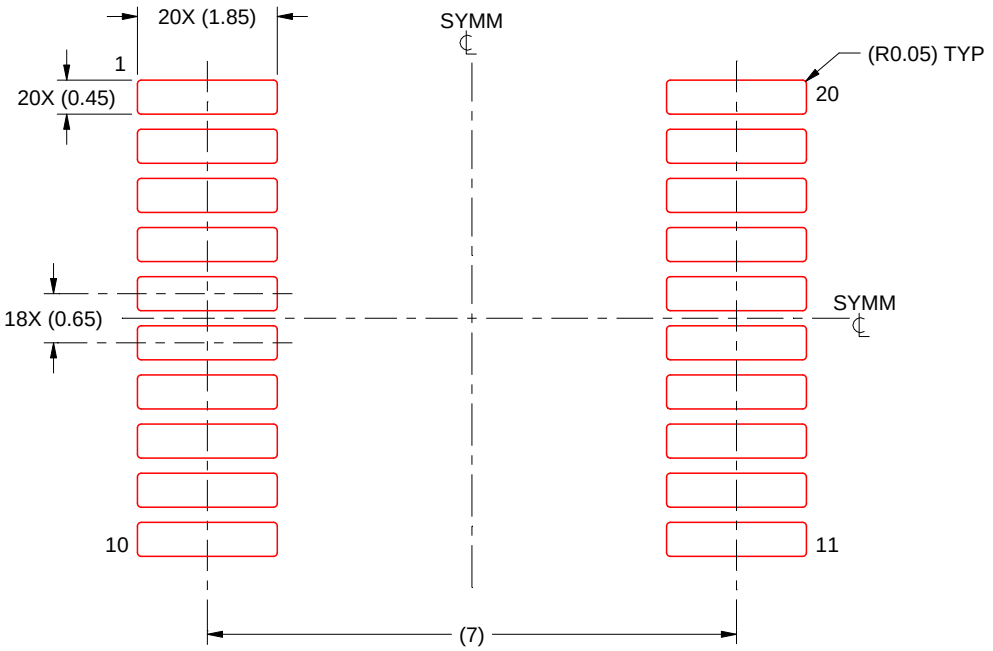
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

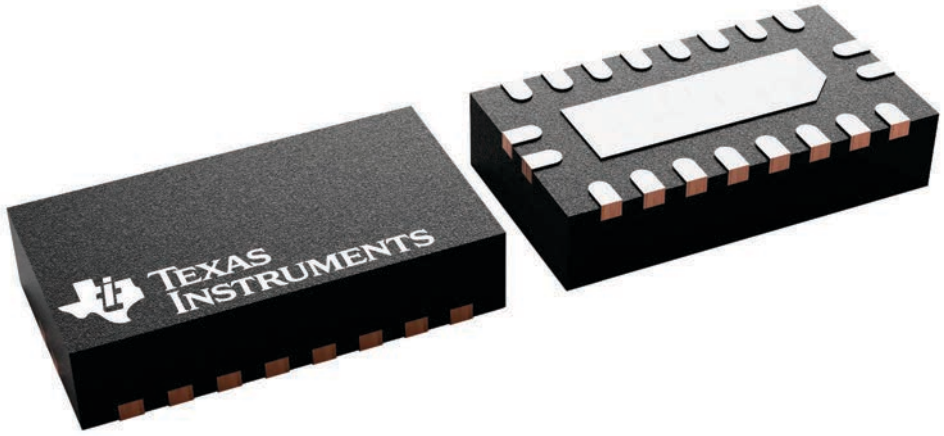
RKS 20

VQFN - 1 mm max height

2.5 x 4.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



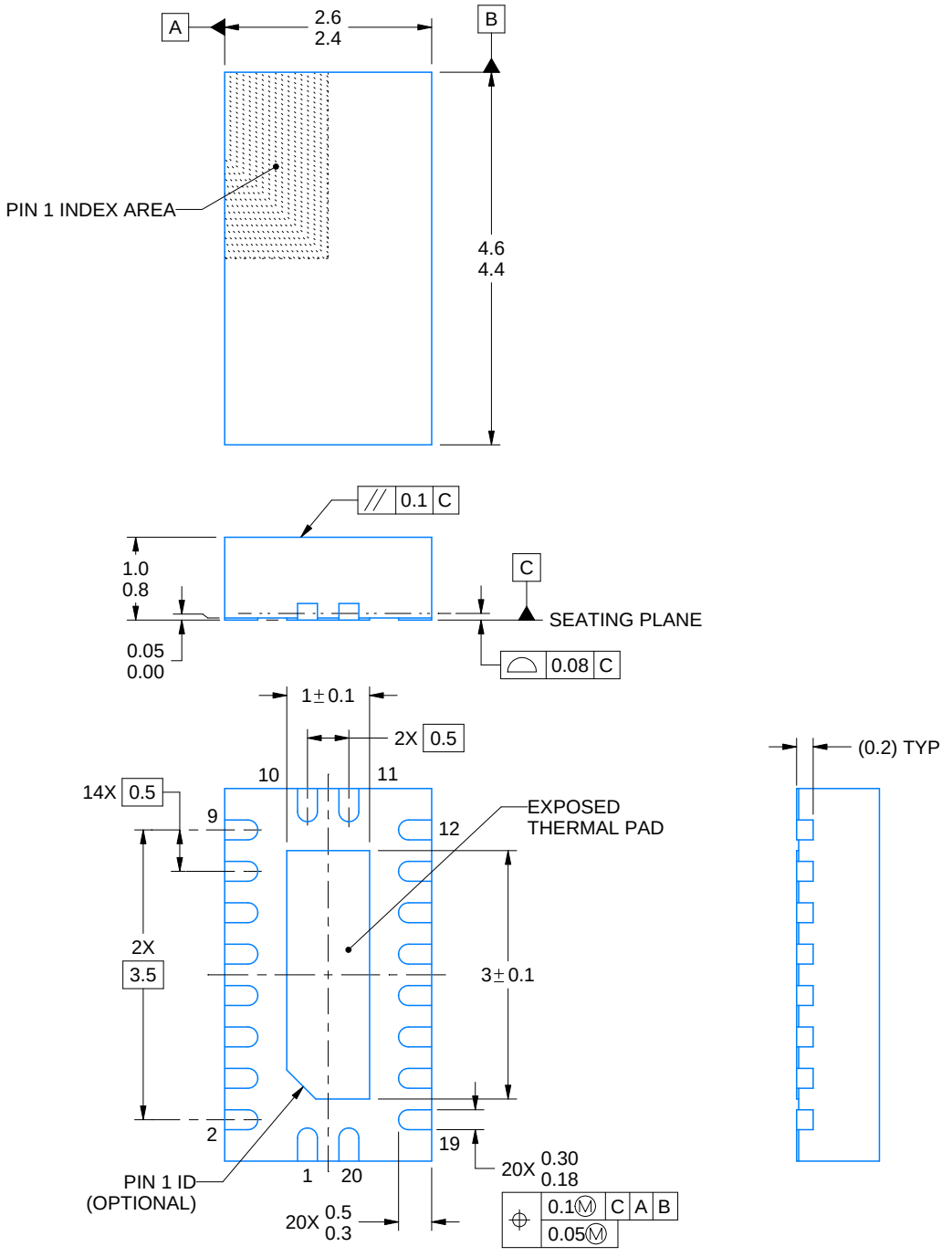
4226872/A

PACKAGE OUTLINE

RKS0020A

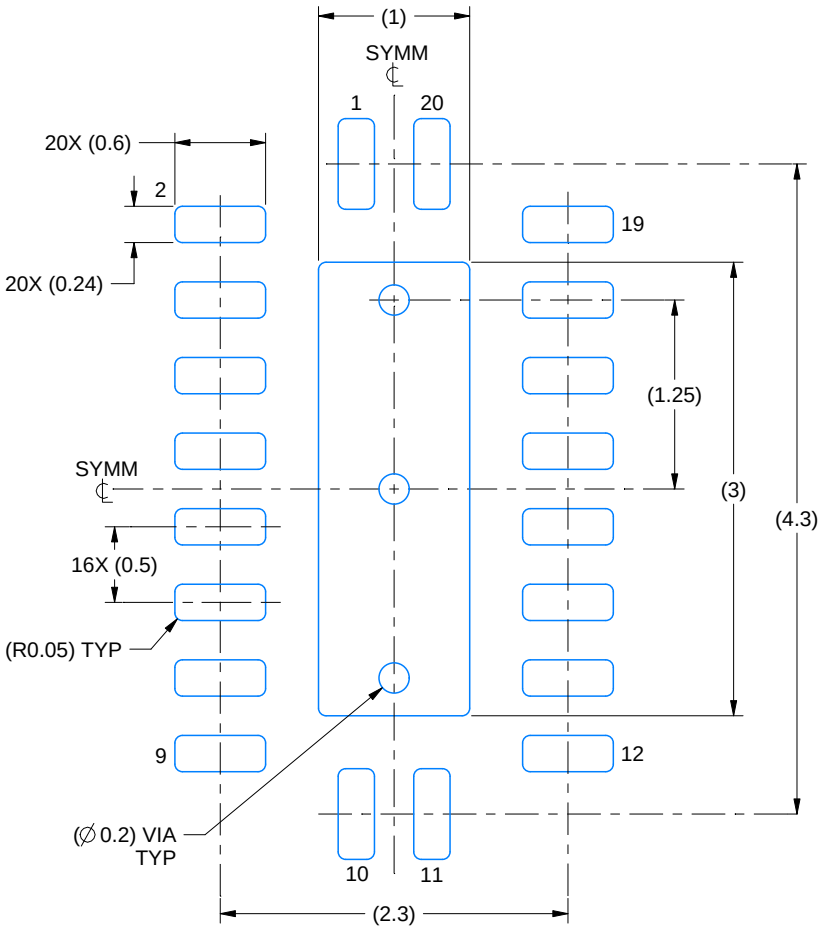
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

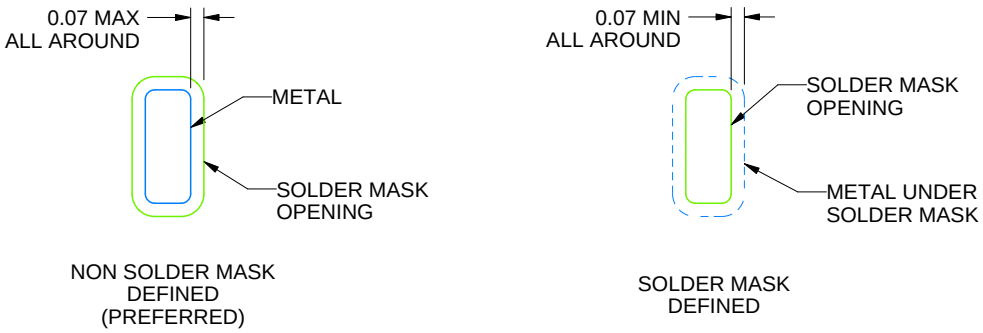


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

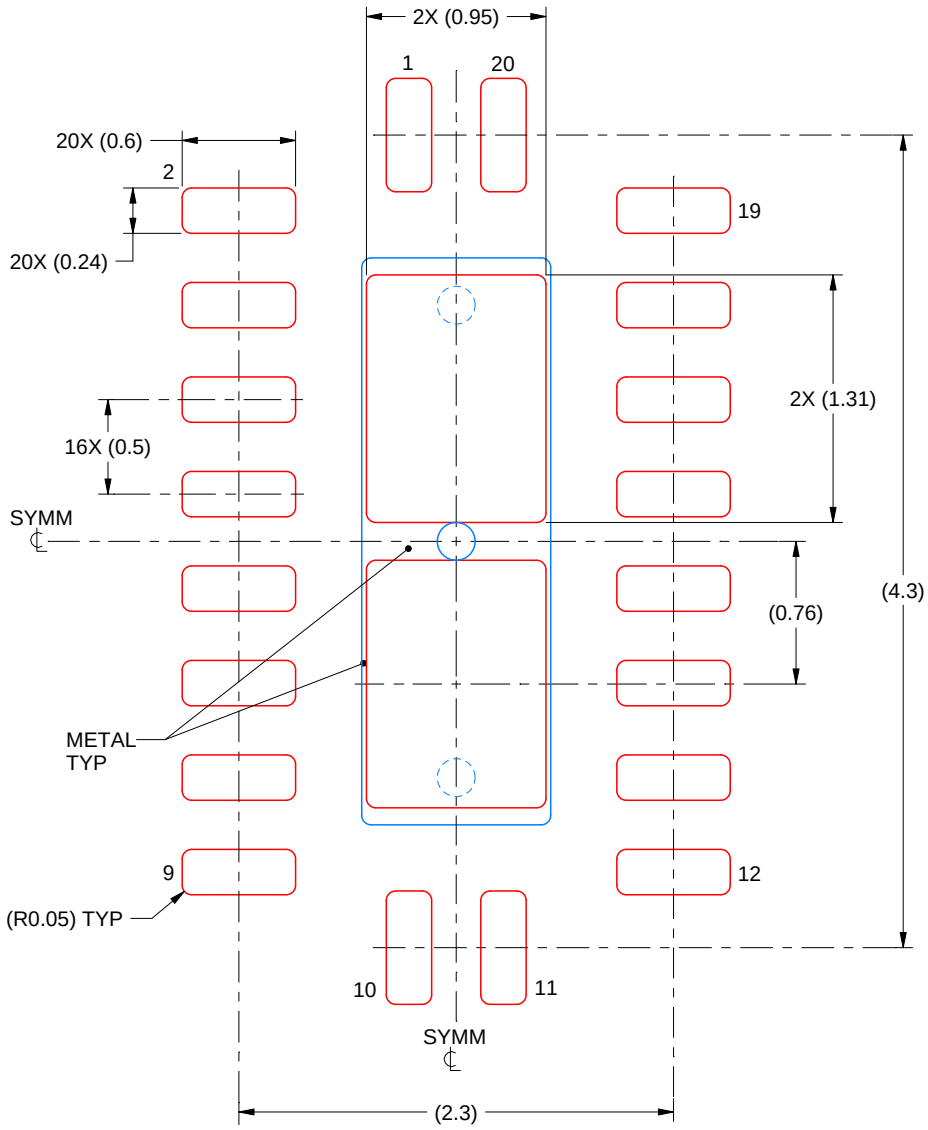


SOLDER MASK DETAILS

4222490/B 02/2021

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
83% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4222490/B 02/2021

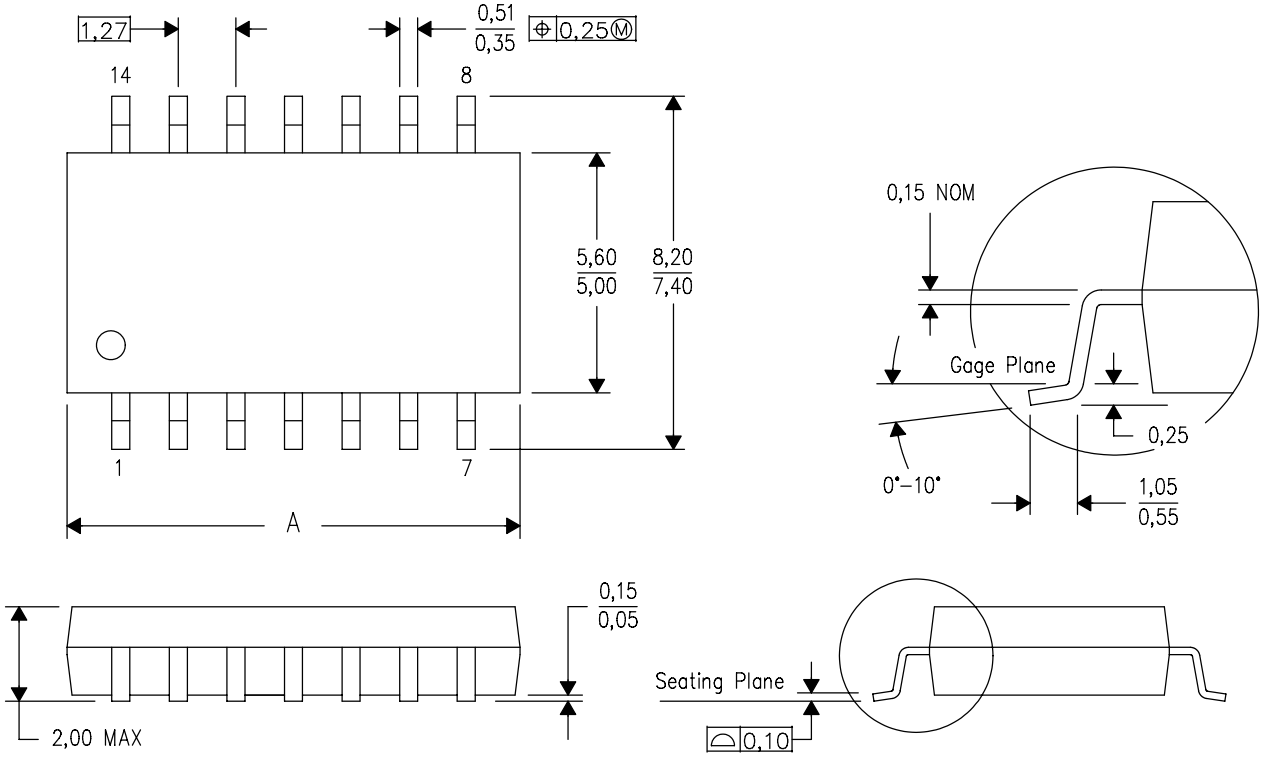
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

GENERIC PACKAGE VIEW

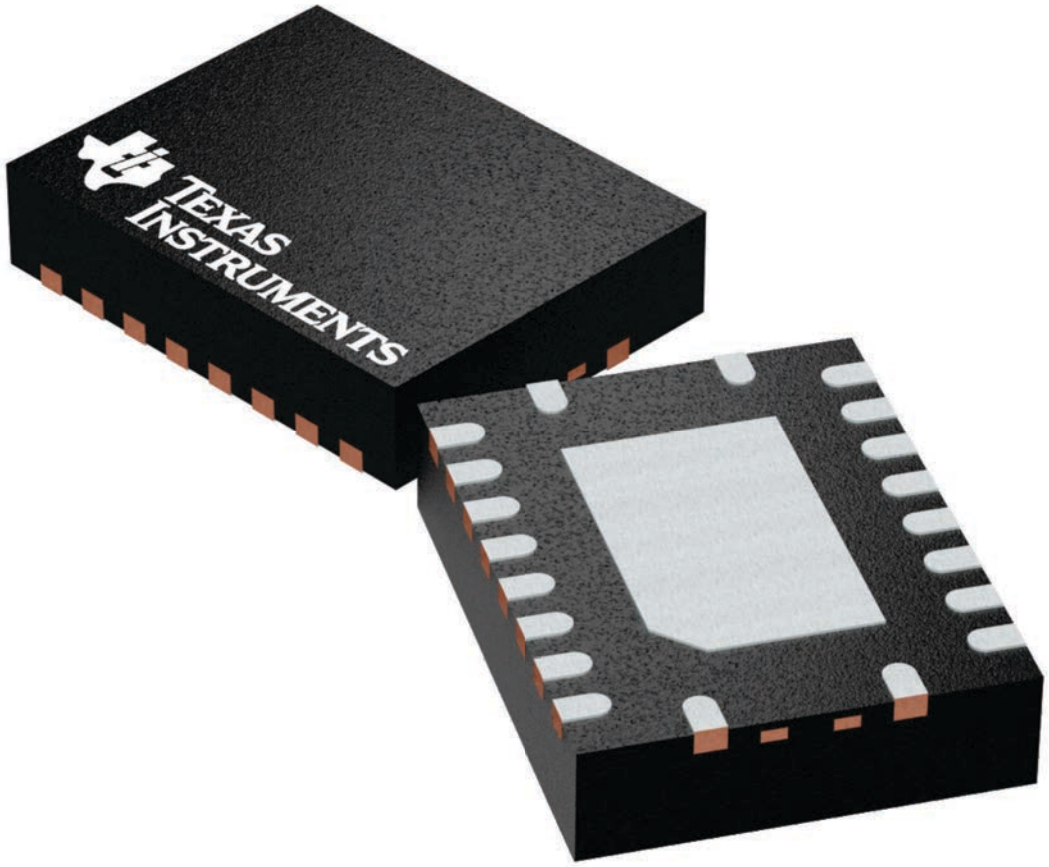
RGY 20

VQFN - 1 mm max height

3.5 x 4.5, 0.5 mm pitch

PLASTIC QUAD FGLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



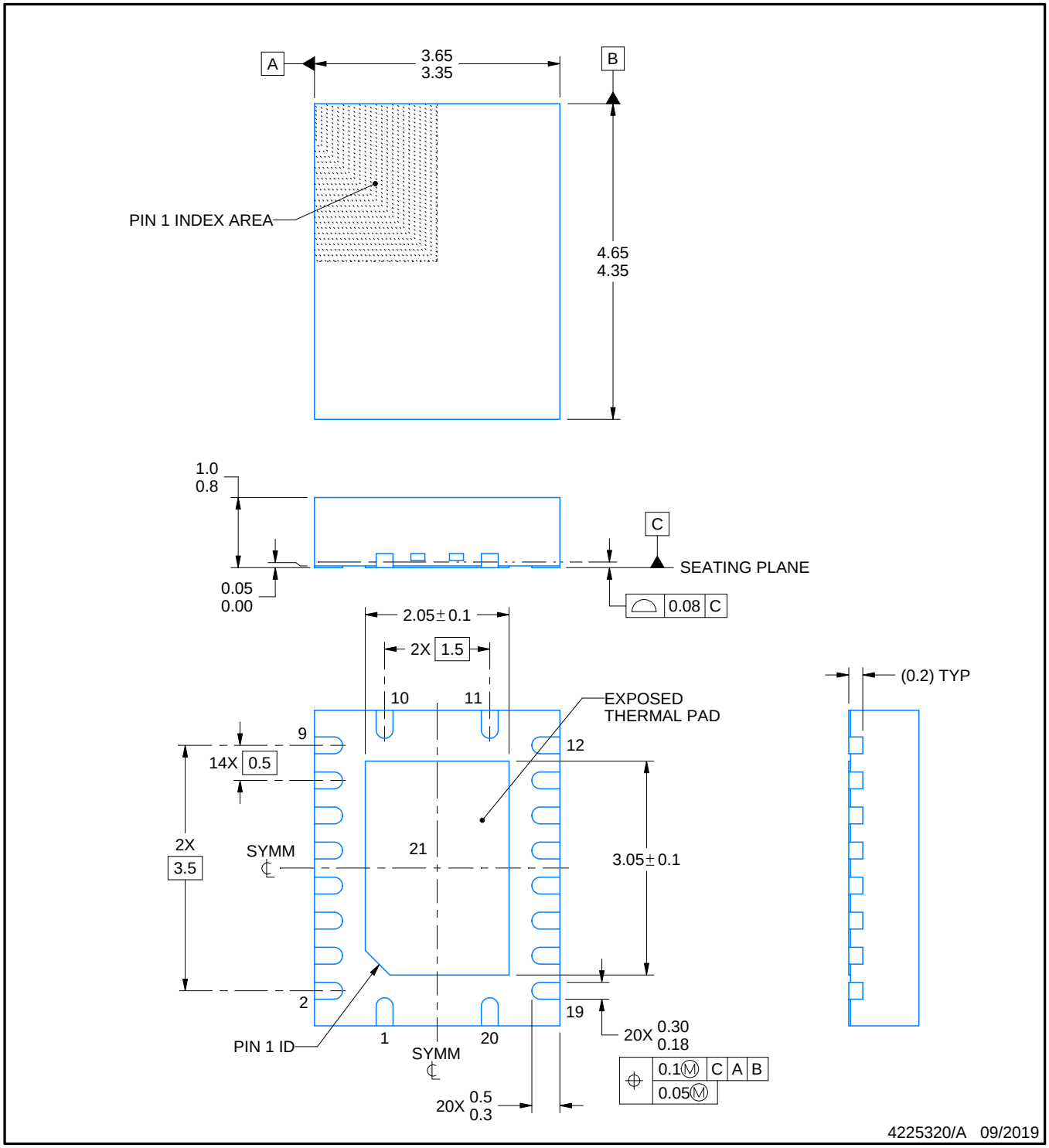
4225264/A

RGY0020A

PACKAGE OUTLINE

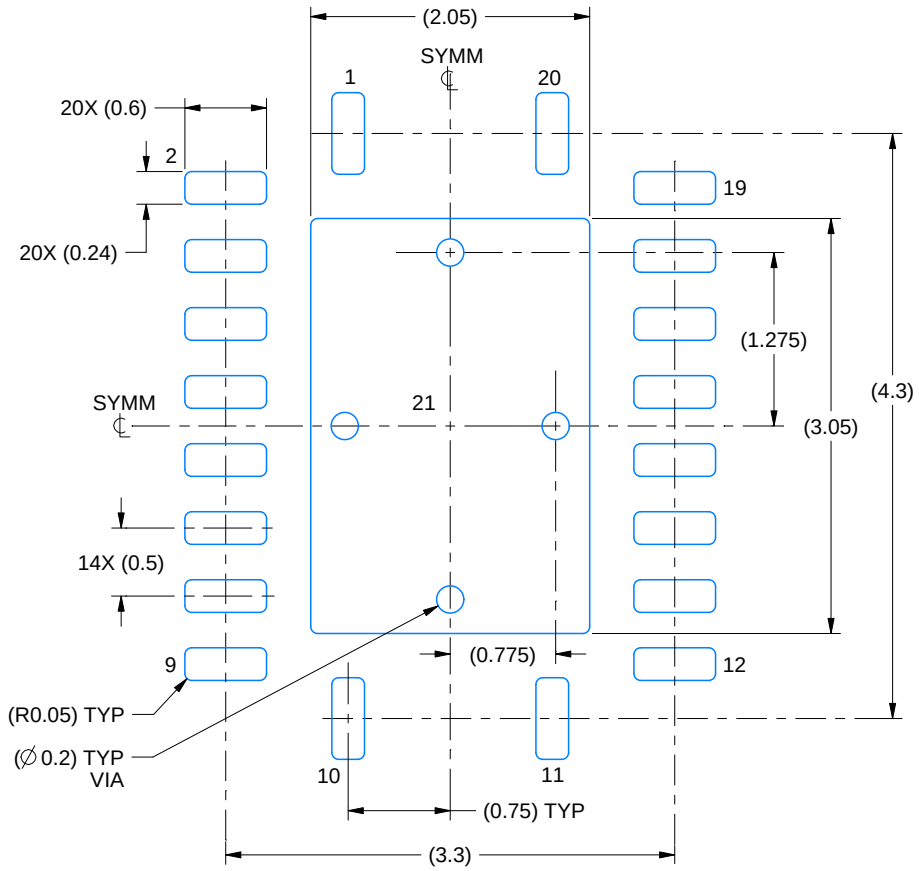
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

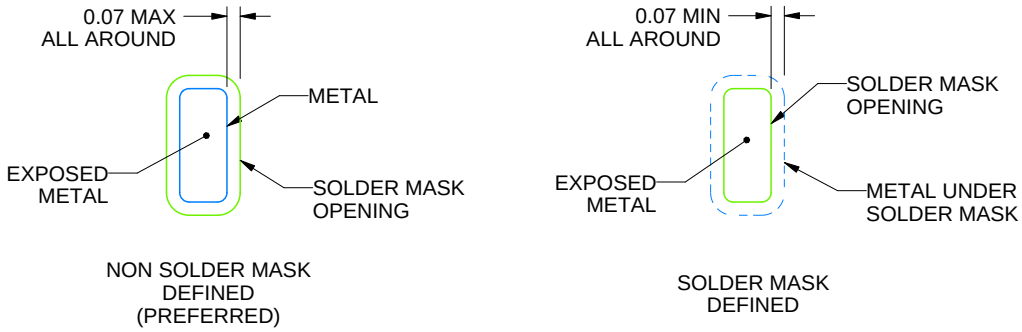


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

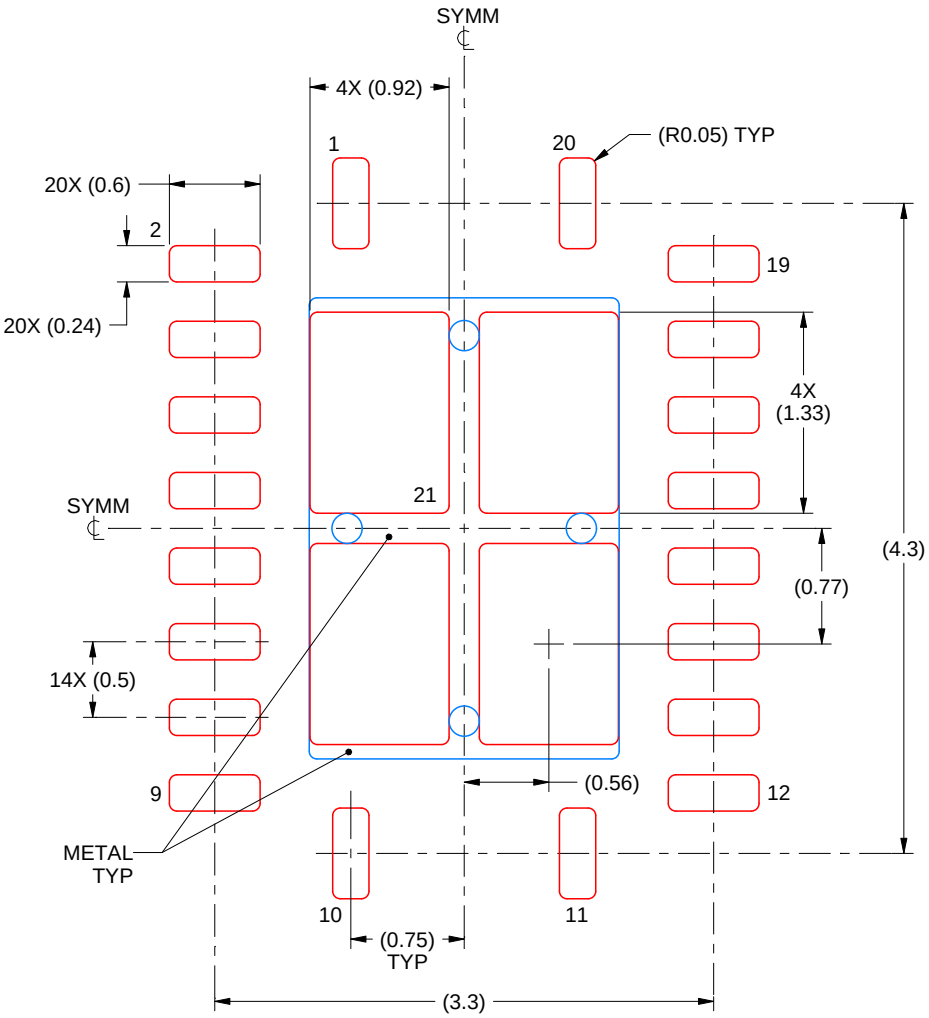


SOLDER MASK DETAILS

4225320/A 09/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



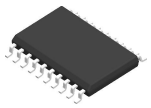
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 21
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4225320/A 09/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

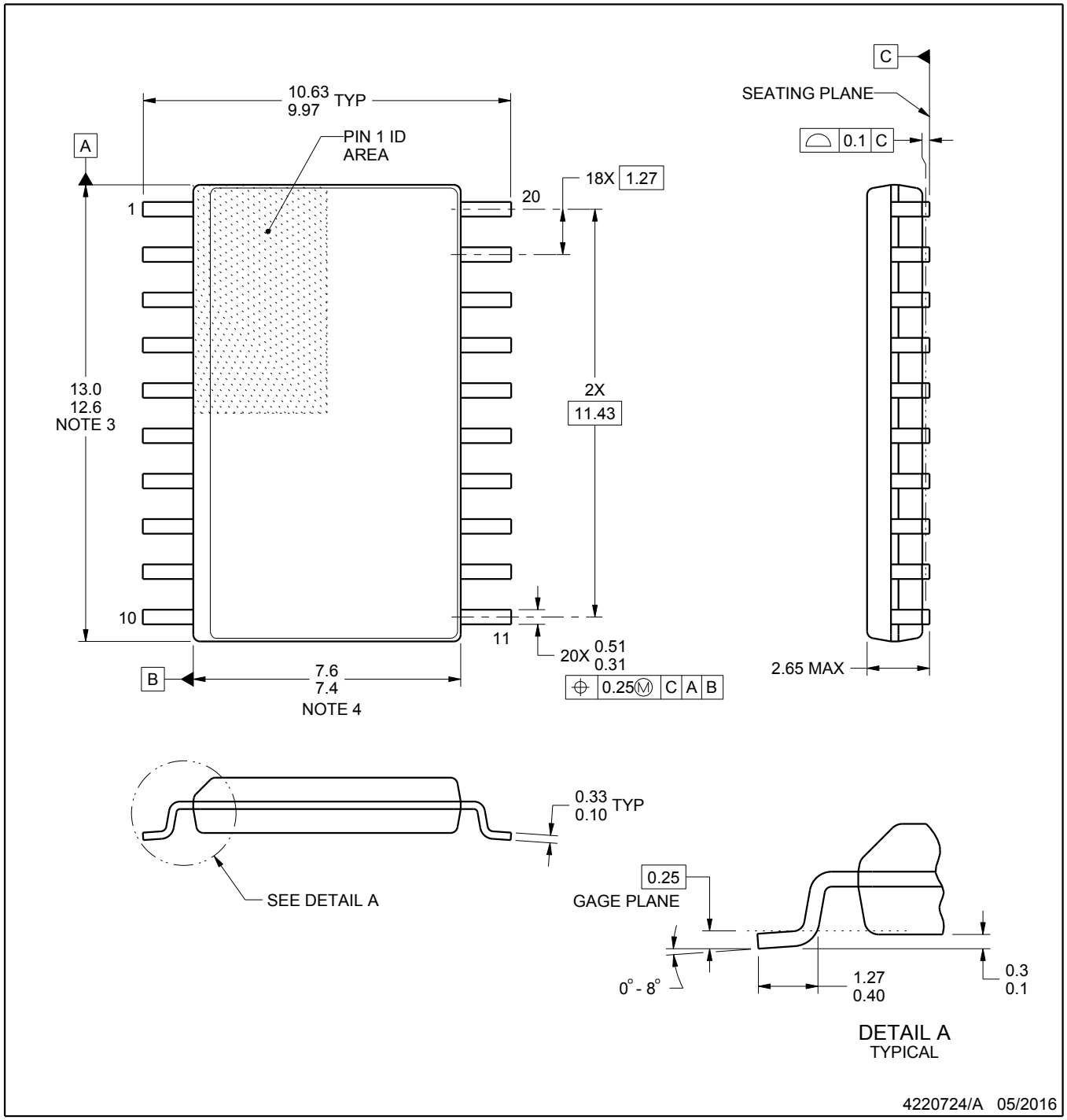


PACKAGE OUTLINE

DW0020A

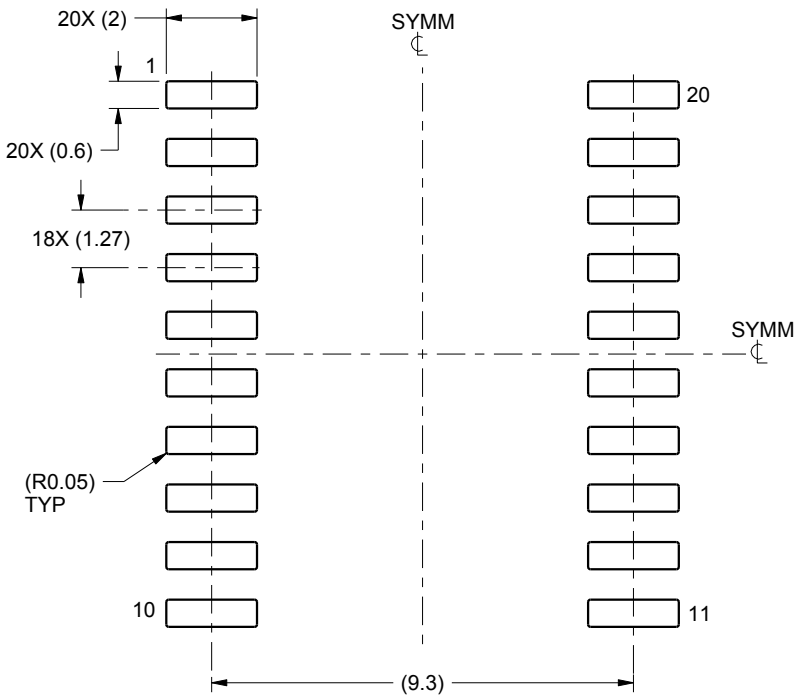
SOIC - 2.65 mm max height

SOIC

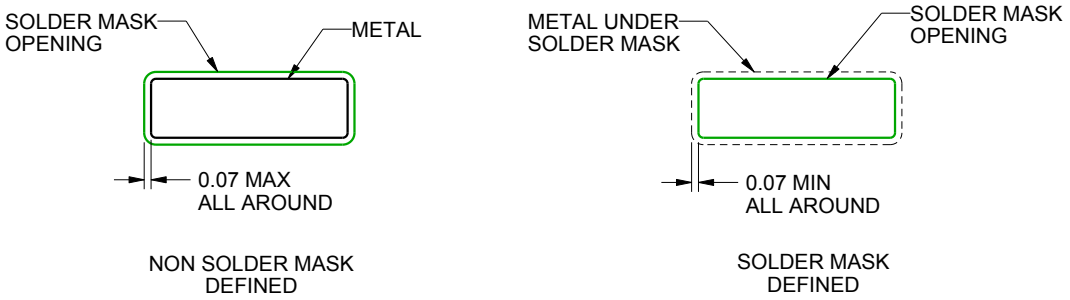


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X

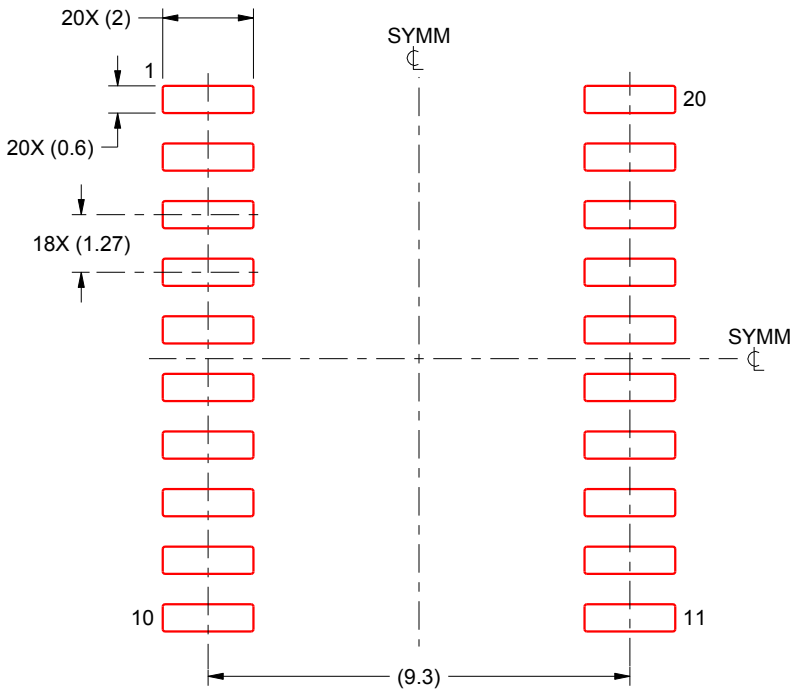


SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025