DUAL DIFFERENTIAL LINE DRIVER

1 Features

- Meets or exceeds the requirements of ANSI EIA/ TIA-422-B and ITU recommendation V.11
- Single 5V supply
- Balanced-line operation
- TTL compatible
- High output impedance in power-off condition
- High-current active-pullup outputs
- Short-circuit protection
- Dual channels
- Input clamp diodes

2 Applications

- Factory automation
- ATM and cash counters
- Smart grid
- AC and servo motor drives

3 Description

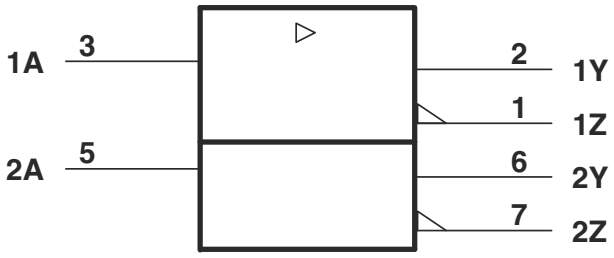
The SN75158 is a dual differential line driver designed to satisfy the requirements set by the ANSI EIA/ TIA-422-B and ITU V.11 interface specifications. The outputs provide signals with high-current capability for driving balanced lines, such as twisted pair, at normal line impedance without high power dissipation. The output stages are TTL totem-pole outputs, providing a high-impedance state in the power-off condition.

The SN75158 is characterized for operation from 0°C to 70°C.

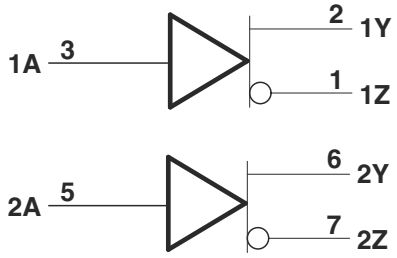
Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
SN75158	SOIC (D, 8)	4.9mm × 6mm
	PDIP (P, 8)	9.81mm × 9.43mm
	SOP (PS, 8)	6.2mm × 7.8mm

(1) For more information, see Section 8.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Logic Symbol[1]



Logic Diagram (Positive Logic)

[1] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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4 Pin Configuration and Functions

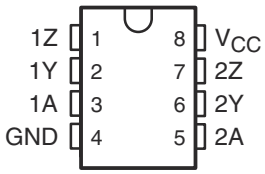


Figure 4-1. D, P, OR PS Package (Top View)

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
1Z	1	O	Inverting Output of Differential Driver on Channel 1
1Y	2	O	Non-Inverting Output for Differential Driver on Channel 1
1A	3	I	Single Ended Data Input for Channel 1
GND	4	GND	Device Ground
2A	5	I	Single Ended Data Input for Channel 2
2Y	6	O	Non-Inverting Output for Differential Driver on Channel 2
2Z	7	O	Inverting Output of Differential Driver on Channel 2
V_{CC}	8	P	5V Power Supply Positive Terminal Connection

(1) Signal Types: I = Input, O = Output, I/O = Input or Output, P = Power, GND = Ground.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage(2)		7	V
V_I	Input voltage range		5.5	V
	Continuous total power dissipation		See Dissipation Ratings	
T_J	Operating free-air temperature range	0	70	°C
T_{stg}	Storage temperature range	–65	150	°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 s		260	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential input voltage, are with respect to the network ground terminal.
(3) Differential input voltage is measured at the noninverting input with respect to the corresponding inverting input.

5.2 Dissipation Ratings

PACKAGE	TA ≤ 25°C POWER RATING	OPERATING FACTOR ABOVE TA = 25°C	TA ≤ 70°C POWER RATING
D	725 mW	5.8 mW/°C	464 mW
P	1000 mW	8.0 mW/°C	640 mW
PS	450 mW	3.6 mW/°C	288 mW

5.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			–40	mA
I_{OL}	Low-level output current			40	mA
T_A	Operating free-air temperature	0		70	°C

5.4 Thermal Information

THERMAL METRIC(1)		D	P	PS	UNIT
		8-Pins			
$R_{\theta JA}$	Junction-to-ambient thermal resistance	116.7	84.3	89.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	56.3	65.4	46.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	63.4	62.1	50.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	8.8	31.3	23.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	62.6	60.4	60.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

5.5 Electrical Characteristics

over recommended ranges of supply voltage,common-mode input voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS[1]		MIN	TYP[2]	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = –12mA		–0.9	–1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2V,	V_{IL} = 0.8V, I_{OH} = –40mA	2.4	3		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2V,	V_{IL} = 0.8V, I_{OH} = 40mA		0.2	0.4	V
$\|V_{OD1}\|$	Differential output voltage	V_{CC} = MAX,	I_O = 0		3.5	2 × V_{OD2}	V
$\|V_{OD2}\|$		V_{CC} = MIN,	R_L = 100Ω, See Figure 6-1		3	3	V
ΔV_{OD}	Change in magnitude of differential output voltage[3]	V_{CC} = MIN,	R_L = 100Ω, See Figure 6-1		±0.02	±0.4	V
V_{OC}	Common-mode output voltage[4]	V_{CC} = MAX,	R_L = 100Ω, See Figure 6-1		1.8	3	V
		V_{CC} = MIN,			1.5	3	
ΔV_{OC}	Change in magnitude of common-mode output voltage[3]	V_{CC} = MIN or MAX,	R_L = 100Ω, See Figure 6-1		±0.02	±0.4	V
I_O	Output current with power off	V_{CC} = 0,	V_O = 6V		0.1	100	μA
			V_O = –0.25V		–0.1	–100	
			V_O = –0.25 to 6V			±100	
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5V			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4V			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4V			–1.6	mA
I_{OS}	Short-circuit output current[5]	V_{CC} = MAX,		–40	–90	–150	mA
I_{CC}	Supply current (both drivers)	V_{CC} = MAX, T_A = 25°C,	Inputs grounded, No load		37	50	mA

(1) For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.
(2) All typical values are at V_{CC} = 5 V and T_A = 25°C except for V_{OC}, for which V_{CC} is as stated under test conditions.
(3) ΔV_{OD} and $\Delta|V_{OC}|$ are the changes in magnitudes of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
(4) In ANSI Standard EIA/TIA-422-B, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.
(5) Only one output should be shorted at a time, and duration of the short circuit should not exceed one second.

5.6 Switching Characteristics

V_{CC} = 5V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	See Figure 6-2	Termination A		16	25	ns
			Termination B		13	20	
t_{PHL}	Propagation delay time, high- to low-level output	See Figure 6-2	Termination A		10	20	ns
			Termination B		9	15	
t_{TLH}	Transition time, low-to-high-level output	See Figure 6-2	Termination A		4	20	ns
t_{THL}	Transition time, high- to low-level output	See Figure 6-2	Termination A		4	20	ns
	Overshoot factor	See Figure 6-2	Termination C			10	%

5.7 Typical Characteristics

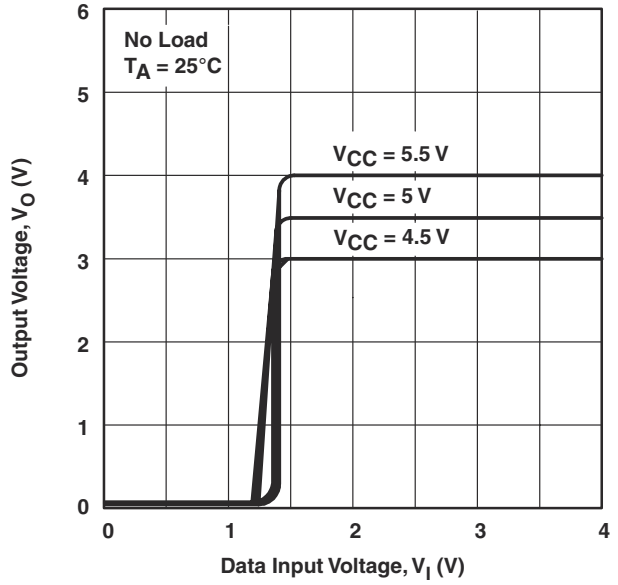


Figure 5-1. Output Voltage vs Data Input Voltage

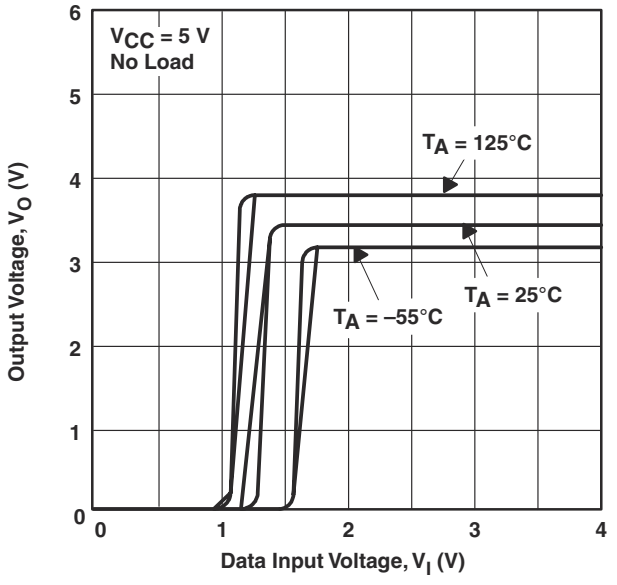


Figure 5-2. Output Voltage vs DATA Input Voltage

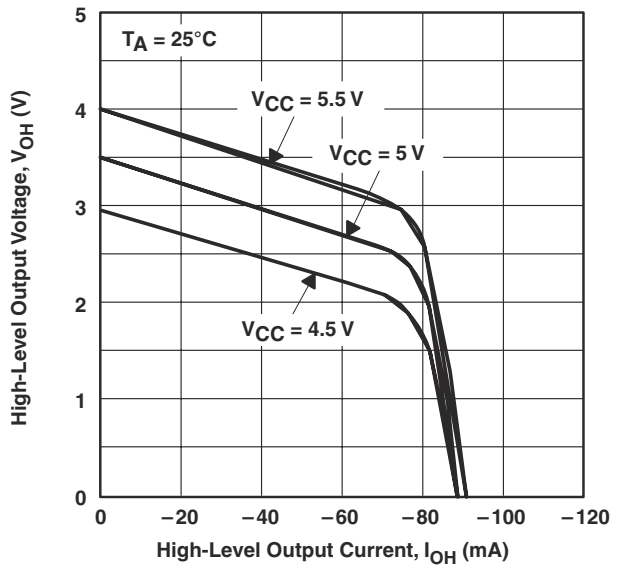


Figure 5-3. High-Level Output Voltage vs High-Level Output Current

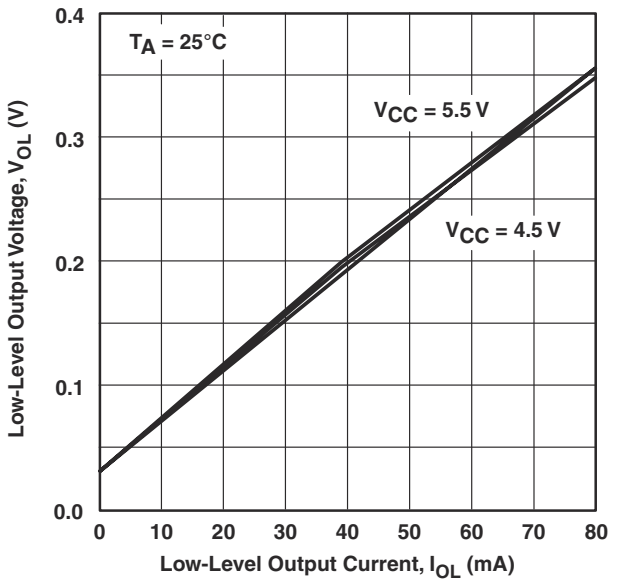


Figure 5-4. Low-Level Output Voltage vs Low-Level Output Current

5.7 Typical Characteristics (continued)

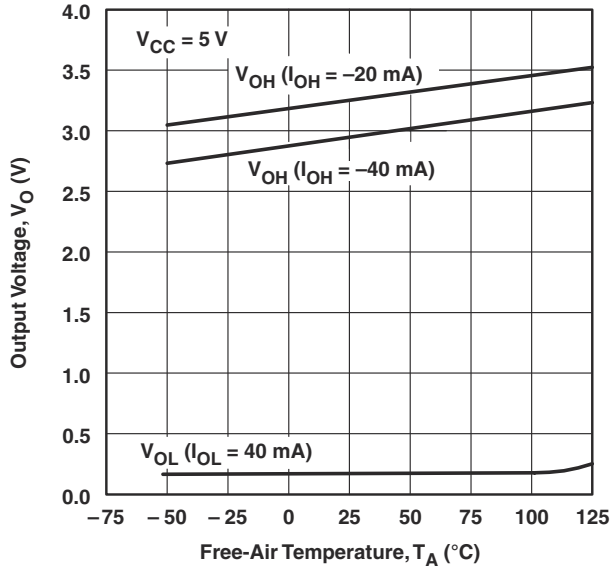


Figure 5-5. Output Voltage vs Free-Air Temperature

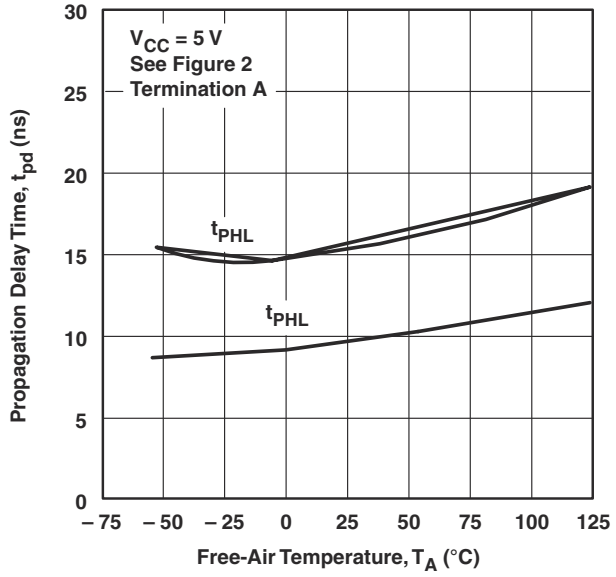


Figure 5-6. Propagation Delay Times vs Free-Air Temperature

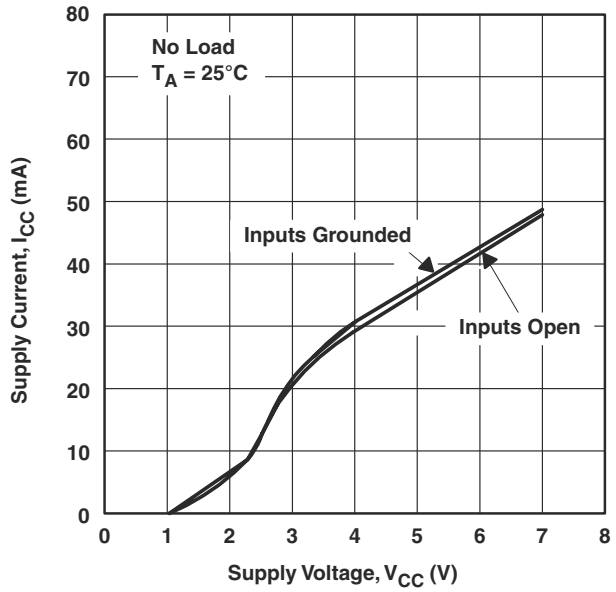


Figure 5-7. Supply Current(Both Drivers) vs Supply Voltage

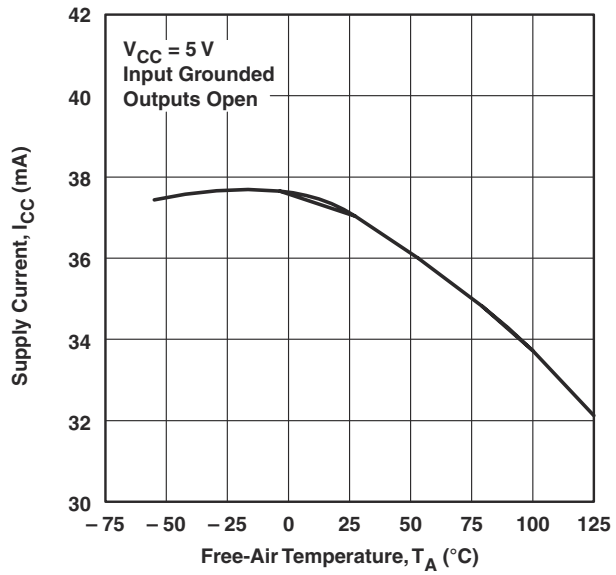


Figure 5-8. Supply Current(Both Drivers) vs Free-Air Temperature

5.7 Typical Characteristics (continued)

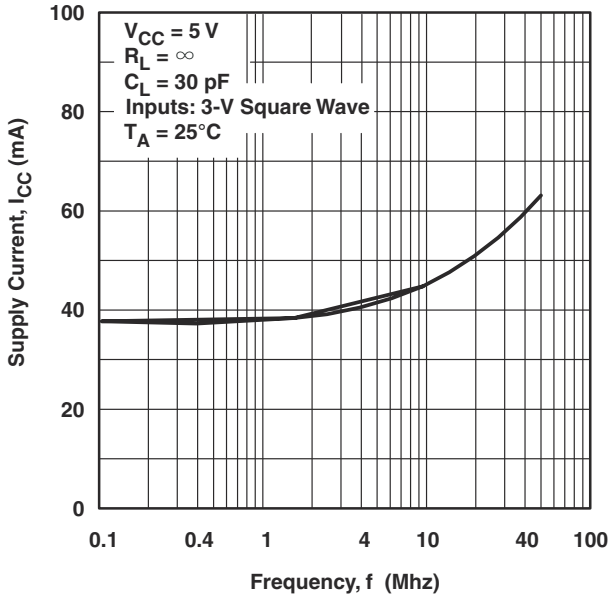


Figure 5-9. Supply Current(Both Drivers) vs Frequency

Parameter Measuremrnt Information

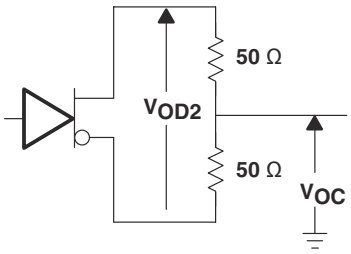
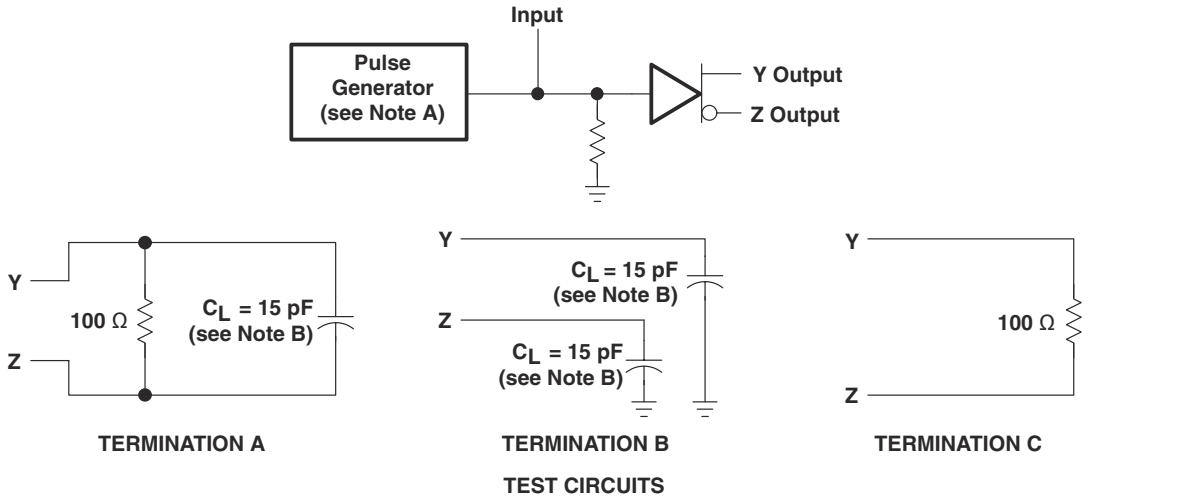


Figure 6-1. Differential and Common-Mode Output Voltages



A. The input pulse is supplied by a generator having the following characteristics: Z_O = 50Ω, t_w = 25ns, PRR ≤ 10MHz.

B. C_L includes probe and jig capacitance.

Figure 6-2. Test Circuit and Voltage Waveforms

6 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

6.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

6.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

6.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

6.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

6.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (May 1995) to Revision C (March 2024)	Page
• Changed the numbering format for tables, figures, and cross-references throughout the document	1

8 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN75158D	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	0 to 70	75158	
SN75158DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75158	Samples
SN75158P	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN75158P	Samples
SN75158PSR	ACTIVE	SO	PS	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	A158	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

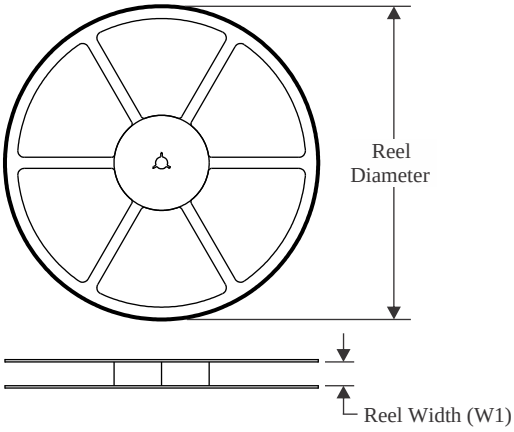
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

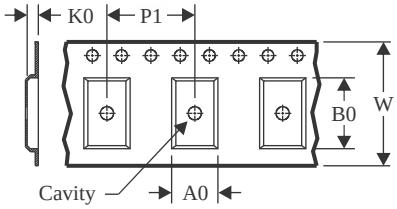
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

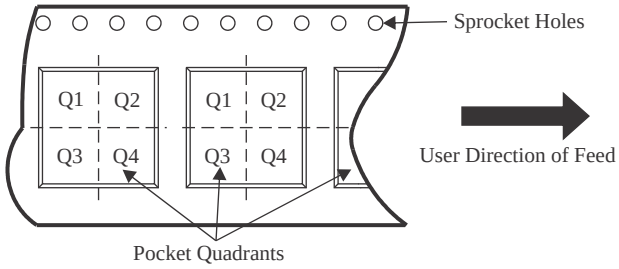


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

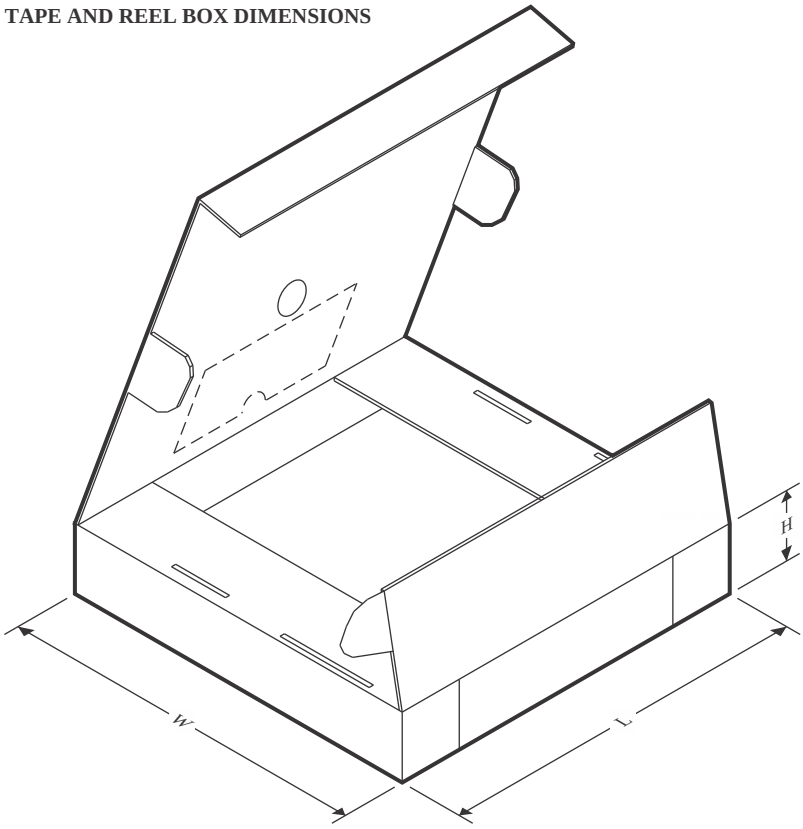
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75158DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN75158DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN75158PSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN75158PSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1

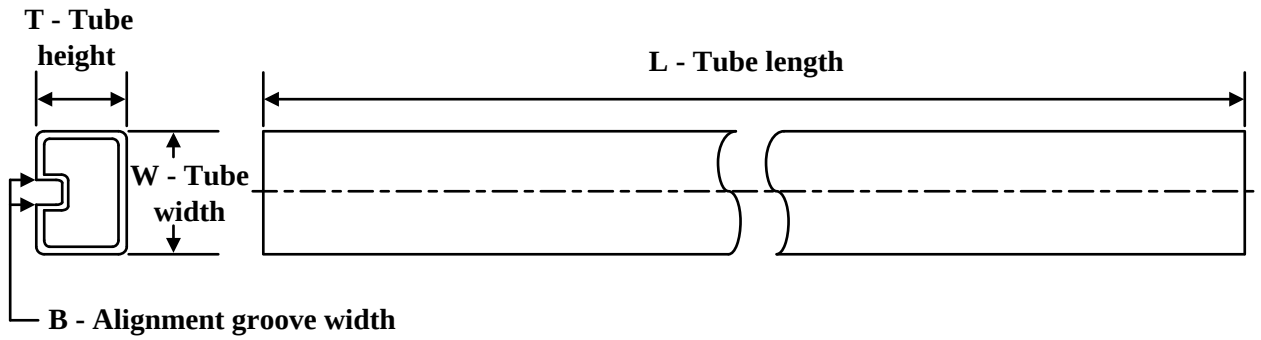
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

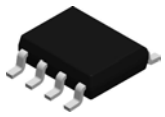
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75158DR	SOIC	D	8	2500	353.0	353.0	32.0
SN75158DR	SOIC	D	8	2500	340.5	336.1	25.0
SN75158PSR	SO	PS	8	2000	356.0	356.0	35.0
SN75158PSR	SO	PS	8	2000	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN75158P	P	PDIP	8	50	506	13.97	11230	4.32

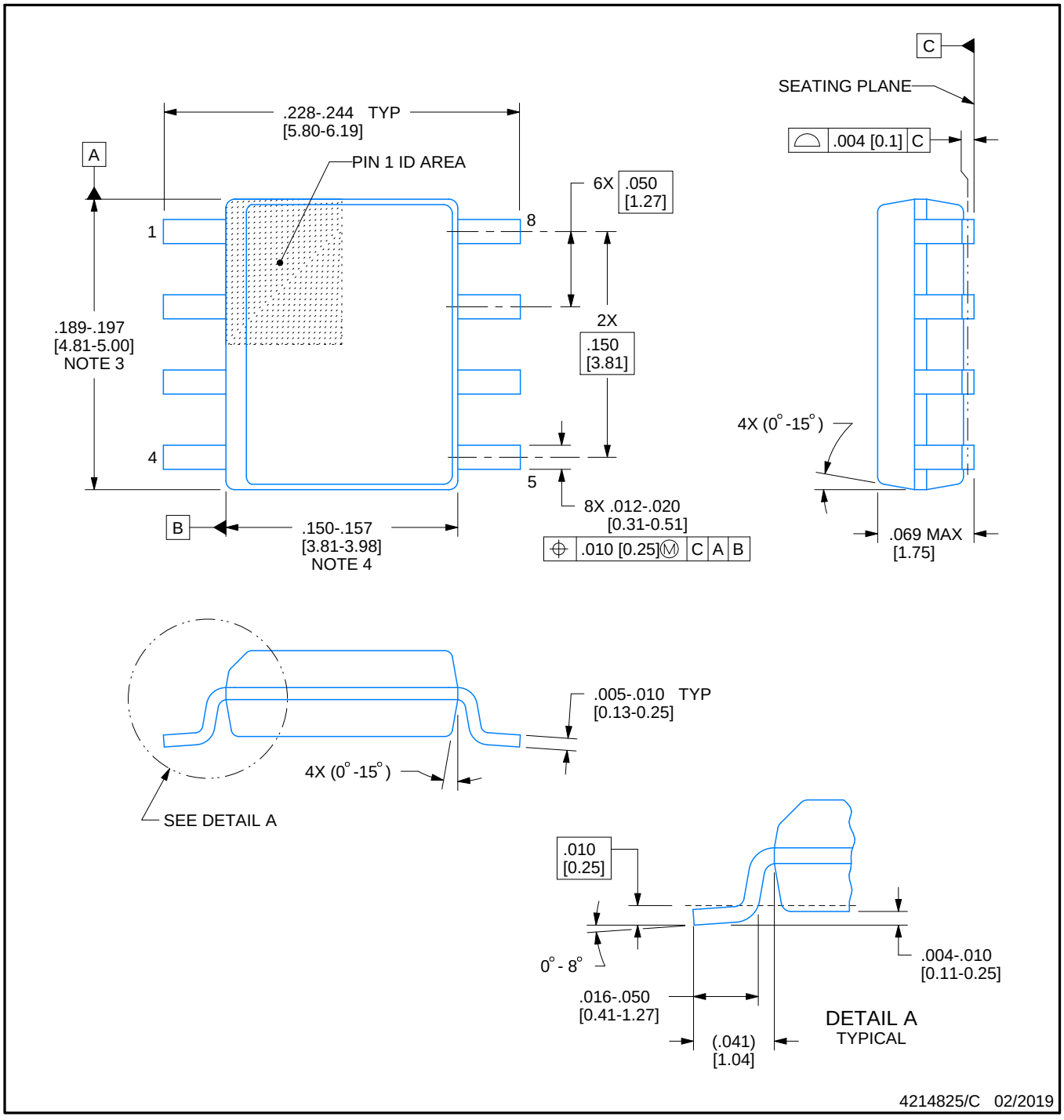


PACKAGE OUTLINE

D0008A

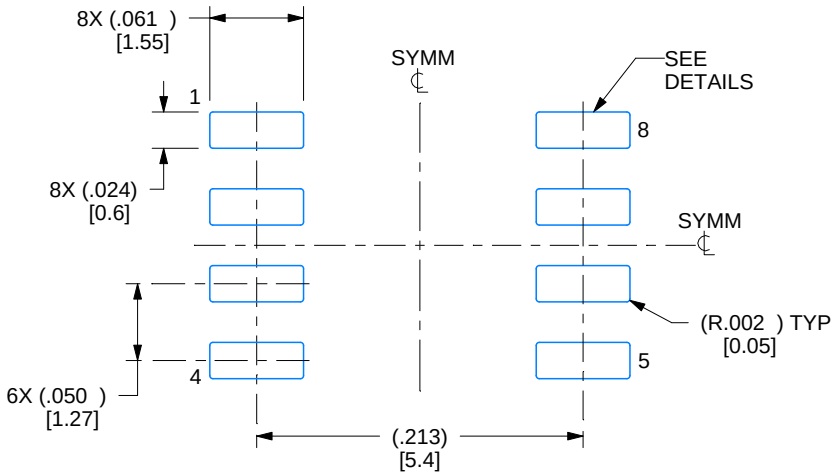
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

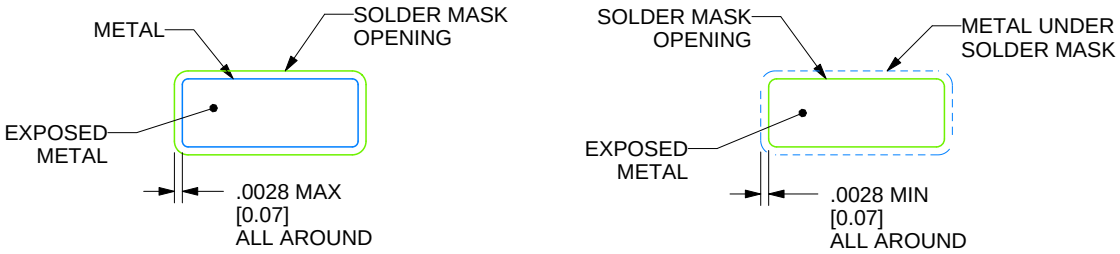


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

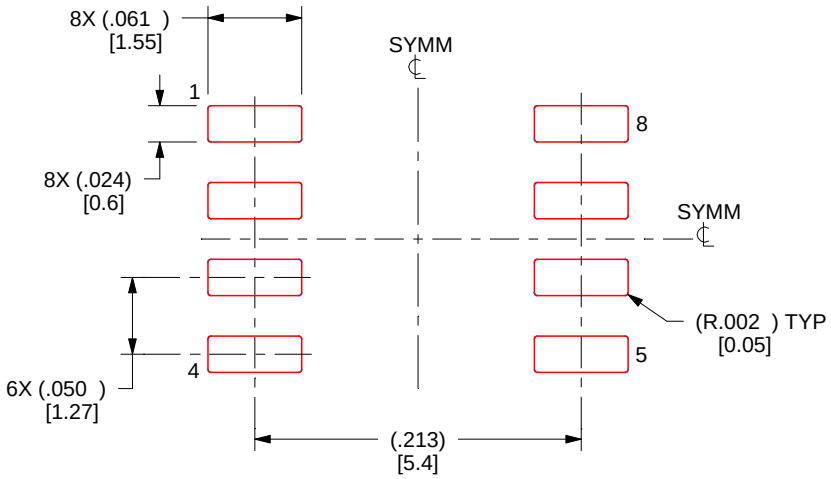
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

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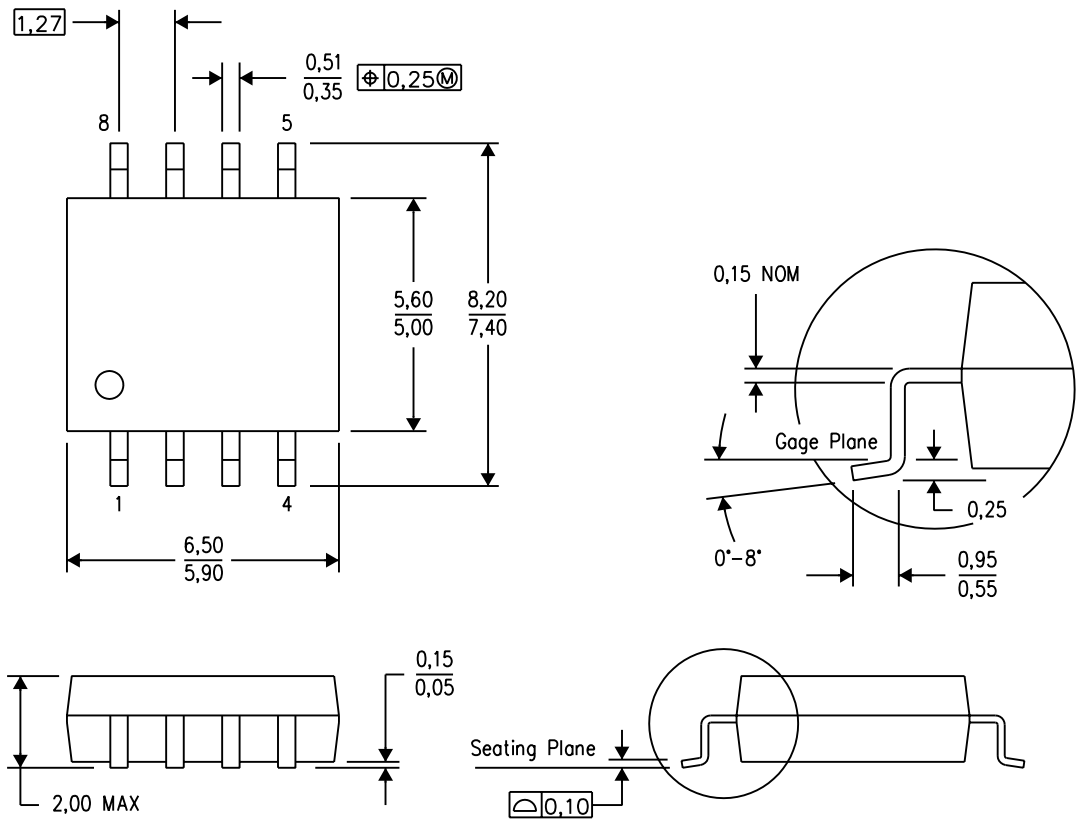
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

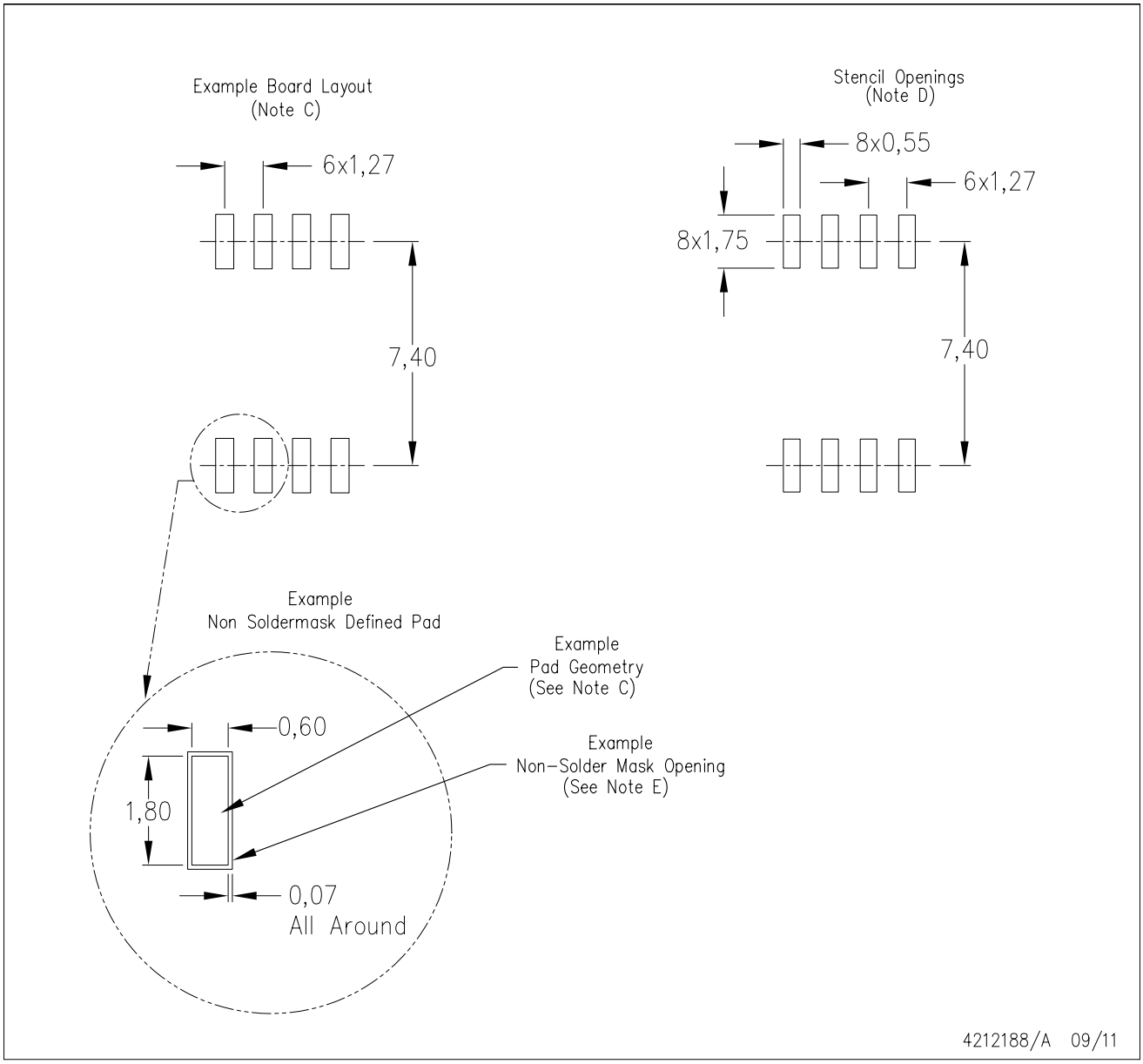
PS (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



4040063/C 03/03

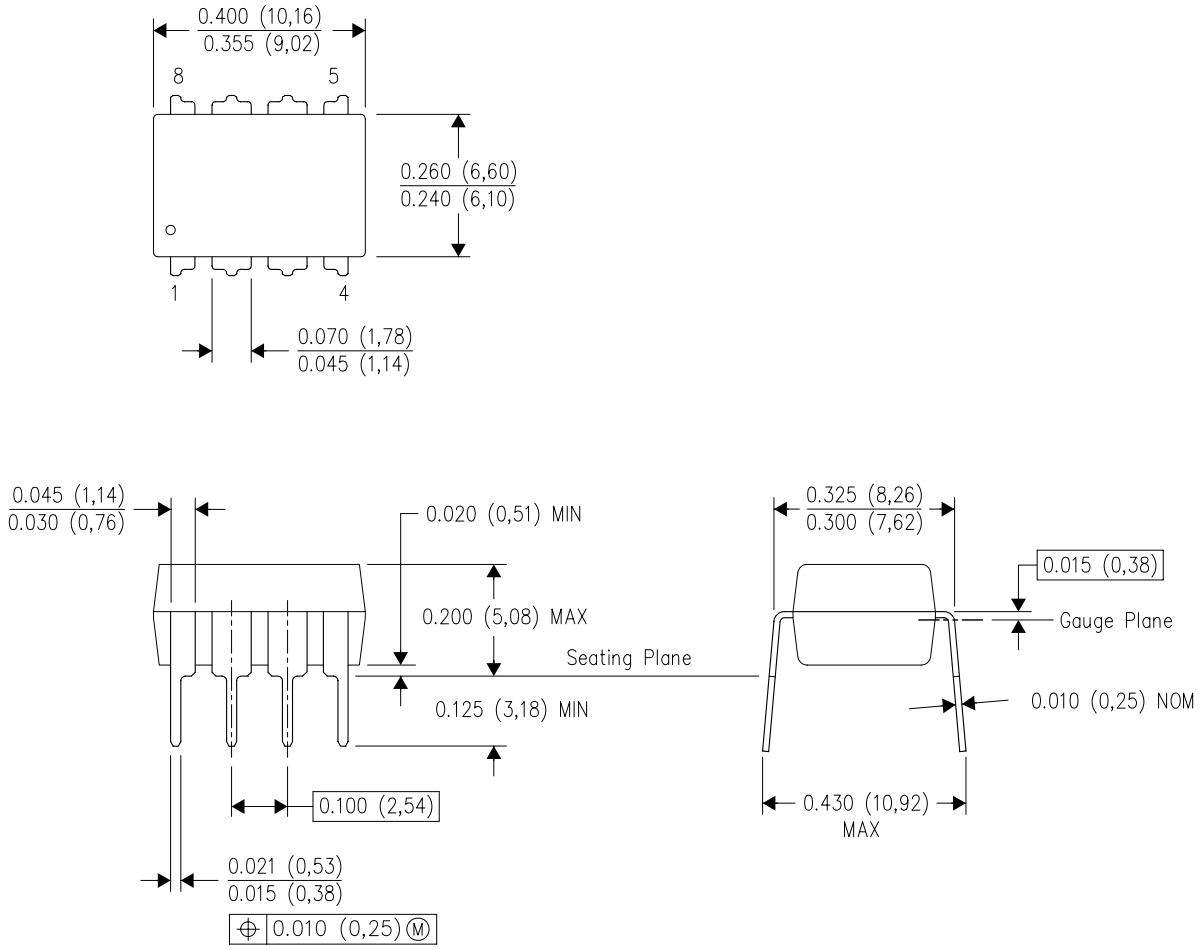
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PS (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

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